VLB ARRAY MEMO No. 421

DIGITIZATION AND RECORDING MEETING AT MIT: SUMMARY

Alan E. E. Rogers
10 January 1985

Attendees:

NRAO:	L. D'Addario	K. Kellermann
	R. Escoffier	J. Romney
	H. Hvatum	P. Sebring
CalTech:	M. Ewing	
MIT/Haystack:	H. Hinteregger	A. Rogers
	J. Levine	J. Salah
	W. Petrachenko	J. Webber
		A. Whitney

A meeting was held at MIT on January 4, 1985 to review and decide upon certain VLBA data acquisition and recorder design issues that were necessary to allow further continuation of the design. The following agreements and action items were reached:

(1) The data acquisition system will record 1 or 2 bits per sample. Data recoded with 1 bit/sample contains only the sign bit and would be processed in the 2-level correlation mode. Data recorded with 2 bits/sample can be processed in a 2, 3 or 4-level correlation mode. Since the correlator may not support 4-level processing data recorded with 2 bit/sample will probably be processed as 3-level data in which case the simple encoding into sign and magnitude bits uses 25% more tape than a more efficient encoding of the data. However it is expected that continuum data will use 2-level quantization recorded as 1 bit/sample which yields about the same SNR as an efficient encoding of 3-levels for the same amount of tape. The threshold level for the sampling of the magnitude will be under software control to allow optimization of the SNR.

(2) The formatter design will include non-data replacement.

(3) The overall concept of the formatter design presented in the block diagram and data flow schematics is acceptable, with possible format enhancements to be considered, and can proceed to the next detailed design phase. Format enhancements to be studied include shortening the frame length, CRC code additions and changes in the sync block.

(4) The specifications on the recorder (Project Book Section 9.1.1, 27 Nov 84) will be changed according to the following:

(a) Change "track" to "channel" on line 36.
(b) Delete "for an averaging time of 10 sec" on line 37 and 38.
(c) Change the criterion on "Fraction of incorrect bits flagged valid (excluding bits out of sync)" to < 3 x 10**-4 on line 43.

These spec changes will also be made formally in the Project Book. Further details will be given in a formal VLBA specification.

(5) Haystack will document its proposed scheme for VLBA error detection, sync acquisition, and sync loss detection. The documentation will include comparisons with alternate methods. NRAO will have a chance to review the scheme before it is considered acceptable. The proposal to use (9,8) parity will be accepted by NRAO if necessary to meet performance goals, but Haystack will consider other methods, taking into account the results of statistical studies now underway. Final decision of the format will be made at the completion of the studies, and will consider schedule constraints.

(6) No error correction is required.

(7) One playback speed and three record speeds are acceptable specifications. The maximum speed-up is 4:1. There is a need for playback slowdown (factor of 2) as a desirable positive option to accommodate correlator processing slowdown in certain experiments. Haystack will estimate cost, performance and other impacts for this option.

(8) Variable phase sampling will not be included in the data acquisition system. It is understood that this will result in a loss in SNR amounting to 3.5% in continuum and somewhat more in outer line channels unless line data is oversampled in which case the losses for 2X oversampling are no more than 3% in the outer channels.

(9) Phase switching will be performed in the L.O., ahead of the baseband converters. The DPS will accomodate the required unscrambling.