VLB ARRAY MEMO No. 504

TIMEKEEPING AT THE VLBA STATIONS

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17 September 1985

1. DESIGN CONSIDERATIONS

The primary time reference at each VLBA station will be a hydrogen maser, which will have outputs at 5 MHz and 100 MHz. The maser will be operated on uninterruptable power, and it should be stable and reliable for long periods of time. Departures of its absolute frequency from the nominal values will be monitored astronomically. However, time references at frequencies much lower than 5 MHz are also needed, as follows:

1. Sampling clock, 1 MHz to 32 MHz with 1 MHz resolution, requiring a 1 MHz reference;
2. Baseband converter LO, 500 MHz to 1000 MHz with 10 kHz resolution, requiring a 10 kHz reference;
3. Station timing signal (for noise source switching, phase switching, etc.), at 20 to 100 Hz;
4. Time of day (TOD) clock, with a period (MSB) of at least several days (probably several years, for convenience).

Because all of these involve frequencies below the lowest maser output frequency, frequency dividers must be used. The phases of these dividers must be known in order to maintain the timing accuracy of the station. Provisions for reading and/or resetting all dividers must be made, including the setting of all digits of the TOD clock.

A procedure must exist within the station (independent of outside references) for verifying that the relative phases of the station's dividers are set in a standard way; and, if not, for resetting them. A procedure must also exist for setting the station to agree with an outside reference. Outside references of several kinds are available: (a) Very coarse time may be sent via computer link (telephone line) from the operations center, subject to uncertainty in the transmission time, including software delays. (b) UTC may be derived to an accuracy of a few msec using signals received at the station from LORAN or similar services, and eventually this may be improved to about 1 μsec using signals from GPS satellites. (c) The most precise time is obtained by astronomical transfer of the clock at another VLBA station (or other VLBI station). In the latter case, rather than actually resetting the station's clock, we will probably just keep, at the operations center, a record of the error. Since the astronomical transfer is time consuming, it is important that once a station's clock error is determined it be as stable as possible. Therefore, a divider with an output period long enough to be resolved by references (a) or (b) must be maintained on uninterruptable power, and perhaps should have a redundant backup.

2. SYSTEM DESCRIPTION

A block diagram of a system satisfying the above requirements is given in Figure 1. Uninterruptable power is supplied to the maser and to a module called the Timing Generator (also to the station computer, but that is not essential to our present purpose). The Timing Generator divides the 5 MHz maser output down to 0.1 Hz, whose period is easily resolved via the link to the operations center. We adopt the convention that this divider should have zero phase at 10 sec boundaries of UTC, and therefore we provide for resetting it to an external UTC second tick (e.g., from a LORAN receiver) upon command from the station computer.

At intermediate stages of the Timing Generator's divider, two other reference signals are derived. These are a 1 MHz reference for the sample clock generator and the TOD clock, and the Station Timing Signal (here taken to be 80 Hz, as further discussed below). The STS must have a period long enough to be resolved by the Monitor/Control Bus (MCB), through which the station computer communicates with all equipment at the station; under ideal conditions, the MCB can resolve about 1 msec, but to be safe we should not count on resolving less than 10 msec in this way, because the MCB and the computer may be busy with other tasks. The STS is distributed throughout the station, including the station computer, where it generates an interrupt for each STS period. The computer can thus maintain an interrupt counter; if it has modulus 800, it will be in phase with the similar counter in the Timing Generator, so that we have a redundant 10 sec clock. Agreement between these can be checked because provision is made for the computer to read the mod-800 divider in the Timing Generator.

All other dividers can be reset to "agree" with the Timing Generator by means of the STS. Since the computer is able to determine the exact time at each STS rising edge, it can command that any counter be cleared on a specific STS transition. This applies to the sample clock divider and the baseband converter LO divider.

The TOD clock is a little more complicated. It is split into two parts that are separately readable and setable by the computer. The first divides down to 10~sec period with 1/(32~MHz) resolution; it can be set to agree with the Timing Generator without need for an outside reference. The other part divides down to the maximum period and needs outside data for setting, but its resolution is low enough that this data can be sent from the operations center. In both cases, the resetting occurs on an edge of the STS, so that the computer can command it to occur at the correct time using the MCB.

For monitoring purposes, a 0.1 Hz signal is brought out of the TOD clock to the Timing Generator, where it is compared with the phase of the 0.1 Hz signal there; any phase difference sets an error status bit that is readable by the computer.

3. CHOICE OF STATION TIMING SIGNAL FREQUENCY

This signal may be used for many purposes, so the choice of frequency is a compromise. For maintaining the station timing, almost any frequency resolvable by the MCB will do. For convenience, it should have an integral number of cycles in a small, integral number of UTC seconds (here 800 cycles exactly in 10 sec). It should also be harmonically related to 60 Hz (here four STS cycles equals three cycles of 60 Hz), so that any line-frequency interference will average out in measurements made over some integral numbers of STS cycles.

The STS may also be used to control noise source switching and/or phase switching. For these purposes, its frequency should be fairly high, to allow for complicated switching cycles in a reasonable period. It is this consideration that drives the frequency as high as 80 Hz.

The selection of 80 Hz for this discussion should be considered an example only, subject to change.

The rise time of the STS signal received at most devices must be fast enough to resolve one cycle of the next higher frequency time reference received by that device. This is never higher than 5 MHz (200 nsec resolution needed). For the TOD clock and sample generator, it would be desirable to be able to resolve one cycle of 32 MHz (30 nsec), since resettings would then account for any phase shift through the times-32 multiplier.

4. EXAMPLES OF PROCEDURES

A. For setting TOD Clock to Timing Generator:

This procedure is appropriate if power has been lost, or the clock is believed to be in error for any reason, but the Timing Generator is believed to be still at the proper phase.

1. Wait for next STS interrupt.
2. Determine MSB of time (10 sec resolution) by transfer from AOC via telphone link.
3. Determine LSB of time by dividing current interrupt count (since last 10 sec boundary) by 96 Hz. If the computer's internal count is in doubt, it can be checked against the count in the Timing Generator via the MCB.
4. Load MSB and LSB of time into clock latches via MCB. Command clock to reset from latches at next STS edge.

B. For setting Timing Generator to external 1 Hz reference:

1. Determine UTC to 1 sec accuracy. This may be achievable via computer link from the operations center, but if not it can be obtained by decoding signals from LORAN or GPS; this requires interfacing the appropriate receiver to the MCB.
2. Wait for the next 10 sec boundary of UTC.
3. Command Timing Generator to reset on next 1 Hz reference edge.
4. Reset TOD clock (procedure above), sample clock generator, and BB converter LO generator to agree with Timing Generator.

C. For resetting coarse bits of TOD clock and TG (e.g., inserting a leap second):

1. During the STS cycle just before the desired reset time, load the MSB latch of the TOD clock with the new time and command a reset on the next STS edge.
2. Count STS interrupts to determine the next 10 sec boundary of UTC. During the STS cycle just before this boundary, command the coarse divider in the TG (STS to 0.1 Hz) to reset on the next STS edge. For a leap second insertion, this will require waiting either 1 sec or 9 sec, depending on the sign of the leap second.
3. Note that during the interval between steps 1 and 2, the comparitor will indicate an error. This should be ignored.

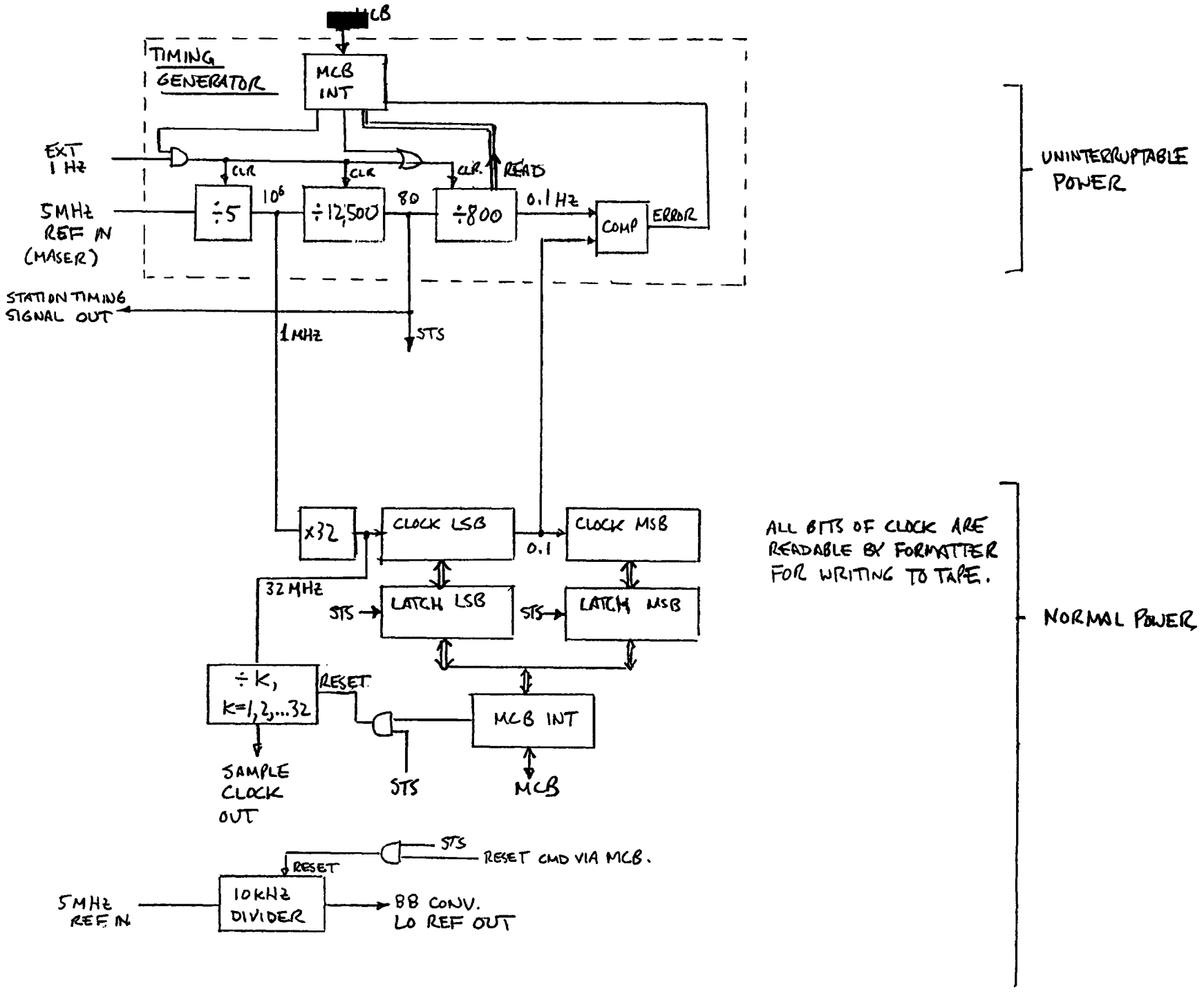
MCB
TIMING GENERATOR
MCB INT
EXT 1 Hz
CLR
CLR
CLR
READ
5MHz REF IN (MASER)
÷5
10^6
÷12,500
80
÷800
0.1 Hz
COMP
ERROR
UNINTERRUPTABLE POWER
STATION TIMING SIGNAL OUT
1 MHz
STS
x32
CLOCK LSB
CLOCK MSB
0.1
32 MHz
STS
LATCH LSB
STS
LATCH MSB
ALL BITS OF CLOCK ARE READABLE BY FORMATTER FOR WRITING TO TAPE.
NORMAL POWER
÷K, K=1,2,...32
RESET
MCB INT
SAMPLE CLOCK OUT
STS
MCB
STS
RESET
RESET CMD VIA MCB.
5MHz REF IN
10kHz DIVIDER
BB CONV. LO REF OUT

Figure 1