VLB ARRAY MEMO No. 57

NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

MEMORANDUM

January 20, 1982

To: VLB Working Group

From: R. Lacasse

Subj: Data Digitization Electronics

The function of manipulating the four wideband IF signals from the Vertex Cabin into four bit streams suitable to the recorder is performed by the Data Digitization Electronics (DDE). A few miscellaneous functions, as discussed below, are also performed by the DDE. As shown in Figure 1, the DDE consists of an IF Processor, four IF to Video Converters, a Sampler, Delay Calibrator, Time of Day Clock, RS232 Distributor, and 5 MHz Distributor. The design is based on the Mark III system, modified for fewer converters with wider bandwidths, and with the data formatting and quality monitoring left to the recorder electronics.

As shown in Figure 2, the IF Processor has four IF inputs in the band from 300 MHz to 1500 MHz. Each of these inputs is frequency translated, with 10 kHz resolution, such that the lower edge of the band of interest is at 500 MHz. This section of the DDE is best implemented in the Vertex Cabin, to avoid sending wideband signals through long lengths of cable and then having to deal with the resulting frequency dependent cable attenuation.

As a result of the frequency agility of the IF Processor, the Video Converters can be relatively simple. Primarily, they frequency translate the outputs of the IF Processor to baseband, using fixed 500 MHz oscillators, and single sideband networks. The Video Converters also provide IF level setting attenuators, and selectable output bandwidths of 14 MHz, 3.5 MHz, 1 MHz, 500 kHz, 250 kHz, and 125 kHz. Video, IF, and LO power levels are monitorable.

The Sampler produces one-bit, 2 level samples of the filtered, baseband data at a maximum rate of 28 Mbps. The sampling clock is derived from the 5 MHz reference using phase-locked techniques; oversampling is easily accomplished for the narrow bandwidths. Both the sampled data streams and the sampling clock are transmitted to the recorder. A Time-of-Day Clock output is also transmitted to the recorder.

The Delay Calibrator in the DDE is the same as that used in the Mark III system with the exception that it also includes a self-contained counter and communicator module. The Delay Calibrator provides a 5 MHz reference to the Vertex Phase Calibrator System, and also measures the round trip delay in the 5 MHz reference cable.

Communication to the host computer is implemented as in the Mark III system: each module includes an RS232 transceiver which is assigned an address on an RS232 link. A module responds according to a well defined protocol when it is addressed. Thus, all significant functions in the DDE are remotely controllable and/or observable.

Hardware costs are broken down in Table 1, and manpower requirements in Table 2.

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Enclosures
1. Table 1: Data Digitization Electronics Hardware Cost Breakdown
2. Table 2: Data Digitization Electronics Manpower Requirements
3. Figure 1: Data Digitization Electronics Block Diagram
4. Figure 2: Data Digitization Electronics IF Processor

TABLE 1

Data Digitization Electronics Hardware Cost Breakdown

Item	Cost
IF Processor	$36 K
IF to Video Converters	12 K
Sampler	2 K
RS232 Distributor	1 K
Delay Calibrator	3 K
Rack, Power Supplies, Connectors, etc.	10 K
5 MHz Distributor	2 K
Total	$66 K

TABLE 2

Data Digitization Electronics Manpower Requirements

Item	Time (Man-Months)
Design and Document	14
Order	1
Assemble	50
Total	65

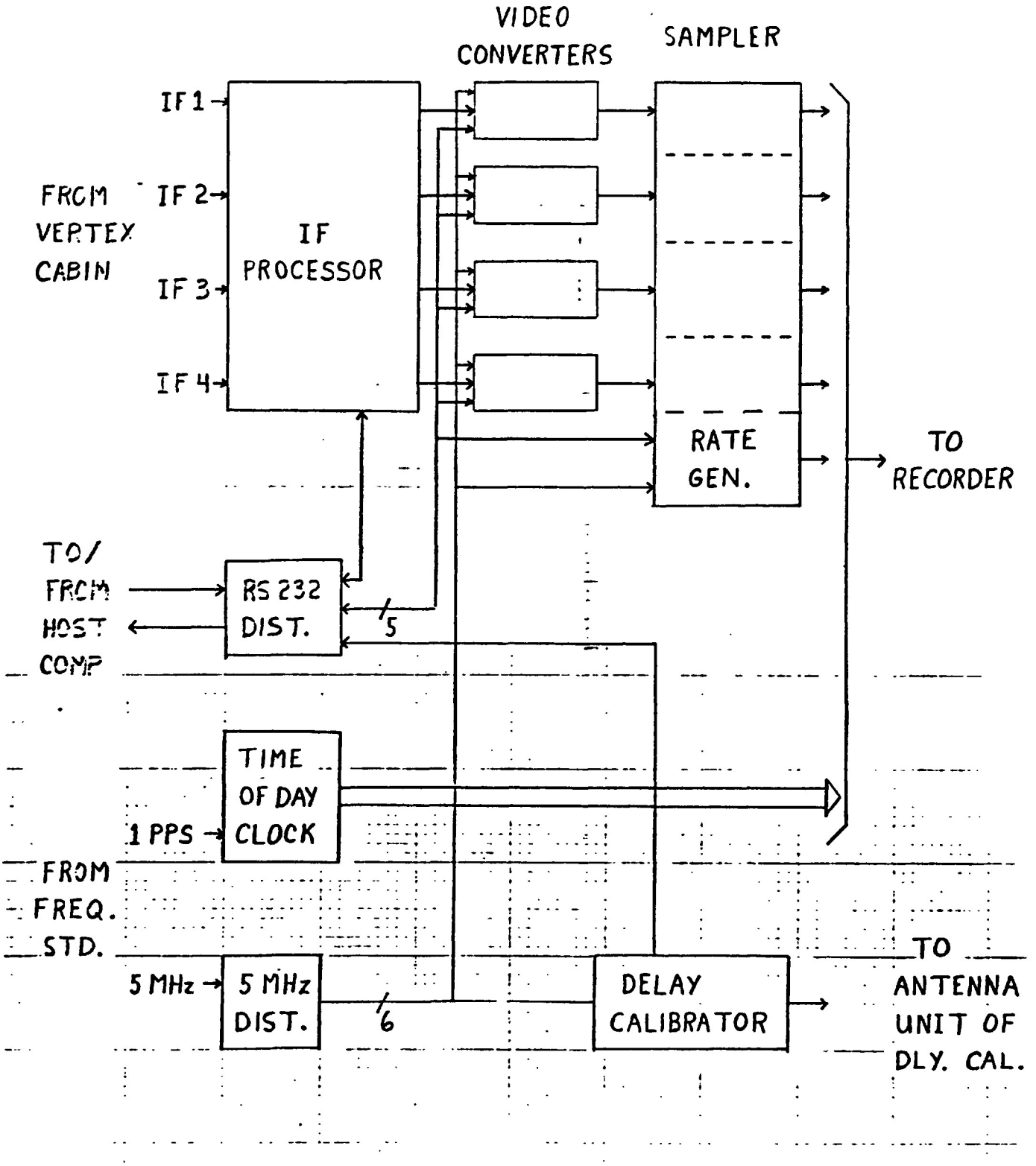

FIGURE 1

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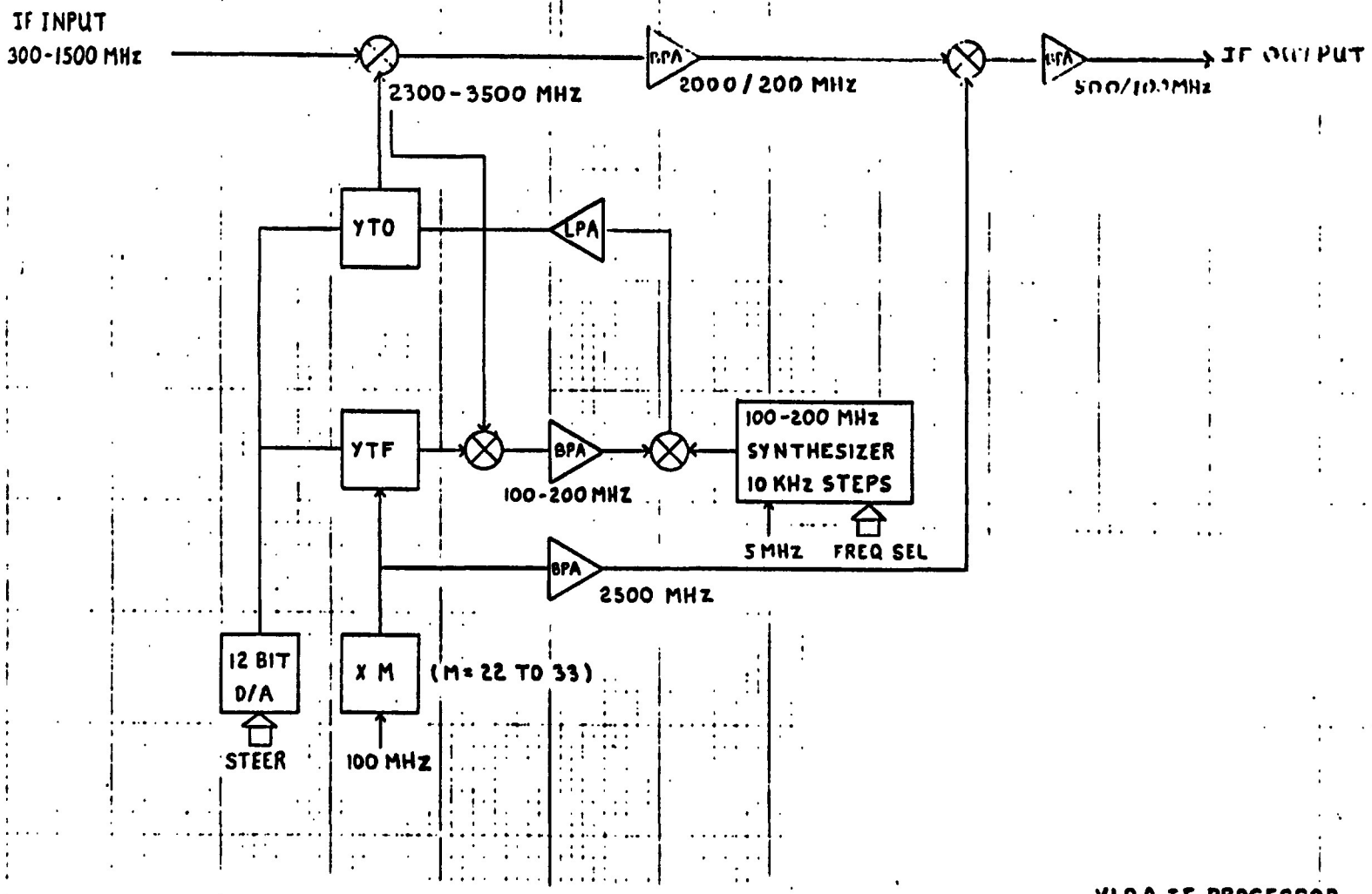

NOTE: ONLY ONE OF FOUR IDENTICAL CHANNELS IS SHOWN.

VLBA IF PROCESSOR
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FIGURE 2