VLBA CORRELATOR DESIGN

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The purpose of this document is to present some estimates of the size and cost of a VLBA correlator based on the JPL/Caltech Block II system.

This system uses Mark III tapes (28 tracks) and will run at 8 Mb/s. Notice, therefore, that the total bit rate (224 Mb/s) and bandwidth (112 Mhz) capability is double that of the VLA-based proposal (VLBA Memo #61). Only about 20% in cost would be saved by cutting back to 112 Mb/s, since the total number of lag channels must remain constant. We therefore keep the full Block II processing rate in most of these estimates. (Excess processor capacity is highly desireable to reduce logistical bottlenecks.)

We choose 12 stations as a reasonable compromise between redundancy, network extension capability, and cost. Cost for this design has the following station dependency:

Cost ~ N + 2 * N**2 (N = no. of stations)

if the number of lags per baseline is held constant, or,

Cost ~ N + 0.8 * N**2

if the total number of lags is kept constant.

We analyze four cases of correlators that might be built:

- Block II, enlarged to 12 stations, 8 lags/baseline/track continuum, 112 frequency channels/baseline spectral line
- Block II, 12 stations, 32 lags/baseline/track continuum, 448 frequency channels/baseline
- Block II, 12 stations, 32 lags/baseline/track continuum, 448 frequency channels/baseline, with gate array technology
- Block II, 12 stations, 64 lags/baseline/track continuum, 448 frequency channels/baseline, with gate array technology, only 14 tracks at 8 Mbs each.

1. Enlarged Block II

We begin by estimating the parts count for a correlator using exactly the Block II design, with the following exceptions:

12 stations, 66 baselines
32 lag channels per baseline

This design is largely completed; it makes heavy use of LSI ICs that have become available in the past 1-2 years.

The following tables summarize the integrated circuit (IC) usage and power consumption of the Block II (current design).

STATION-ORIENTED ELECTRONICS

	IC count	Power (w)
"ECL" Front-end	450	160
Delay buffering	1200	500
Phase Calibrator	620	275
Station Controller	60	25
Station Phase Gen.	175	75
	2505	1035

BASELINE-ORIENTED ELECTRONICS (per group of 3 baselines)

Cross-corr.	2400	1050
Corr. Controller	60	25
Corr. Phase Processor	175	75
Corr. Sig. Processor	175	75
Fringe Proc. (Tensor)	500	160
	3310	1385

2. Block II, Quadrupled Lags

Of the baseline-oriented components in Block II, only about 1/3 are actual lag-channels. That is, a 32-lag version would have only 4*(1/3)+2/3, or twice the number of ICs per 3-baseline group. This option is called "4 X Block II" in the table below. It provides "full" spectroscopic capability of at least 448 frequency channels per baseline.

3. Enhanced Block II Design

The economics of the Block II approach for a large correlator improve considerably with the state of the art in VLSI (very large scale integration) technology. In fact, a 30 - 50% compression of the correlator chip count has become feasible in the last months with the introduction of a larger capacity PAL (programmed array logic) chip.

In making a final, "best-guess" estimate of the cost of the real VLBA correlator following these design principles, it is necessary to estimate the level of 1985 VLSI. We feel that the following projections are conservative.

We anticipate that a custom gate array in the range 4,000 - 10,000 gates will be available and will be the optimum choice for a Block II-style implementation in the near future. One-time charges of $30,000 - $40,000 are likely for mask layouts. We assume the total IC count in the lag-dependent sections of the correlator will be reduced by a factor of 4. The gate arrays will cost about double per chip compared to the ICs currently used.

The overall effect would be to reduce chip count by 73 K and reduce parts cost by $350 K. Other cost savings due to generally falling prices of memory and other LSI components may be expected, but are not included here.

4. Gate arrays with reduced total bit rate.

(This example is most directly comparable with the VLA-based design.)

Nearly half the station-dependent circuitry is eliminated, as are parts of the baseline-dependent components. Since the total number of lag channels is constant (due to spectral-line requirements), the same savings are available from gate-array technology.

ESTIMATES

We derive the following estimates for a 12-station correlator using the Block II parallel LSI techniques. If we use a fairly conservative overall estimate of $10 per IC including printed circuit packaging, power supplies, etc., we arrive at the hardware costs indicated. (The gate array design includes an adjustment that allows for the relatively higher price expected for the gate arrays themselves.)

System	IC count	Parts $	Labor Constr.	Labor Devel.
1. Block II, 8 lags/bsl/track	103 K	$1,030 K	4 MY	1 MY
2. 4 X Block II (32 lags)	176 K	$1,760 K	7 MY	3.3 MY
3. 4 X Block II (32 lags, gate arrays)	103 K	$1,270 K	4 MY	4.3 MY
4. Block II (14 tracks, gate arrays, 64 lags/bsl/track)	68 K	$ 950 K	3 MY	4.6 MY

Development labor includes printed circuit layouts, prototyping, gate array design, microcoding, mechanical design, and documentation, as required.

Construction labor includes clerical, mechanical, integration, and test functions.

CONTROL COMPUTER

A VAX-11/780 computer operating in a general-purpose timesharing mode serves as the control computer for the Block II. This is possible because of the substantial computational power residing in the correlator itself. Geometry, phase calibration, and tape control are all performed in Block II's microprocessors. Coherent integrations, bandwidth synthesis, and first-stage fringe analysis are handled in the "Tensor" processors (one for every 3 baselines) that contain hardware FFT systems, large buffers, and M68,000 control computers.

We estimate that a single, dedicated VAX system will be adequate for the 12-station, quadrupled Block II correlator. Such a system would include 2 MByte memory, dual 6250 bpi tape units, and 600 MB disk capacity. Existing Block II software will be adequate for continuum observing. (A VAX computer is required to make use of this software.) Substantial new programming will be needed for spectral line work. Estimates are given in the following table.

COMPUTER ESTIMATES

Hardware (VAX-11/780 with peripherals):		$370 K
Software:	Systems Programming	1 MY
	Spectroscopy	4 MY

CONCLUSIONS

The cost of a "conventional" VLBI correlator architecture is at least competitive with the alternative VLA-based design. The Block II/Mark III system offers 112 MHz bandwidth at record time or 56 MHz with twice-real-time playback rate. Adaptations of the Block II design could be made to work with other channelization parameters, with some parts-count savings, but with some redesign required.

In particular, correlator option 4 would be compatible with the 7-tape 16 Mb/s/tape cassette system now being proposed.

The Block II incorporates full recorder controls, deskewing and delay buffering, phase calibration, and fringe processing. Many aspects of its design derive from its principle application to geodesy and bandwidth synthesis. Relatively little, however, is to be gained by changing the design to eliminate the generality of the bandwidth synthesis capabilities.

Full spectroscopic and polarization capabilities (4 correlations per frequency) are provided in the "4 X Block II" design.

The cost attractiveness of Block II's "LSI-parallel" approach compared to the VLA recirculating technique can be expected to improve as VLSI's density grows faster than ECL's speed.