NATIONAL RADIO ASTRONOMY OBSERVATORY
Socorro, New Mexico

VLBA TECHNICAL REPORT NO. 19
(Rev. A, December 1995)

RACK-B INTERFACE MODULE
M102

E. Schlecht
July 1990

Rev. A
J. Oty
December 1995

Table of Contents

Specifications

Maximum Voltage to Analog Inputs	+/- 20 Volts
Analog Voltage Measurement Range	+/- 10 Volts
Module Serial Number Relative Address	22 hexadecimal
Address ID Code Range	40 - 43 hexadecimal
Analog Monitor Relative Address Range	00 - 0F hexadecimal
Digital Monitor Relative Address Range	10 - 21 hexadecimal
Command Relative Address Range	10 - 20 hexadecimal
Power Supply Voltages Required	+5, +/-15 and +28 Volts

Rack-B Interface Module (M102)
[ID No. 40h]
COMMANDS

Relative Address(es) (hex)	Function
10	S101 - T101 (330 MHz) Converter Test Switch[1]
12	S103 - T103 (1.5 GHz) Converter Test Switch
13	S104 - T104 (2.3 GHz) Converter Test Switch
14	S105 - T105 (4.8 GHz) Converter Test Switch
15	S106D - T106 (8.4/23 GHz) Converter Dual Channel Switch[2]
16	S107 - T107 (10.7 GHz) Converter Test Switch
17	S108 - T108 (15 GHz) Converter Test Switch
18	Bin C Spare Converter Test Switch
19	S110C - T110 (43 GHz/ALT) Converter Test Switch
1A	S110AB - T110 (43 GHz/ALT) Converter Input Select Switch[3]
22	Clear 1 - bit (C/M 0) commands[4]

Other COMMANDS not used in present system

Rel. Addr. (hex)	Type	Description	Label
11	1 - bit	Relay Driver	RD2
1B	1 - bit	Relay Driver	RD12
1C - 1F	1 - bit	TTL Level	C9 - C12
20	8 - bit	word TTL level	C1 - C8

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[1] A COMMAND of 0 to the address puts switch in position 0 (NORMAL)
A COMMAND of 1 to the address puts switch in position 1 (TEST)
The TEST position reverses the channels inside the converter.

[2] A COMMAND of 0 = DUAL Channel (NORMAL), 1 = SINGLE Channel (GEODESY)

[3] A COMMAND of 0 to the address puts switch in position 0 (NORMAL)
A COMMAND of 1 to the address puts switch in position 1 (ALT INPUT)

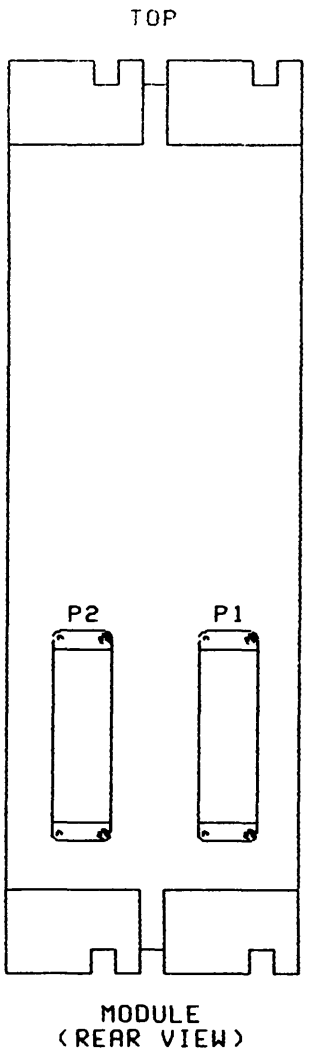
[4] Any command to Relative Address 22h will clear the 1 - bit commands (Relative Address 10h thru 1Fh)

MONITORS (Cont.)

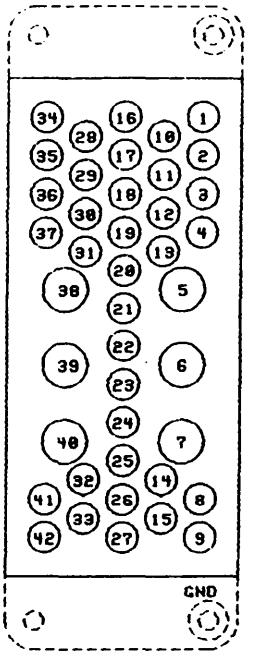
Other MONITORS not used

Rel. Addr. (hex)	Type	Description	Bits	Label
0A-0D	Analog	Differential Monitor		AV11 - AV14
11	Digital	1-bit Relay Driver Readback	0	RD2
1C-1F	Digital	1-bit TTL Level Readback	0	C9 - C12
20	Digital	8-bit TTL Level Readback	0 - 7	C1 - C8

42-PIN REAR PANEL CONNECTOR PINOUT



MODULE
(REAR VIEW)



P1
(REAR VIEW)

P1 42 PIN AMP					
PIN	FUNCTION	COMMENT	PIN	FUNCTION	COMMENT
1	T101 TEST SWITCH		22	ID 0	
2	RD 2		23	ID 1	
3	T103 TEST SWITCH		24		
4	T104 TEST SWITCH		25	PARITY	
5			26	TS5 + (+15V)	
6			27	TS5 + (+15V)	
7			28		
8	XMIT +		29	+ 28V SUPPLY	
9	XMIT -		30	T110 MUX SWITCH	
10	+5V SUPPLY	950 mA	31	RD 12	
11			32	TS3 + (+15V)	
12	T105 TEST SWITCH		33	TS4 + (+15V)	
13	T106 MUX SWITCH		34	GROUND	
14	RCV +		35		
15	RCV -		36		
16	+15V SUPPLY	80 mA	37	RLY MON 2	
17	-15V SUPPLY	40 mA	38		
18	T107 TEST SWITCH		39		
19	T108 TEST SWITCH		40		
20	T109 TEST SWITCH	(NOT USED)	41	T110 MUX SWITCH	
21	T110 TEST SWITCH		42	GROUND	

Description of I/O Lines

42-PIN REAR PANEL CONNECTOR:

T101 Test Switch:	Relay Driver output to T101 Converter Test Switch
RD 2:	Unused Relay Driver output
T103 Test Switch:	Relay Driver output to T103 Converter Test Switch
T104 Test Switch:	Relay Driver output to T104 Converter Test Switch
XMIT +, XMIT - :	Monitor/Control transmit bus input from station computer
+5 Volt Supply:	+5 Volt input from Power Supply
T105 Test Switch:	Relay Driver output to T105 Converter Test Switch
T106 Test Switch:	Relay Driver output to T106 Converter Test Switch
RCV +, RCV - :	Monitor/Control receive bus output to station computer
+15 Volt Supply:	+15 Volt input from Power Supply
-15 Volt Supply:	-15 Volt input from Power Supply
T107 Test Switch:	Relay Driver output to T107 Converter Test Switch
T108 Test Switch:	Relay Driver output to T108 Converter Test Switch
RD 9:	Relay Driver output to spare Converter (unused)
T110 Test Switch:	Relay Driver output to T110 Converter Test Switch
T110 Input Sel Sw:	Relay Driver output to T110 Converter Input Select Switch
T110 Input Sel Sw:	Relay Driver output to T110 Converter Input Select Switch
ID 0 - 1:	ID input to MCB Standard Interface Board
Parity:	ID Parity input to MCB Standard Interface Board
RD 12:	Relay Driver output spare (unused)
TS 5+, 6+ :	+15 Volt output to Temperature Sensors 5 and 6
+28 Volt Supply:	+28 Volt input from Power Supply
TS 3+, 4+ :	+15 Volt output to Temperature Sensors 4 and 5
Ground:	Module ground for signals and return for power supplies
RLY Mon 2:	Input from contact 2 of external relay

50-PIN REAR PANEL CONNECTOR

100 M RX IN DET:	Analog input from LO Rcvr 100 MHz In Detector
500 M RX IN DET:	Analog input from LO Rcvr 500 MHz In Detector
100 M RX OUT DET:	Analog input from LO Rcvr 100 MHz Out Detector
500 M RX OUT DET:	Analog input from LO Rcvr 500 MHz Out Detector
TS 3- to 6-:	Inputs from temperature sensors 3 to 6
HT Cur +/-:	Heater current differential analog input
T103 Det & Gnd:	Input from T103 Converter LO Detector
AV11+/-, AV12+/-:	Inputs from VR HVAC monitor circuit
AV13+/-, AV14+/-:	Unused analog inputs
TS 1 & TS2:	Temp sensors inputs from 1 and 2
RLY MON 1:	Input from external relay contact 1
RX LOCK DET:	Input from lock detector in LO RCVR
M3 - M12:	TTL monitor inputs (bit 7 used for HVAC Comp Mon)
C1 - C12:	Command bits (unused)

I. General Description

The B-Rack Interface is a general purpose interface module designed to allow monitoring of analog and digital inputs , as well as the control of various systems using TTL level outputs and 28 volt outputs. Specifically, the B-Rack Interface is used to monitor the LO Receiver power levels and lock status, and the B-Rack and room temperatures. Further, the module is used to control switches in the converter modules used to test and troubleshoot the RF/IF system.

II. Circuit Description.

Referring to the schematic, the module consists of two parts, operationally. On the left hand side of the diagram is the circuitry that interfaces to the Monitor and Control Standard Interface Board (SIB). IC's 3B, 5A and 5C are used for address decoding. 3B is a digital multiplexer which is required because some sections of the address space are further decoded in the latch IC's, whereas the rest must be completely decoded. ADDR 5 makes the selection, which means that addresses up to 0Fh are decoded completely, down to ADDR 0, by decoder IC's 5A and 5B. IC 5A decodes the write requests and 5B decodes the read requests. Addresses starting at 10h are decoded into 8-address blocks. The signals for the 8-address blocks go to IC's 2D, 2E, 3D and 3E which are 8-addressable latches and 8-bit selectors. These serve as single bit latches and readback buffers.

IC's 2D and 2E latch the 1-bit commands, and 3D and 3E allow the latched outputs to be read back. IC's 2B and 2C are 28 volt relay drivers. Lines C9 - C12 are regular TTL outputs. IC 1E is a standard 8-bit single byte output latch, and 1D is its readback buffer. 2A is the ID read buffer (see specification A55001N002-A). The ID byte comes partly from three inputs, ID 0 and ID 1 which are brought in from outside the module and ID 2 which is held low inside the module, and allow the ID to be selected from eight possible combinations, 40h to 47h. IC 1C reads the module serial number set on DIP switch 4E. IC's 1A and 1B provide for the monitoring of one single word of 12-bits TTL level. IC 3A is a power up reset. If power fails, this IC resets the output latches to logical 0.

The module allows 8 differential and 8 single-ended analog inputs to be monitored, IC 3C is a single ended 8-input CMOS analog multiplexer for the single ended inputs (pins A - J on the 50-pin rear panel connector). Normally its output, and the reference ground, would go to one of the differential inputs on the SIB. This would allow 15 analog inputs - 8 single-ended from the multiplexer along with the 7 remaining differential. However, 8 differential inputs are required, so the CMOS switch 4D was added. When the eighth differential input is requested for monitoring, the switch selects it to send the eighth differential input to the SIB. When the single-ended multiplexer is selected, the switch passes the multiplexer output along with the reference ground to the SIB's eighth input. The selection is made by IC 5B which normally selects the multiplexer. When the address

III. Test Procedure.

The original test procedure for this module was used at Charlottesville during the construction phase. This test hardware and software is not used at the AOC. Repair and testing is now done by the DCS group with final checkout in the AOC test racks.

VLBA B-RACK INTERFACE MODULE (M102) WIRING HARNESS
DRAWING NO: A53510W004 W. WIREMAN 5/27/88
REVISION: C 12/28/95 J. OTY

PART I WIREWRAP CONNECTOR WIRING

PIN	FUNCTION	SOURCE	COLOR	GA.	PIN	FUNCTION	SOURCE	COLOR	GA.
1	GND	TB1-1	BLK	22	2	5V	TB1-7	ORG	22
3	GND	CHASS	BLK	22	4	5V			
5	AV1	FT-1	WHT/BLU	26	6	AV2	FT-2	WHT/ORG	26
7	AV3	FT-3	WHT/GRN	26	8	AV4	FT-4	WHT/BRN	26
9	TS3	FT-5	WHT/GRY	26	10	TS4	FT-6	WHT/VIO	26
11	TS5	FT-7	WHT/YEL	26	12	TS6	FT-8	WHT/BLK	26
13	HTCUR+	FT-9	WHT/BLU	26	14	HTCUR-	FT-10	WHT/ORG	26
15	C/M 0	P1-33	WHT/GRN	26	16	C/M 1	P1-16	WHT/BRN	26
17	C/M 2	P1-32	WHT/GRY	26	18	C/M 3	P1-15	WHT/VIO	26
19	C/M 4	P1-31	WHT/YEL	26	20	C/M 5	P1-14	WHT/BLK	26
21	C/M 6	P1-30	WHT/BLU	26	22	C/M 7	P1-13	WHT/ORG	26
23	C/M 8	P1-29	WHT/GRN	26	24	C/M 9	P1-12	WHT/BRN	26
25	C/M 10	P1-28	WHT/GRY	26	26	C/M 11	P1-11	WHT/VIO	26
27	GND	CHASSIS	BLK	22	28	TS RET	P1-24	BLK	22
29	C/M 12	P1-27	WHT/YEL	26	30	C/M 13	P1-10	WHT/BLK	26
31	C/M 14	P1-26	WHT/BLU	26	32	C/M 15	P1-9	WHT/ORG	26
33	ANLG 1+	P1-1	WHT/GRN	26	34	ANLG 1-	P1-18	WHT/BRN	26
35	ADDR 0	P1-48	WHT/GRY	26	36	ADDR 1	P1-47	WHT/VIO	26
37	ADDR 2	P1-46	WHT/YEL	26	38	ADDR 3	P1-45	WHT/BLK	26
39	ADDR 4	P1-44	WHT/BLU	26	40	ADDR 5	P1-43	WHT/ORG	26
41	DEV REQ	P1-35	WHT/GRN	26	42	DEV ACK	P1-36	WHT/BRN	26
43	R/W	P1-49	WHT/GRY	26	44	ID READ	P1-9	WHT/VIO	26
45	ANENB	P1-37	WHT/YEL	26	46	HI-LO SEL	P1-17	WHT/BLK	26
47	RD 1	FT-49	WHT/BLU	26	48	RD 2	FT-50	WHT/ORG	26
49	GND	CHASSIS	BLK	22	50				
51	RD 3	FT-51	WHT/GRN	26	52	RD 4	FT-52	WHT/BRN	26
53	RD 5	FT-53	WHT/GRY	26	54	RD 6	FT-54	WHT/VIO	26
55	RD 7	FT-55	WHT/YEL	26	56	RD 8	FT-56	WHT/BLK	26
57	RD 9	FT-57	WHT/BLU	26	58	RD 10	FT-58	WHT/ORG	26
59	RD 11	FT-63	WHT/GRN	26	60	RD 12	FT-64	WHT/BRN	26
61	C 1	FT-37	WHT/GRY	26	62	C 2	FT-38	WHT/VIO	26
63	C 3	FT-39	WHT/YEL	26	64	C 4	FT-40	WHT/BLK	26
65	C 5	FT-41	WHT/BLU	26	66	C 6	FT-42	WHT/ORG	26
67	C 7	FT-43	WHT/GRN	26	68	C 8	FT-44	WHT/BRN	26
69	C 9	FT-45	WHT/GRY	26	70	C 10	FT-46	WHT/VIO	26
71	C 11	FT-47	WHT/YEL	26	72	C 12	FT-48	WHT/BLK	26
73	GND	CHASSIS	BLK	22	74	PA	FT-62	WHT/BRN	26
75	RLYMON1	FT-25	WHT/BLU	26	76	M 2	FT-26	WHT/ORG	26
77	M 3	FT-27	WHT/GRN	26	78	M 4	FT-28	WHT/BRN	26
79	M 5	FT-29	WHT/GRY	26	80	M 6	FT-30	WHT/VIO	26

PART II STANDARD INTERFACE BOARD WIRING

JACK P1					JACK P2				
PIN	FUNCTION	SOURCE	COLOR	GA.	PIN	FUNCTION	SOURCE	COLOR	GA.
1	ANLG 1+	W-33	WHT/GRN	26	1	5V			
2	T103DET+	FT-11	WHT/GRN	26	2				
3	AV 11+	FT-13	WHT/GRY	26	3				
4	AV 12+	FT-15	WHT/YEL	26	4				
5	AV 13+	FT-17	WHT/BLU	26	5				
6	AV 14+	FT-19	WHT/GRN	26	6				
7	TS1 OUT	W-87	WHT/VIO	26	7				
8	TS2 OUT	W-89	WHT/BLK	26	8				
9	C/M 15	W-32	WHT/ORG	26	9	ID READ	W-44	WHT/VIO	26
10	C/M 13	W-30	WHT/BLK	26	10				
11	C/M 11	W-26	WHT/VIO	26	11				
12	C/M 9	W-24	WHT/BRN	26	12				
13	C/M 7	W-22	WHT/ORG	26	13				
14	C/M 5	W-20	WHT/BLK	26	14	5V	TB1-7	ORG	22
15	C/M 3	W-18	WHT/VIO	26	15	15V	TB1-3	RED	22
16	C/M 1	W-16	WHT/BRN	26	16	-15V	TB1-4	YEL	22
17	HI-LO SEL	W-46	WHT/BLK	26	17	GND	TB1-1	BLK	22
18	ANLG 1-	W-34	WHT/BRN	26	18				
19	T103DETG	FT-12	WHT/BRN	26	19	RCV+	FT-66	WHT (TP)	26
20	AV 11-	FT-14	WHT/VIO	26	20	RCV-	FT-75	BLK (TP)	26
21	AV 12-	FT-16	WHT/BLK	26	21	XMIT+	FT-65	RED (TP)	26
22	AV 13-	FT-18	WHT/ORG	26	22	XMIT-	FT-74	BLK (TP)	26
23	AV 14-	FT-20	WHT/BRN	26	23				
24	TS RET	W-28	BLK	26	24				
25	TS RET	P1-24	BUSS	26	25	GND			
26	C/M 14	W-31	WHT/BLU	26					
27	C/M 12	W-29	WHT/YEL	26					
28	C/M 10	W-25	WHT/GRY	26					
29	C/M 8	W-23	WHT/GRN	26					
30	C/M 6	W-21	WHT/BLU	26					
31	C/M 4	W-19	WHT/YEL	26					
32	C/M 2	W-17	WHT/GRY	26					
33	C/M 0	W-15	WHT/GRN	26					
34	GND								
35	DEV REQ	W-41	WHT/GRN	26					
36	DEV ACK	W-42	WHT/BRN	26					
37	ANENB	W-45	WHT/YEL	26					
38	GND	TB1-1	BLK	22					
39	-15V	TB1-4	YEL	22					
40	15V	TB1-3	RED	22					

PART III REAR PANEL CONNECTOR WIRING

JACK 1 (AMP 42 PIN)									
PIN	FUNCTION	SOURCE	COLOR	GA.	PIN	FUNCTION	SOURCE	COLOR	GA.
1	RD 1	FT-49	WHT/BLU	26	2	RD 2	FT-50	WHT/ORG	26
3	RD 3	FT-51	WHT/GRN	26	4	RD 4	FT-52	WHT/BRN	26
5					6				
7					8	XMIT+	FT-65	RED (TP)	26
9	XMIT-	FT-74	BLK (TP)	26	10	5V	FT-68	ORG	20
11					12	RD 5	FT-53	WHT/GRY	26
13	RD 6	FT-54	WHT/VIO	26	14	RCV+	FT-66	WHT (TP)	26
15	RCV-	FT-75	BLK (TP)	26	16	15V	FT-69	RED	20
17	-15V	FT-71	YEL	20	18	RD 7	FT-55	WHT/YEL	26
19	RD 8	FT-56	WHT/BLK	26	20	RD 9	FT-57	WHT/BLU	26
21	RD 10	FT-58	WHT/ORG	26	22	ID 0	FT-59	WHT/BLU	26
23	ID 1	FT-60	WHT/ORG	26	24				
25	PA	FT-62	WHT/BRN	26	26	TS 5+	P1-33, 27	RED	26
27	TS 6+	P1-26	RED	26	28				
29	28V	FT-70	GRY	20	30	RD 11	FT-63	WHT/GRN	26
31	RD 12	FT-64	WHT/BRN	26	32	TS 3+	P1-33,FT-7	RED	26/22
33	TS 4+	P1-32, 26	RED	26	34	GND	FT-67	BLK	20
35					36				
37	RLYMON2	FT-73	BLK	22	38				
39					40				
41	RD 13	FT-61	WHT/GRN	22	42	GND	CHASSIS	BLK	16

PART IV REAR SHIELD PANEL, FILTER FEEDTHRU

	INTERNAL CONNECTIONS					REAR PANEL CONNECTIONS			
FT	FUNCTION	SOURCE	COLOR	GA.	FT	FUNCTION	SOURCE	COLOR	GA.
1	AV 1	W-5	WHT/BLU	26	1	AV 1	J2-A	WHT/BLU	26
2	AV 2	W-6	WHT/ORG	26	2	AV 2	J2-B	WHT/ORG	26
3	AV 3	W-7	WHT/GRN	26	3	AV 3	J2-C	WHT/GRN	26
4	AV 4	W-8	WHT/BRN	26	4	AV 4	J2-D	WHT/BRN	26
5	TS 3	W-9	WHT/GRY	26	5	TS 3	J2-E	WHT/GRY	26
6	TS 4	W-10	WHT/VIO	26	6	TS 4	J2-F	WHT/VIO	26
7	TS 5	W-11	WHT/YEL	26	7	TS 5	J2-H	WHT/YEL	26
8	TS 6	W-12	WHT/BLK	26	8	TS 6	J2-J	WHT/BLK	26
9	HTCUR+	W-13	WHT/BLU	26	9	HTCUR+	J2-K	WHT/BLU	26
10	HTCUR-	W-14	WHT/ORG	26	10	HTCUR-	J2-L	WHT/ORG	26
11	T103DET+	P1-2	WHT/GRN	26	11	T103DET+	J2-M	WHT/GRN	26
12	T103DETG	P1-19	WHT/BRN	26	12	T103DETG	J2-N	WHT/BRN	26
13	AV 11+	P1-3	WHT/GRY	26	13	AV 11+	J2-P	WHT/GRY	26
14	AV 11-	P1-20	WHT/VIO	26	14	AV 11-	J2-R	WHT/VIO	26
15	AV 12+	P1-4	WHT/YEL	26	15	AV 12+	J2-S	WHT/YEL	26
16	AV 12-	P1-21	WHT/BLK	26	16	AV 12-	J2-T	WHT/BLK	26
17	AV 13+	P1-5	WHT/BLU	26	17	AV 13+	J2-U	WHT/BLU	26
18	AV 13-	P1-22	WHT/ORG	26	18	AV 13-	J2-V	WHT/ORG	26
19	AV 14+	P1-6	WHT/GRN	26	19	AV 14+	J2-W	WHT/GRN	26
20	AV14-	P1-23	WHT/BRN	26	20	AV 14-	J2-X	WHT/BRN	26
21	15V	TB1-3	RED	22	21	TSV+	J2-Y	RED	22
22	TS 1-	W-88	WHT/VIO	26	22	TS 1-	J2-Z	WHT/VIO	26
23					23				
24	TS 2-	W-90	WHT/BLK	26	24	TS 2-	J2-b	WHT/BLK	26
25	RLYMON1	W-75	WHT/BLU	26	25	RLYMON1	J2-c	WHT/BLU	26
26	M 2	W-76	WHT/ORG	26	26	M 2	J2-d	WHT/ORG	26
27	M 3	W-77	WHT/GRN	26	27	M 3	J2-e	WHT/GRN	26
28	M 4	W-78	WHT/BRN	26	28	M 4	J2-f	WHT/BRN	26
29	M 5	W-79	WHT/GRY	26	29	M 5	J2-h	WHT/GRY	26
30	M 6	W-80	WHT/VIO	26	30	M 6	J2-j	WHT/VIO	26
31	M 7	W-81	WHT/YEL	26	31	M 7	J2-k	WHT/YEL	26
32	M 8	W-82	WHT/BLK	26	32	M 8	J2-m	WHT/BLK	26
33	M 9	W-83	WHT/BLU	26	33	M 9	J2-n	WHT/BLU	26
34	M 10	W-84	WHT/ORG	26	34	M 10	J2-p	WHT/ORG	26
35	M 11	W-85	WHT/GRN	26	35	M 11	J2-r	WHT/GRN	26
36	M 12	W-86	WHT/BRN	26	36	M 12	J2-s	WHT/BRN	26
37	C 1	W-61	WHT/GRY	26	37	C 1	J2-p	WHT/GRY	26
38	C 2	W-62	WHT/VIO	26	38	C 2	J2-u	WHT/VIO	26
39	C 3	W-63	WHT/YEL	26	39	C 3	J2-v	WHT/YEL	26
40	C 4	W-64	WHT/BLK	26	40	C 4	J2-w	WHT/BLK	26

PART V POWER DISTRIBUTION TERMINAL BLOCK

POWER SUPPLY INPUT					POWER DISTRIBUTION		
PIN	FUNCTION	SOURCE	COLOR	GA	SOURCE	COLOR	GA
TB1-1	GND	FT-67	BLK	20	P1-38, P2-17, W-1, W-99, FT-73	BLK	22
TB1-2							
TB1-3	15V	FT-69	RED	20	P1-40, P2-15, W-95, FT-21, FT-72	RED	22
TB1-4	-15V	FT-71	YEL	20	P1-39, P2-16, W-94	YEL	22
TB1-5	28V	FT-70	GRY	20	W-96	GRY	22
TB1-6							
TB1-7	5V	FT-68	ORG	20	P1-50, P2-14, W-2, W-100	ORG	22

NOTE: ADD A 100 MICROFARAD CAP WITH A 2.2 MICROFARAD CAP AND A 20K OHM, 1/4 WATT RESISTOR ACROSS EACH SUPPLY TO GROUND AT THE TERMINAL BLOCK.

Data Sheets
Selected portions

1. TL082 Texas Instruments
2. HI508A Harris Semiconductor
3. DG303A Intersil
4. AD581 Analog Devices
5. UDN2981A Sprague

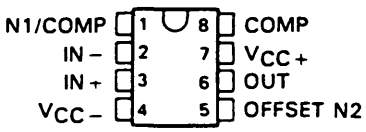
TYPES TL080 THRU TL085, TL080A THRU TL084A
TL081B, TL082B, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS

D2297, FEBRUARY 1977—REVISED SEPTEMBER 1983

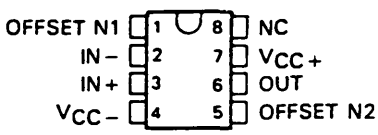
24 DEVICES COVER MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

- Low-Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% TYP
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL080, TL080A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ

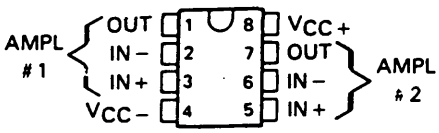
TL080, TL080A
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



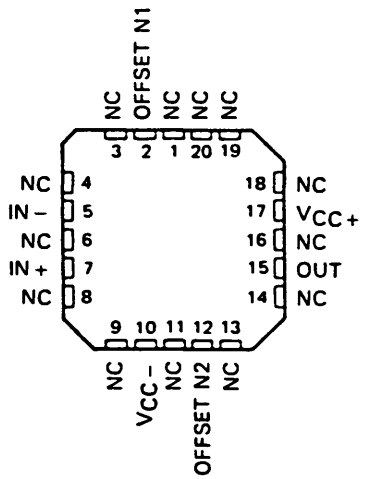
TL081, TL081A, TL081B
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



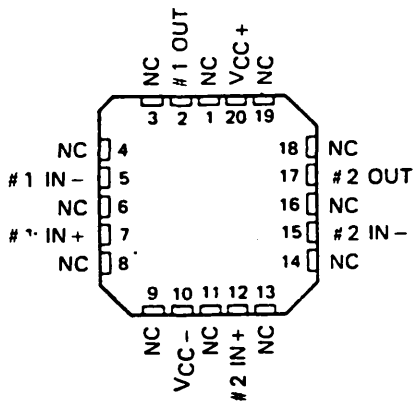
TL082, TL082A, TL082B
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



TL081M . . . FH OR FK
CHIP CARRIER PACKAGE
(TOP VIEW)



TL082M . . . FH OR FK
CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TL080	TL081	TL082	TL083	TL084	TL085
TL08_M	JG	FH, FK, JG	FH, FK, JG	FH, FK, J	FH, FK, J, W	•
TL08_I	JG, P	JG, P	JG, P	J, N	J, N	•
TL08_C	JG, P	JG, P	JG, P	J, N	J, N	N
TL08_AC	JG, P	JG, P	JG, P	J, N	J, N	•
TL08_BC	•	JG, P	JG, P	•	J, N	•

*These combinations are not defined by this data sheet.

HI-508/HI-509

Single 8/Differential 4 Channel CMOS Analog Multiplexer

FEATURES

- FAST ACCESS 220ns
- FAST SETTLING (0.01%) 600ns
- LOW R_{ON} 180 Ω
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP
- TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")

APPLICATIONS

- PRECISION INSTRUMENTS
- DATA ACQUISITION SYSTEMS
- TELEMETRY

DESCRIPTION

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so that two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and Maximum 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

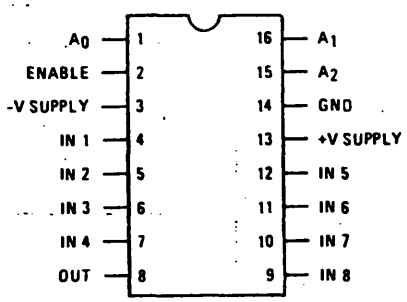
The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. The recommended supply voltage is ± 15V; however, reasonable performance is available down to ± 7V. Each device is packaged in a 16 pin DIP.

The HI-508/509 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For further information see Application Notes 520 and 521.

PINOUTS

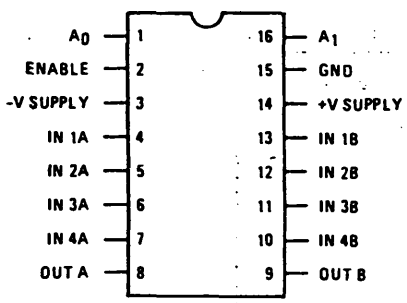
HI-508

TOP VIEW



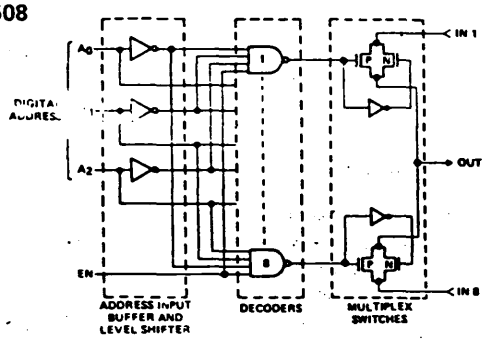
HI-509

TOP VIEW

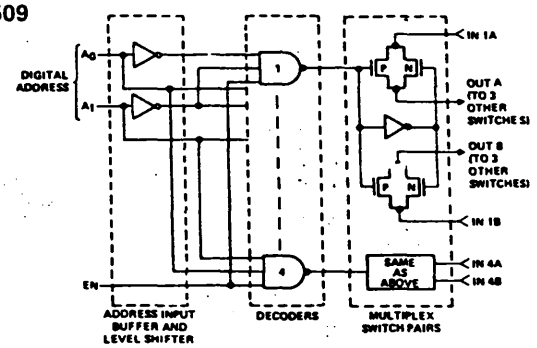


FUNCTIONAL DIAGRAMS

HI-508



HI-509



DG300A/DG301A/ DG302A/DG303A
TTL Compatible CMOS Analog Switches

INTERSIL

GENERAL DESCRIPTION

The DG300A–303A family of monolithic CMOS switches are a truly compatible second source of the original manufacturer. The switches are latch-proof and are designed to block signals up to 30 volts peak-to-peak when OFF. Featuring low leakage and low power consumption, these switches are ideally suited for precision application in instrumentation, communication, data acquisition and battery-powered applications. Other key features include Break-Before-Make switching, TTL and CMOS compatibility, and low ON resistance. Single supply operation (for positive switch voltages) is possible by connecting V^- to 0 volts.

The DG300A–DG303A family is available over commercial, industrial, and military temperature range.

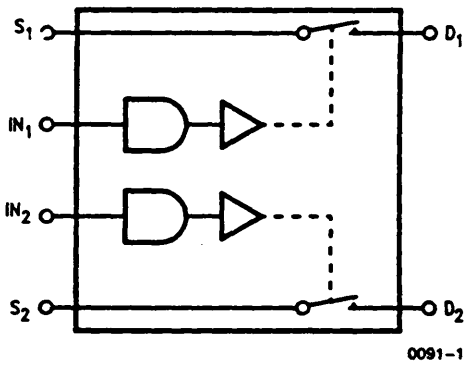
FEATURES

- **Low Power Consumption**
- **Break-Before-Make Switching t_{off} 130 ns, t_{on} 150 ns Typical**
- **TTL, CMOS Compatible**
- **Low $R_{DS(on)}$ ($\leq 50\Omega$)**
- **Single Supply Operation**
- **True Second Source**

ORDERING INFORMATION

Part Number	Temperature Range	Package
DG300A/301A/ 302A/303AAK	−55°C to +125°C	14-Pin CERDIP
DG300A/301A/ 302A/303ABK	−25°C to +85°C	14-Pin CERDIP
DG300A/301A/ 302A/303ACK	0°C to +70°C	14-Pin CERDIP
DG300A/301A/ 302A/303ACJ	0°C to +70°C	14-Pin Plastic DIP
DG300A/301AAA	−55°C to +125°C	10-Pin Metal Can
DG300A/301ABA	−25°C to +85°C	10-Pin Metal Can
DG300A/301ACA	0°C to +70°C	10-Pin Metal Can

DG300A



Two SPST Switches per Package*

Truth Table

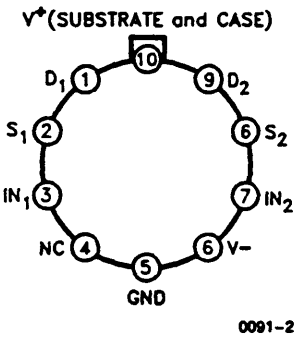
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8V
Logic "1" ≥ 4.0V

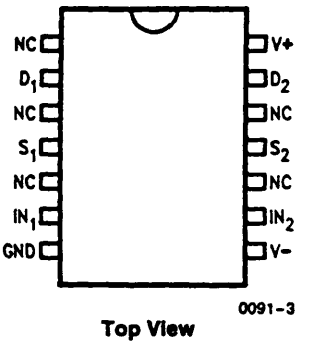
*Switches Shown for Logic "1" Input

Figure 1: Functional Diagrams

Metal Can Package



Dual-In-Line Package



Top View

Figure 2: Pin Configurations

307025-001

NOTE: All typical values have been characterized but are not tested.

ANALOG DEVICES

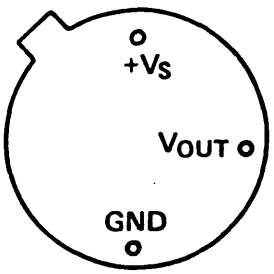
High Precision 10V IC Reference

AD581*

FEATURES

- Laser-Trimmed to High Accuracy:
  - 10.000 Volts ±5mV (L and U)
- Trimmed Temperature Coefficient:
  - 5ppm/°C max, 0 to +70°C (L)
  - 10ppm/°C max, -55°C to +125°C (U)
- Excellent Long-Term Stability:
  - 25ppm/1000 hrs. (Noncumulative)
- Negative 10 Volt Reference Capability
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability
- 3-Terminal TO-5 Package

AD581 FUNCTIONAL BLOCK DIAGRAM



TO-5
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical Zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected Zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C; the AD581S, T, and U are specified for the -55°C to +125°C range. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

*Covered by Patent Nos. 3,887,863; RE 30,586

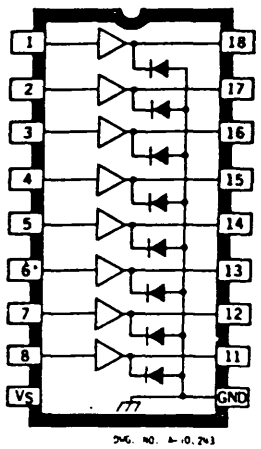
PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from -55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 13 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.

SERIES UDN-2980A
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- Output Breakdown Voltage to 80 V



RECOMMENDED for applications requiring separate logic and load grounds, load supply voltage to +80 V, and load currents to 500 mA, Series UDN-2980A source drivers are used as interfaces between standard low-power digital logic and relays, solenoids, stepping motors, and LEDs.

Under normal operating conditions, these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of +15 V. All devices in this series incorporate input current limiting resistors and output transient suppression diodes.

Type UDN-2981A and UDN-2983A drivers are for use with +5 V logic systems — TTL, Schottky TTL, DTL, and 5 V CMOS. Type UDN-2982A and UDN-2984A drivers are intended for MOS interface (PMOS and CMOS) operating from supply voltages of 6 to 16 V. Types UDN-2981A and UDN-2982A will sustain a maximum output OFF voltage of +50 V, while Types UDN-2983A and UDN-2984A will sustain an output voltage of +80 V. In all cases, the output is switched ON by an active high input level.

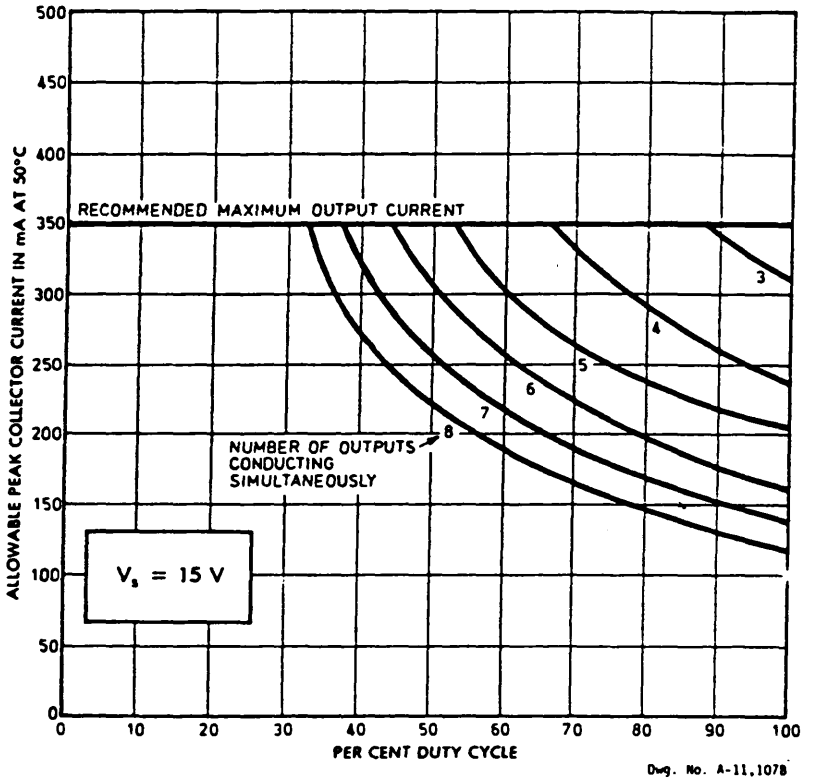
Series UDN-2980A high-voltage, high-current source drivers are supplied in 18-lead dual in-line packages. On special order, hermetically-sealed versions of these devices (with reduced package power dissipation capability) can also be furnished.

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

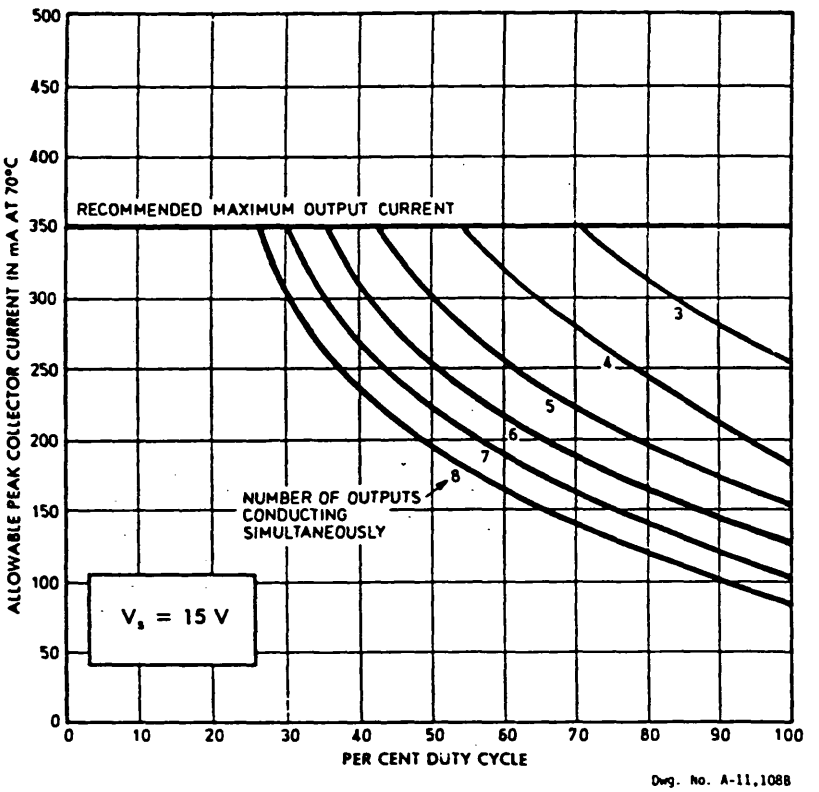
Output Voltage Range, V_{CE} (UDN-2981A & UDN-2982A)	+5 V to +50 V
(UDN-2983A & UDN-2984A)	+35 V to +80 V
Input Voltage, V_{IN} (UDN-2981A & UDN-2983A)	+15 V
(UDN-2982A & UDN-2984A)	+30 V
Output Current, I_{OUT}	−500 mA
Power Dissipation, P_D (any one driver)	1.1 W
(total package)	2.2 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 18 mW/°C above +25°C.

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE TYPE UDN-2981A/82A



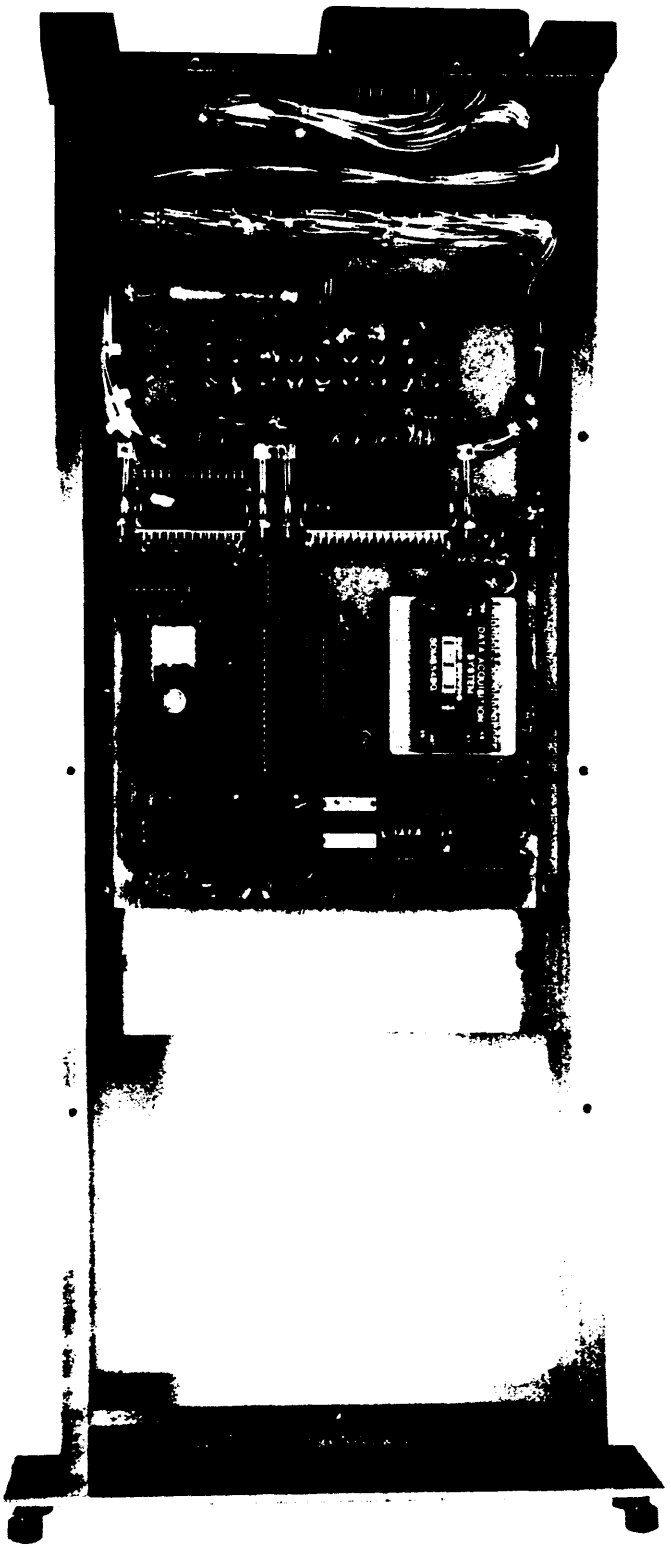
Dwg. No. A-11,107B

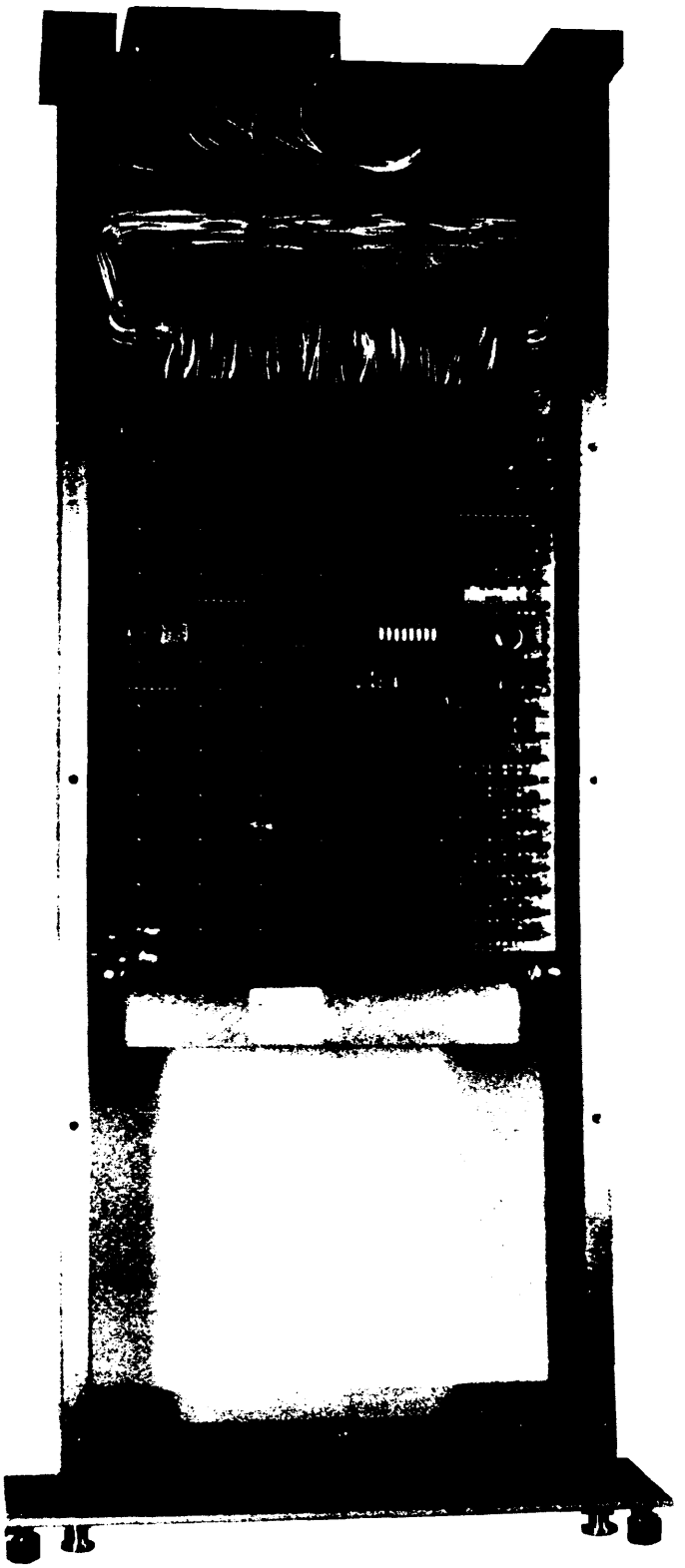


Dwg. No. A-11,108B

Addendum

Module Photograph
Selected Drawings





REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

REAR PANEL

FILTER PANEL

J1

1	RD 1
2	RD 2
3	RD 3
4	RD 4
5	
6	
7	
8	XMIT+
9	XMIT-
10	5V
11	
12	RD 5
13	RD 6
14	RCV+
15	RCV-
16	15V
17	-15V
18	RD 7
19	RD 8
20	RD 9
21	RD 10
22	RD 0
23	RD 1
24	
25	PA
26	VS1 5+
27	VS2 5+
28	
29	28V
30	RD 11
31	RD 12
32	VS1 4+
33	VS2 4+
34	GND
35	
36	
37	RLYMON2
38	
39	
40	
41	RD 13
42	GND

J2

A	AV 1
B	AV 2
C	AV 3
D	AV 4
E	TS 3
F	TS 4
H	TS 5
J	TS 6
K	HTCUR+
L	HTCUR-
M	T103DET+
N	T103DETG
P	AV 11+
R	AV 11-
S	AV 12+
T	AV 12-
U	AV 13+
V	AV 13-
W	AV 14+
X	AV 14-
Y	TS 1+
Z	TS 1-
a	TS 2+
b	TS 2-
c	RLYMON1
d	M 2
e	M 3
f	M 4
h	M 5
j	M 6
k	M 7
m	M 8
n	M 9
p	M 10
r	M 11
s	M 12
t	C 1
u	C 2
v	C 3
w	C 4
x	C 5
y	C 6
z	C 7
AA	C 8
BB	C 9
CC	C 10
DD	C 11
EE	C 12
FF	
HH	

FT-1 FT-2 FT-3 FT-4 FT-5 FT-6 FT-7 FT-8 FT-9 FT-10 FT-11 FT-12 FT-13 FT-14 FT-15 FT-16 FT-17 FT-18 FT-19 FT-20 FT-21 FT-22 FT-23 FT-24 FT-25 FT-26 FT-27 FT-28 FT-29 FT-30 FT-31 FT-32 FT-33 FT-34 FT-35 FT-36 FT-37 FT-38 FT-39 FT-40 FT-41 FT-42 FT-43 FT-44 FT-45 FT-46 FT-47 FT-48 FT-49 FT-50 FT-51 FT-52 FT-53 FT-54 FT-55 FT-56 FT-57 FT-58 FT-59 FT-60 FT-61 FT62 FT-63 FT-64 FT-65 FT-66 FT-67 FT-68 FT-69 FT-70 FT-71 FT-72 FT-73 FT-74 FT-75 FT-76

NRAO DRAWING # D55002S002
STANDARD INTERFACE BOARD

J2: +5V, ID_READ, 5V, 12V, -12V, GND, RCV+, RCV-, XMIT+, XMIT-, GND

J1: ANG.1+, T103DET+, AV 11+, AV 12+, AV 13+, AV 14+, TS1 OUT, TS2 OUT, C/N 15, C/N 13, C/N 11, C/N 9, C/N 7, C/N 5, C/N 3, C/N 1, M-LOSEL, ANG.1-, T103DETG, AV 11-, AV 12-, AV 13-, AV 14-, TS_RET, C/N 14, C/N 12, C/N 10, C/N 8, C/N 6, C/N 4, C/N 2, C/N 0, GND, DEV REQ, DEV ACK, ANSENB, GND, -12V, 12V, ADDR 5, ADDR 4, ADDR 3, ADDR 2, ADDR 1, ADDR 0, R/W, 5V

NRAO DRAWING #C5351DSDD2
WIRE WRAP BOARD

GND 5V GND 5V AV1 AV2 AV3 AV4 TS3 TS4 TS5 TS6 HTCUR+ HTCUR- C/N 0 C/N 1 C/N 2 C/N 3 C/N 4 C/N 5 C/N 6 C/N 7 C/N 8 C/N 9 C/N 10 C/N 11 GND TS_RET C/N 12 C/N 13 C/N 14 C/N 15 ANG.1+ ANG.1- ADDR 0 ADDR 1 ADDR 2 ADDR 3 ADDR 4 ADDR 5 DEV REQ DEV ACK ID_READ ANSENB M-LOSEL RD 1 RD 2 GND RD 3 RD 4 RD 5 RD 6 RD 7 RD 8 RD 9 RD 10 RD 11 RD 12 C 1 C 2 C 3 C 4 C 5 C 6 C 7 C 8 C 9 C 10 C 11 C 12 GND PA RLYMON1 M 2 M 3 M 4 M 5 M 6 M 7 M 8 M 9 M 10 M 11 M 12 TS1 OUT TS 1- TS 1+ -12V 12V 28V GND 5V GND 5V

TB 1: 1 GND, 2 5V, 3 15V, 4 -15V, 5 28V, 6 5V, 7

100 uF, .00022uF

NOTE: CAPACITOR COMBINATION CONNECTED ACROSS EACH POWER SUPPLY AT TB1

ACAD : 53510W12

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLBA PROJECT : M102 MODULE

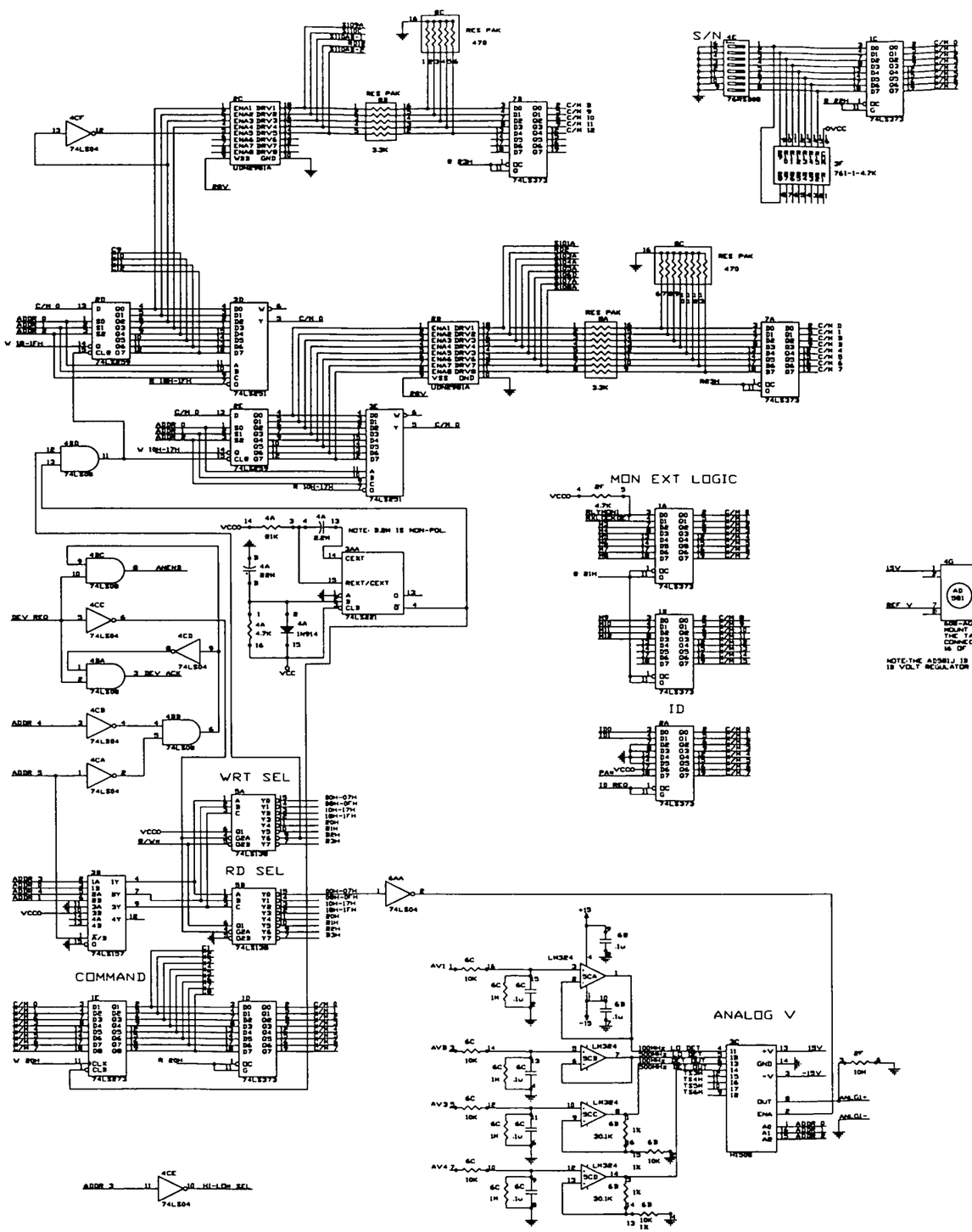
TITLE : M102 B-RACK INTERFACE MODULE WIRING DIAGRAM

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C53510W012 | REV. – | SCALE NONE

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY J. OTY	DATE 1-96
DESIGNED BY J. OTY	DATE 1-96
APPROVED BY J. OTY	DATE 1-96

REV.	DATE	DRAWN BY	APROV'D BY	DESCRIPTION
F	1-93	K. TATE		UPDATES TO NRAO STANDARDS
G	8-93	K. TATE	J. DIY	GENERAL REVISIONS
H	1-96	W.ZAMORA	W.ZAMORA	REVISED AND REDRAWN



ORCAD : 53510S02

C53518V003	WIRE LIST
A535188004	BOM
D53510A003	ASSEMBLY
NEXT ASSEMBLY	DVO TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
2 PLACE DECIMALS(.XX) ±
3 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:

FINISH:

PROJECT: FRONT END INTERFACE

TITLE: M102 MODULE RACK B INTERFACE SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
EDGEWOOD,NEW MEXICO 87801

DRAWN BY	W.WISEMAN	7-96
DESIGNED BY		DATE
APPROVED BY		DATE

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D53510S02 | REV H | SCALE -

REV	DATE	DRAWN BY	APPRVD BY	DESCRIPTION
C	1-91	ANDREATTA		REDRAWN WITH ACAD ;

CPU ADDRESS/DATA BUS

CONTROL/MONITOR LINE BUFFERS

U1 INTEL P8032AH uCONT — CONTROL PROCESSOR

U2 INTEL D8755A-2 — EPROM PROGRAM MEMORY

U5 INTEL P8156H-2 — RAM-I/O

U8 75174 DIFF DRIVER

U9 75175 DIFF RECEIVER

U10 74LS245

U11 74LS245

U12A 96LS02

U3 74LS173

U7A 74LS221

U7B 74LS221

U13 LS04

U14 LS04

U15 LS00

U16 LS04

U17 LS10

U18 LS04

U19 LS04

P1 PARALLEL I/O

P2 SERIAL I/O

RELATIVE ADDR TO ADDR BUS DRIVER U4 (SHT 2)

12 BIT ANALOG CONV. FROM U14 (SHT 2)

INSTALL HAND WIRE LINK TO P1.7 OR DESIRED SIGNAL

EXTERNAL INDICATOR DRIVER

ACTIVITY INDICATORS (EXTERNAL)

RESET LINK

R to B - FOR SYSTEM RESET INPUT (P2-34)
R to G - FOR EXTERNAL RESET INPUT (P2-23)

WARNING :
CPU U1 WILL NOT RUN IF LINK "R" IS LEFT FLOATING. IT MUST BE TERMINATED TO LINK "G" OR "B".

NOTES :

1. ALL IC's ARE 'LS' LOGIC UNLESS OTHERWISE INDICATED.
2. USE EXACT PART NUMBERS ONLY ON U1, U2, AND U5. DO NOT SUBSTITUTE.
3. BYPASS CAPACITORS (.01 'Cx' ON ASSEMBLY DWG.) NOT SHOWN.
4. ✕ = NOT USED.
5. ALL RESISTOR VALUES ARE IN OHMS.

ACAD : SIBDSK-1

CPU, MEMORY, AND I/O DRIVERS

A55002B002	BOM
D55002A002	ASSEMBLY
D55002P002	DRILL DWG.
D55002Q002	ARTWORK
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

VLBA PROJECT : STANDARD INTERFACE BOARD

TITLE : STANDARD INTERFACE BOARD MODEL "D" SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY HARDEN	DATE 12-85
DESIGNED BY WEBER	DATE 5-84
APPROVED BY	DATE

SHEET NUMBER 1 of 2 | DRAWING NUMBER D55002S002 | REV. C | SCALE —

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
C	1-91	ANDREATTA		REDRAWN WITH ACAD

PARALLEL I/O P1

+5V — 50 — +5V DISTR
5V COMM — 34 — DIGITAL GND
+15V — 40 — +15V DISTR
HIQ GND — 38 — ANALOG GND
-15V — 39 — -15V DISTR
DEV ACK — 36 — DEVICE ACKNOWLEDGE
ANENB — 37 — ANALOG ENABLE

R/W U16-12 (SHT 1)
IOR U2-39 (SHT 1)
PU1
U13 74LS74
U16 LS04
LS10 U17
LS00 U15
U12A 96LS02
STRB/ACK
TO U1-12 CPU INTR-0 (SHT 1)

H = D0-D11 IS IN HI-Z STATE
L = D0-D11 DUMPED ON BUS

SERIAL I/O P2

+5V DISTR — 1, 14 — +5V
DIGITAL GND — 13, 25 — LOGIC COMM
+15V DISTR — 15 — +15V
ANALOG GND — 17 — ±15V COMM
-15V DISTR — 16 — -15V

EXTERNAL ACCESSORY DC POWER AVAILABLE FOR TEST AND ALIGNMENT PURPOSES

DIFFERENTIAL ANALOG INPUTS

ANLG-0 H 1 / L 18 — CH1+ / CH1-
ANLG-1 H 2 / L 19 — CH2+ / CH2-
ANLG-2 H 3 / L 20 — CH3+ / CH3-
ANLG-3 H 4 / L 21 — CH4+ / CH4-
ANLG-4 H 5 / L 22 — CH5+ / CH5-
ANLG-5 H 6 / L 23 — CH6+ / CH6-
ANLG-6 H 7 / L 24 — CH7+ / CH7-
ANLG-7 H 8 / L 25 — CH8+ / CH8-

S/H CONT — BUSY — STRB — EN1 EN2 EN3 — DI1 EN — SHORT CYCLE — +5V — -15V — ANALOG COMM — +15V

BUSY = CONVERSION IN PROGRESS

OUTPUT D0-D11

D0 — CON/MON-4 (LSB)
D1 — CON/MON-5
D2 — CON/MON-6
D3 — CON/MON-7
D4 — CON/MON-8
D5 — CON/MON-9
D6 — CON/MON-10
D7 — CON/MON-11
D8 — CON/MON-12
D9 — CON/MON-13
D10 — CON/MON-14
D11 — CON/MON-15 (MSB)

CON/MON BUS (12-BIT ANALOG CONVERSION) TO P1 (SHT 1)

MUX EN1
MUX EN2
CLR — +5V
S/H OFFSET — RV3 1K — FINE OFFSET ADJ

U14
SDM854BG (BURR-BROWN)
ANALOG DATA ACQUISITION SYSTEM

CONFIGURED FOR

8-CHAN DIFFERENTIAL INPUTS
BIPOLAR OPERATION (±10V RANGE)
12-BIT RESOLUTION (4.8828 mV/BIT)
2's COMPLIMENT OUTPUT CODING
OUTPUT IS ONE 12-BIT WORD, HI-Z DRIVERS

A0 A1 A2 A3 — DIG GND — LOAD — DLY OUT — TRIG — DLY ADJ — BPO — 2.5V REF OUT — IN — MUX OUT — 20V RANGE — S/H OUT — S/H IN

RV2 50 ZERO — RV1 100 GAIN — C11 .01 µF — R10 249 — RG1 RG2 — NC — OFFSET

FOR 4.8828 mV/bit INSTALL JUMPER IN LIEU OF R10
FOR 5.0 mV/bit INSTALL 240 OHM VV RESISTOR PER BURR-BROWN SPECS

HI/LO SEL — 17 — R7 470 — U6 74LS157 — SEL — 1Y 2Y 3Y 4Y — 1A 1B 2A 2B 3A 3B 4A 4B — ADDR-0 ADDR-3 ADDR-1 ADDR-4 ADDR-2 ADDR-5

LOAD REG — TRIG A/D

U19 BURR-BROWN INA101CM INSTR. AMPL.
U19 PIN OUT (TOP VIEW)

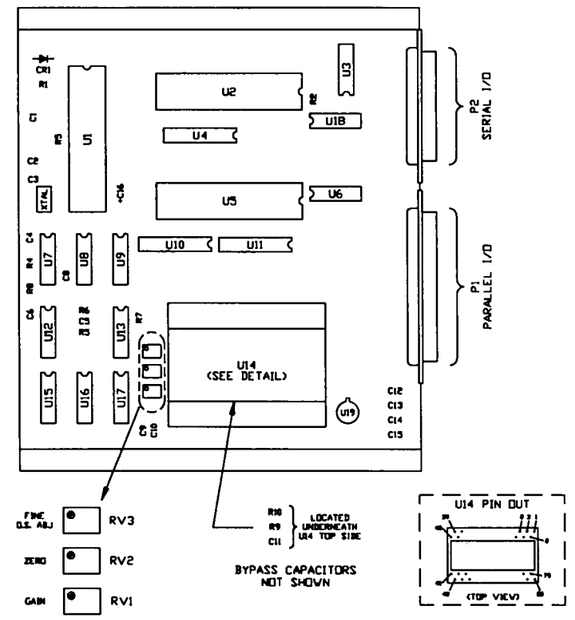
-15V +15V

FROM U2 (SHT 1) — PU2 — U4 74LS245 ADDR BUS DRIVER — RA0-RA7 — A0-A7 — B0-B7 — ADDR-0 ADDR-1 ADDR-2 ADDR-3 ADDR-4 ADDR-5 ADDR-6 ADDR-7 — DIR

ADDRESS BUS

PARELLEL I/O P1

ADDR-0 — 48 — RA-0
ADDR-1 — 47 — RA-1
ADDR-2 — 46 — RA-2
ADDR-3 — 45 — RA-3
ADDR-4 — 44 — RA-4
ADDR-5 — 43 — RA-5
ADDR-6 — 42 — RA-6
ADDR-7 — 41 — RA-7



ANALOG CIRCUITRY

A55002B002	BOM
D55002A002	ASSEMBLY
D55002P002	DRILL DWG.
D55002Q002	ARTWORK
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
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ACAD : SIBDSK-2