TECHNICAL REPORT NO. 23

ROUND-TRIP PHASE MEASUREMENT MODULE L103

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Table of Contents

I. General Description.

The primary function of the Round-Trip Phase (L103) Module is to measure the relative changes in the length of the 500 MHz LO cable going from the station building up to the antenna. It is important to keep track of this length because of its effect on the phase of the LO signals and hence of the received signals from the antenna. Changes in the cable length are measured by reflecting some of the 500 MHz LO signal back from the antenna with sidebands 1.953 kHz away (i.e. 500 MHz ± 1.953 kHz). This is then mixed with a reference signal of 500 MHz + 2.083 kHz in the LO transmitter in the station building. The result of this mixing process is a signal of 130.2 Hz*. The round-trip phase module (L103) then compares the phase of this signal with that of another internally generated reference at the same frequency. Any change in the phase of the returning 500.001953 MHz signal will show the same phase change in the 130.2 Hz signal.

II. Circuit Description.

The Round-Trip Monitor internally generates two reference signals whose frequency is 130.2 Hz, but which have a 90 degree phase difference between them. The phase of the two reference signals is compared with that of the incoming 130.2 Hz signal from the LO Transmitter. This is done using two counter chains which are gated by the output of two exclusive-or (XOR) gates. Each of these two gates compares the incoming signal with each of the two reference signals and produces a logical low when the reference and input signals are in the same logical state.

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* precisely 5×10^6 / 38400 Hz. This will be referred to as the 130.2 Hz

Thus, if the signals are in phase, the XOR output is low and if they are 180 degrees out of phase, the output is high. If the phase difference is increased from 0 to 180 degrees, the output duty cycle increases in proportion. Conversely, if the difference is increased from 180 to 360 degrees, the duty cycle decreases. This means that there is an ambiguity in the phase measurement: a difference of 170 degrees would read the same as one of 190 degrees, and differences of 10 and 350 would also read the same.

This ambiguity is not a problem by itself, since only the relative phase change over time is important, and the total phase drift will not be greater than 180 degrees. However, if the phase difference using one reference is near 0 or 180 degrees, this ambiguity would make the measurement unusable if the phase difference drifted through the 180 or 0 degree points. Hence, if the measurement using one reference is near 0 or 180 degrees, the phase measurement software will choose the other measurement which will be 90 degrees away from the ambiguous points.

Referring to the schematic diagram, IC's 5A through 5F form the 24-bit counter for the 90 degree reference, and 4A through 4F comprise the 0 degree reference counter. Gate 1B, pin 3 (1B3) is the XOR for the 90° reference, and 1B6 is for the 0° XOR. These outputs are connected to AND gates and then on to the ENABLE inputs of the counters in the chains. The AND gates allow the counters to be turned off once every three seconds for latching and resetting, as discussed below. IC's 2A through 2C and 3A through 3C are the latches for the counter chains.

The circuitry on the left of the diagram is used to derive the 1.953 and 2.083 kHz references mentioned in the General Description above. It is also used

to latch the counter outputs and reset all of the counters and references once every three seconds, in case something gets hung up on a supply glitch. Starting at the upper left corner, the first four IC's going down are synchronous counters (as are all the others) which count down the 5 MHz clock 'CK' signal. This signal, which derives from the MASER reference comes into the module as a sine wave. It is squared, and a complementary version, CK* is produced by the comparator, 1D. IC 1C is a buffer. The first counter in the chain, 7A divides the 5 MHz by 5. The next divides by 16 to produce a 62,500 Hz signal at 7B15. IC 7C further divides by 16 to give a 3906.25 Hz signal at 7C15 which is then divided by 2 to produce 1953.125 Hz at 6E3 which is buffered by 1G11 to go out of the module.

The 62,500 Hz signal is divided by 15 in IC 7D, resulting in 4166.667 Hz at 7D15 which is further divided by the flip/flop at 6E to give the 2083.333 Hz reference at 6E5 which is also buffered for output from the module. 6F3 gives a ripple carry out (CO) type of signal suitable for the next counters. This signal then goes to the two counters 6A and 6B which divide it by sixteen to give the 130.208333 Hz signals. IC 6A is the 90° counter. It is initially loaded with a 12, rather than cleared to 0 when the CLR2 signal is delivered once per three seconds. Hence, its output - 6A11 is 90 degrees behind the 0° output 6B11. The outputs then go to the XOR gates as described above. Additionally, 6B11 goes to a buffer, 1G3 to be brought to the LO Transmitter module for the test purpose mentioned above. This buffer is turned off (into the high-impedance state) whenever the 'signal', rather than the 'test' mode is selected. This is so that the reference will not interfere with the signal in the Transmitter. Further, the 130 Hz output from 6B11 is brought to the front panel for testing purposes.

All of this circuitry is synchronized once in three seconds to the 1 PPS (pulse-per-second) signal from the Station Timing Module (L108). Flip/flop circuits 10AA and 10AB divides the 1PPS signal by a factor of three. The negative-going, 1 microsecond long pulse is inverted by 8D1 and fed to the flip/flops 7F6 and 7E3. All of these flip/flops are negative-edge triggered. The 1PPS signal transitions on the negative edge of the clock. Since 7E3 is clocked by the inverted clock, CK*, it flips one half cycle, or 100 ns, later (see the timing diagram, Figure 1). The negative output of the flip/flop 7E2, the GATE signal, goes to AND gates 6F6 and 6F11 to gate off the counting signal from the XOR's. Simultaneously, the positive flip/flop output 7E3 causes the latches 2A - 2C and 3A - 3C to capture the current counts. These outputs also set up flip/flop 7E6 to transition one half cycle later, ie. one full cycle after receiving the 1PPS. This serves to reset flip/flop 7F5 on the next positive clock transition, one cycle later. Flip/flop 7F5 is set up by the 1PPS and transitions on the first positive-going clock, one cycle later. Since 7E6 has set 7F5 up at the same time to transition back (reset), it does so after one more cycle. Thus 7F6 gives a one-cycle-long clear signal starting a half cycle after the current count has been latched. This clear signal, CLR1, CLR2, and CLR*, clears both the reference chain (6A - 6C, 6E, 7A - 7D) and the main counting chains.

Meanwhile, the gate/latch signal which halts the counting must be reset to restart counting. This is done by IC 6C which counts 8 counts of the 130 Hz output from 6B. This waiting period is required to let the transients due to the change in phase of the 2.083 KHz and 1.953 KHz signals die out. They die out slowly, because the signal is fed through a 200 Hz filter in the LO Transmitter module. Thus, long after 8D1 and 7E1 have gone low, 6C15 and 7E4 go high for one

cycle, which sets up 7E to reset to 7E2 high and 7E3 low. Once 7E2 is high again, counting restarts and continues until the next integration cycle.

The IC's depicted on the right side of the schematic comprise the interface to the M/C standard interface board. IC's 8A, 8B, and 10B along with 9A, 9B, and 8C decode the address lines and the handshaking DEV REQ and R/W*. IC 8C activates DEV ACK for most of the addresses which are digital. Addresses 06 and 10 to 17 activates ANENB for the analog monitor. IC 8A decodes 'read' requests, and 8B decodes the lone 'write' request. 2D latches the write, and 3D latches and buffers its corresponding read. Only one bit is currently used, but up to 8 are available in the hardware. 9C allows 8 single bit reads from 8 contiguous addresses. Again, only one is used at this time. 3E allows the module serial number to be read, and 2E reads the module ID for initialization, as described in the Standard interface specification.

Power supplies in the C Rack are monitored via this module. +15V is divided by 2 on header 10C and read via address 11. -15 V is divided by 2 on header 10C and read via address 12. +5V is read via address 13. Address 10 reads a ground voltage. In addition, three analog voltages may be input to the module via P11. They are read via addresses 14, 15, and 17.

Related Documents

1. Specification of Monitor and Control Standard Interface, A55001N002-A, L. R. D'Addario, November, 1985.
2. Specification of Monitor and Control Bus at VLBA Stations, A55001N001, B. G. Clark, December 1984.

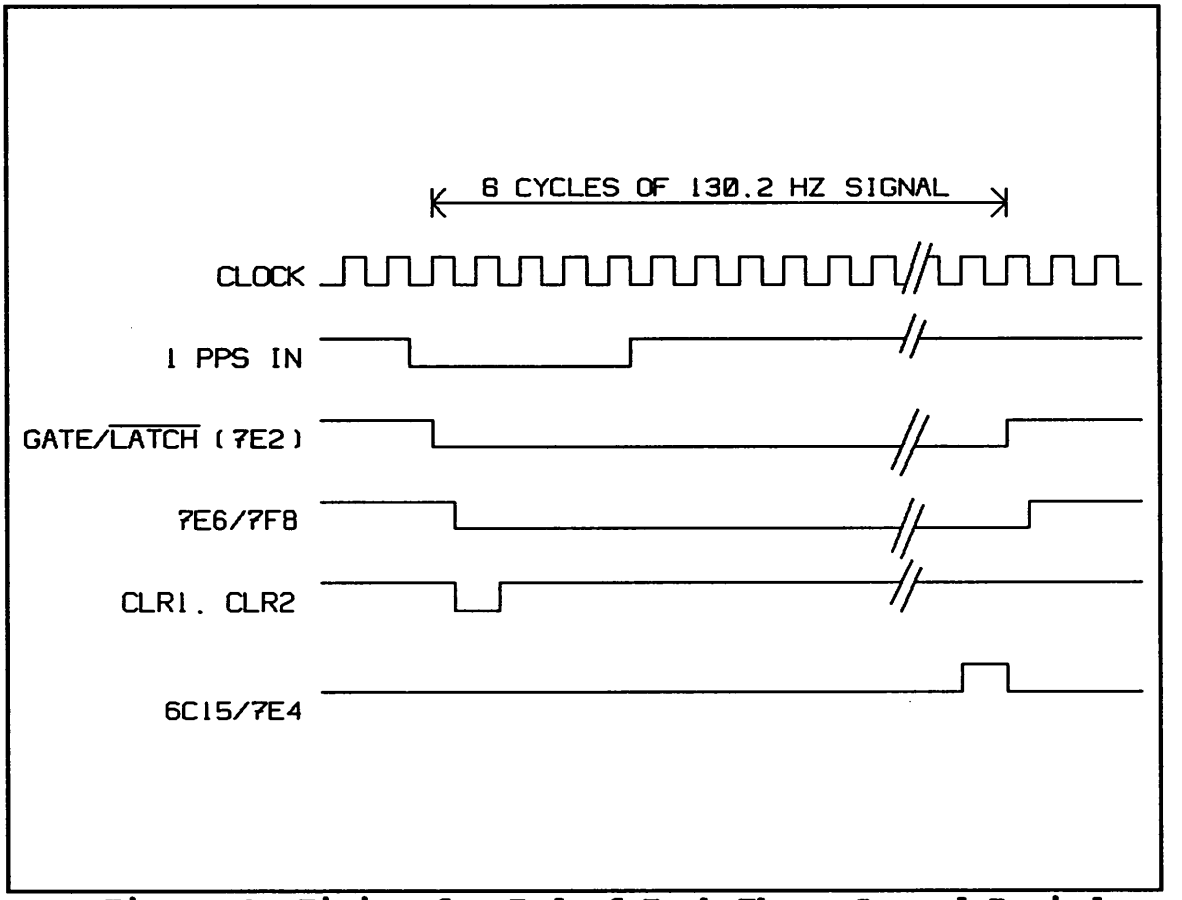


Figure 1. Timing for End of Each Three-Second Period.

III. Round Trip Monitor Test Procedure

The module is tested for its performance initially on the bench. The two clock signals 5 MHz and 1 PPS are derived from a test unit specially designed for testing this module. Powering up the module on the bench and applying the above clock signals, the logical functioning of the various blocks in the module are tested. The output signals 2.083 KHz and 1.953 KHz are monitored at the wirewrap board connector for proper functioning of the divider chain formed by the ICs 7A to 7D and 6EB. Similarly the 130 Hz REF signal is monitored for checking the divider IC 6B. 0 and 90 degree gating circuits and counter chains are tested by giving 130 Hz signal externally to the 130 Hz signal port of the module. There is a facility in the test unit to apply the internally generated 130 Hz REF signal directly for this purpose. This signal will check 0 degree EXOR circuitry and the corresponding counter chain. A switch is provided in the test unit to invert the 130 HZ REF signal, which will test the 90 degree EXOR circuit and the counter chain associated with it.

Standard interface circuitry can be tested after connecting the module to the computer and using the Round Trip test software routine in the MONCON program. Various monitor and command functions are tested. The module ID circuit is also tested.

After the module is tested satisfactorily on the bench, the round trip phase of the LO cable can be measured by placing the module in Rack C. The LO transmitter module L102 in Rack B and the LO Receiver module L105 in Rack C are connected by a cable through a 50-ohm line stretcher (General Radio Constant Impedence Trombone Line Type 874- LTL). The Round trip phase test software in

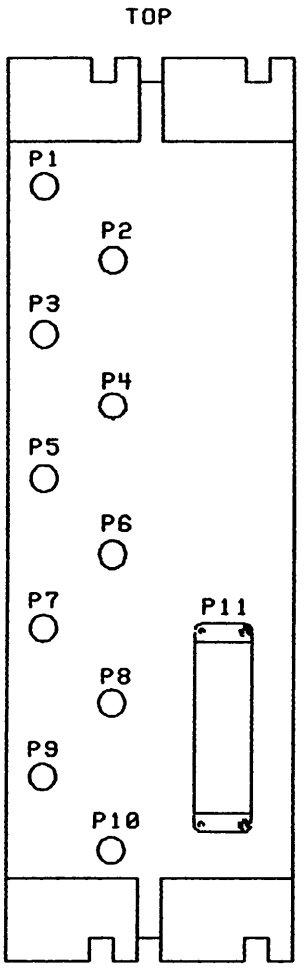
MONCON gives the phase in degrees and also gives the cable length in cms. The line stretcher has the facility to change the tube length by a small amount and the Round Trip module can be checked for proper functioning.

Specifications

Maximum Voltage to Analog Inputs	± 20 VOLT
Analog Voltage Measurement Range	± 10 VOLT
Number of analog inputs	4
Number of internal analog measurements	4
Number of digital inputs	1
Number of digital readbacks	1
Number of digital command outputs	1
Module Serial Number relative address	04 hexadecimal
Address ID code	15 hexadecimal
Analog monitor relative address	06, 10 thru 17
Digital monitor relative address range	00-05, 08
Command relative address range	05 hexadecimal
Power supply voltages required	+ 5, ±15 VOLT

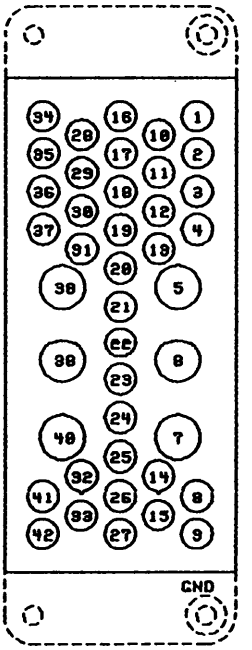
Drawing List

Description	Number
Assembly Drawing	D53304A010
Wire-wrap Board Layout Drawing	A53304A011
Bill of Materials	A53304B010
Front Panel Silkscreen Artwork	B53304I003
Schematic Diagram	D53304S003
Wiring Harness Diagram	A53304W002
Wire List	A53304W001



MODULE
(REAR VIEW)

SIMI-RIGID CABLE	
P1	
P2	
P3	
P4	
P5	
P6	
P7	
P8	
P9	1.953 kHz OUT TTL
P10	2.083 kHz OUT TTL



P11
(REAR VIEW)

P11 (42-PIN REAR)					
PIN	FUNCTION	COMMENT	PIN	FUNCTION	COMMENT
1			22	ANALOG7 +	
2			23	ANALOG7 -	
3			24		
4			25	130Hz SIG/TST SW	TTL
5	2.083 kHz OUT	TTL (50 ohm)	26	100MHz DETECT IN	
6			27		
7	5 MHz IN	0.05 TO 5V Pk	28		
8	XMIT +		29		
9	XMIT -		30		
10	+5V SUPPLY	1400 mA	31		
11			32		
12			33		
13			34	GRND	
14	RCV +		35		
15	RCV -		36		
16	+15V SUPPLY	10 mA	37		
17	-15V SUPPLY	40 mA	38	130Hz OUT	TTL
18	ANALOG4 +		39	1PPS IN (NEG)	TTL
19	ANALOG4 -		40	130Hz IN	TTL
20	ANALOG5 +		41	XMTR LOCK DET	TTL
21	ANALOG5 -		42		

(DC L109RPWL)

ROUND-TRIP PHASE MONITOR (L103)
[ID No. 15_{16}]

CONTROL

Relative address (hex): 05
Function: 130.2 Hz Signal/Reference Test Switch

COMMAND:	0	1
POSITION:	SIG (NORMAL)	REF (TEST)

MONITOR

Relative Address	Normal BITS	Type	Function	Value
00	0-15	DIGITAL	0° Phase Bits 0-15	--
01	0- 7	DIGITAL	0° Phase Bits 16-23	--
02	0-15	DIGITAL	-90° Phase Bits 0-15	--
03	0- 7	DIGITAL	-90° Phase Bits 16-23	--
04	0- 7	DIGITAL	Module SERIAL NUMBER	1 - 255
05	0	DIGITAL	SIG/REF Switch Readback	0 (SIG)
06	--	ANALOG	LO Transmitter Detector Voltage	1.0 Volt
08	1	DIGITAL	LO Transmitter Lock Detect	0 (LOCKED)
10	--		Ground Voltage	0.0 Volt
11	--		+15V/2	7.5 Volt
12	--		-15V/2	-7.5 Volt
13	--		+5 V	+5.0 Volt
14	--		External Analog 4	±10 Volt
15	--		External Analog 5	±10 Volt
16	--	ANALOG	LO Transmitter Detector Voltage	1.0 Volt
17	--		External Analog 7	±10 Volt

Address Map

RA (Hex)	Contents/Function	Note
00	0° Least Sig Word	16 Bits
01	0° Most Sig Word	8 Bits CM7 - CMO
02	90° Least Sig Word	16 Bits
03	90° Most Sig Word	8 Bits CM7-CMO
04	Serial Number	8 Bit Binary CM7-CMO
05	Test Switch Control	Control & Monitor CMO 0=Signal 1=Test
06	100 MHz det Level	Analog Voltage
07	Not Used	-----
08	Lock Detector	Monitor CMO 0=Locked 1=Unlocked
10	OV	Analog Monitor
11	+15/2V	Analog Monitor
12	-15/2V	Analog Monitor
13	+5V	Analog Monitor
14	Analog 4	Spare Analog Monitor via P11

15	Analog 5	Spare Analog Monitor via P11
16	100 MHz det Level	Same Voltage as 06 above
17	Analog 7	Spare Analog Monitor via P11

Interpretation of Digital Monitor Values:

Sig/Ref Switch Readback: Address = 5 -- bit 0 = 1
Results: Same as Command above.

LO Transmitter Lock Detect: Address = 8 -- bit 0 = 1
Results: 0 = LOCKED 1 = UNLOCKED

Notes:

1. The Signal/Reference Switch is used to select between the 130 Hz LO signal and the 130 Hz reference generated by this module. The 130 Hz signal is derived from the 500 MHz LO signal that goes up the LO cable to the antenna vertex room and comes back, and thus varies with length of the cable. The Round-Trip Phase module compares this with an internally generated 130 Hz reference in order to keep track of cable length changes. The Sig/Ref switch allows the reference to be coupled through the LO Transmitter and into the signal input for testing purposes.

2. The 0° and 90° counts are twenty four bit words which are assembled from the lower 16 bits (0-15) plus the upper 8 bits (16-23). Each count represents a change of 0.000064 millimeter in the length of the LO cable. Because of the noise in the system, the counts must be averaged in order to be able to determine length changes to a resolution of 0.005 millimeter as desired.

Description of I/O Lines

42-PIN REAR PANEL CONNECTOR:

2.083 kHz OUT: Goes to LO TRANSMITTER to lock PLL at 2.083 kHz offset from 500 MHz LO signal.
5 MHz IN: From 5 MHz MASER to timing counter chain.
XMIT+, XMIT-: Monitor/Control transmit bus input from station computer.
+5 VOLT SUPPLY: +5 V input from power supply.
RCV+, RCV-: Monitor/Control receive bus output tostation computer.
+15 VOLT SUPPLY: +15 V input from power supply.
-15 VOLT SUPPLY: -15 V input from power supply.
130 Hz SIG/TEST: Output from M/C system to switch in the LO TRANSMITTER which selects normal 130 Hz signal and the 130 Hz reference for test purposes (130 Hz OUT below).
DETECTOR IN: From LO TRANSMITTER, measures 100 MHz MASER signal power level.
GROUND: Module ground for signals and return for power supplies.
130 Hz OUT: Reference switched in place of the 130 Hz signal to test the LO TRANSMITTER circuitry.
1 PPS IN: 1 pulse per second from TIMING Module to reset ROUND TRIP MONITOR once per second.
130 Hz IN: Signal from LO TRANSMITTER whose phase is compared in the ROUND TRIP MONITOR with the 130 Hz reference.
TXMITTER LOCK DET: Allows M/C system to determine if PLL in LO TRANSMITTER is locked.

REAR PANEL RF CONNECTORS (OSP)

1.953 kHz OUT: Goes to vertex room LO RECEIVER to LO return modulator.
2.083 kHz OUT: Goes to vertex room LO RECEIVER to LO Phase Lock Loop.

VLBA ROUND TRIP MONITOR L103 MODULE INTERNAL WIRING HARNESS 8-14-89

DRAWING:A53304W002 WILLIAM WIREMAN FILE:B:L103HARN
NOTE: (L) INDICATES THE SIGNAL IS LOW TRUE, EX. HI-LO(L) LO=LOW SIGNAL

PART I-WIREWRAP CONNECTOR WIRING

PIN	FUNCTION	SOURCE	COLOR	GA.	PIN	FUNCTION	SOURCE	COLOR	GA.
1.	GND	REF GND	BLK	22	2.	5V	TB1-4	ORG	22
3.	GND				4.	5V			
5.	COAX RET	P11-39	SHIELD		6.	1PPS	P11-39	COAX	RG-188
7.	COAX RET	P11-5	SHIELD		8.	2.083KHZ	P11-5	COAX	RG-188
9.	COAX RET	P11-40	SHIELD		10.	130HZ SIG	P11-40	COAX	RG-188
11.	COAX RET	P11-38	SHIELD		12.	130HZ REF	P11-38	COAX	RG-188
13.	R/W(L)	J1-49	WHT/BLU	26	14.	HI-LO(L)SEL	J1-17	WHT/BLK	26
15.	DEV ACK	J1-36	WHT/GRY	26	16.	DEV REQ	J1-35	WHT/BRN	26
17.	ID READ	J2-9	WHT/ORG	26	18.	ANENB	J1-37	WHT/VIO	26
19.					20.	SW OUT	P11-25	WHT/BLU	26
21.					22.	LOCK DET	P11-41	WHT/GRN	26
23.	ADDR 6	J1-42		26	24.	ADDR 7	J1-41		26
25.					26.				
27.	COAX RET	P11-7	SHIELD		28.	5MHZ	P11-7		RG-188
29.	ADDR 0	J1-48	WHT/VIO	26	30.	ADDR 1	J1-47	WHT/YEL	26
31.	ADDR 2	J1-46	WHT/BLK	26	32.	ADDR 3	J1-45	WHT/RED	26
33.	ADDR 4	J1-44		26	34.	ADDR 5	J1-43		
35.	C/M 0	J1-33	WHT/ORG	26	36.	C/M 1	J1-16	WHT/ORG	26
37.	C/M 2	J1-32	WHT/BLU	26	38.	C/M 3	J1-15	WHT/BLU	26
39.	C/M 4	J1-31	WHT/RED	26	40.	C/M 5	J1-14	WHT/RED	26
41.	C/M 6	J1-30	WHT/BLK	26	42.	C/M 7	J1-13	WHT/BLK	26
43.	C/M 8	J1-29	WHT/YEL	26	44.	C/M 9	J1-12	WHT/YEL	26
45.	C/M 10	J1-28	WHT/VIO	26	46.	C/M 11	J1-11	WHT/VIO	26
47.	C/M 12	J1-27	WHT/GRY	26	48.	C/M 13	J1-10	WHT/GRY	26
49.	GND				50.				
51.	C/M 14	J1-26	WHT/BRN	26	52.	C/M 15	J1-9	WHT/BRN	26
53.	COAX RET	FRT.PNL.	SHIELD		54.	2.083KHZ	FRT.PNL.	COAX	RG-188
55.	COAX RET	FRT.PNL.	SHIELD		56.	1.953KHZ	FRT.PNL.	COAX	RG-188
57.	COAX RET	FRT.PNL.	SHIELD		58.	130HZ	FRT.PNL.	COAX	RG-188
59.	COAX RET	FRT.PNL.	SHIELD		60.	130HZ SIG	FRT.PNL.	COAX	RG-188
61.					62.				
63.					64.				
65.					66.				
67.					68.				
69.					70.				
71.					72.	2.083 KHz*	P10	COAX	RG-188
73.	COAX RET	P9/P10	SHIELD		74.	1.953KHZ	P9	COAX	RG-188
75.					76.				
77.					78.				
79.					80.				

INTERNAL WIRING HARNESS (cont.)

81.					82.				
83.					84.				
85.					86.				
87.					88.	+5V	J1-4		26
89.					90.	-15/2V	J1-3		26
91.					92.	+15/2V	J1-2		26
93.					94.	+15/V	TB1-6	RED	22
95.					96.	-15V	TB1-5	YEL	22
97.	GND				98.	5V			
99.	GND	REF GND	BLK	22	100.	5V	TB1-4	ORG	22

PART II-STANDARD INTERFACE BOARD WIRING

JACK J1

PIN	FUNCTION	SOURCE	COLOR	GA
1.	GROUND	TB-1-1		26
2.	+15/2V	W-92		26
3.	-15/2V	W-90		26
4.	+15V	W-88		26
5.	ANALOG 4+	P11-18		26
6.	ANALOG 5+	P11-20		26
7.	DET IN	P11-26	WHT/ORG	26
8.	ANALOG 7+	P11-22		25
9.	C/M 15	W-52	WHT/BRN	26
10.	C/M 13	W-48	WHT/GRY	26
11.	C/M 11	W-46	WHT/VIO	26
12.	C/M 9	W-44	WHT/YEL	26
13.	C/M 7	W-42	WHT/BLK	26
14.	C/M 5	W-40	WHT/RED	26
15.	C/M 3	W-38	WHT/BLU	26
16.	C/M 1	W-36	WHT/ORG	26
17.	HI-LO(L)SEL	W-14	WHT/BLK	26
18.	GND	TB1-1		26
19.	GND	TB1-1		26
20.	GND	TB1-1		26
21.	GND	TB1-1		26
22.	ANALOG 4-	P11-19		26
23.	ANALOG 5-	P11-21		26
24.	DET IN RET	P11-38	BUSS	26
25.	ANALOG 7-	P11-23		26
26.	C/M 14	W-51	WHT/BRN	26
27.	C/M 12	W-47	WHT/GRY	26
28.	C/M 10	W-45	WHT/VIO	26
29.	C/M 8	W-43	WHT/YEL	26
30.	C/M 6	W-41	WHT/BLK	26
31.	C/M 4	W-39	WHT/RED	26
32.	C/M 2	W-37	WHT/BLU	26
33.	C/M 0	W-35	WHT/ORG	26
34.	GND	REF GND	BLK	22
35.	DEV REQ	W-16	WHT/BRN	26
36.	DEV ACK	W-15	WHT/GRY	26
37.	ANENB	W-18	WHT/VIO	26

JACK J2

PIN	FUNCTION	SOURCE	COLOR	GA
1.	5V			
2.				
3.				
4.				
5.	RST+	P11-35	GRN-PR	26
6.	RST-	P11-36	BLK-PR	26
7.				
8.				
9.	ID READ	W-17	WHT/ORG	26
10.				
11.				
12.				
13.	GND	REF GND	BLK	22
14.	5V	TB1-4	ORG	22
15.	15V	TB1-6	RED	22
16.	-15V	TB1-5	YEL	22
17.				
18.				
19.	RCV+	P11-14	WHT-PR	26
20.	RCV-	P11-15	BLK-PR	26
21.	XMIT+	P11-8	RED-PR	26
22.	XMIT-	P11-9	BLK-PR	26
23.				
24.				
25.	GND			

INTERNAL WIRING HARNESS (cont.)

38. GND				
39. -15V	TB1-5	YEL	22	
40. 15V	TB1-6	RED	22	
41. ADDR 7	W-24		26	
42. ADDR 6	W-23		26	
43. ADDR 5	W-34		26	
44. ADDR 4	W-33		26	
45. ADDR 3	W-32	WHT/RED	26	
46. ADDR 2	W-31	WHT/BLK	26	
47. ADDR 1	W-30	WHT/YEL	26	
48. ADDR 0	W-29	WHT/VIO	26	
49. R/W(L)	W-13	WHT/BLU	26	
50. 5V	TB1-4	ORG	22	

PART III-REAR PANEL CONNECTOR WIRING

JACK P11 (AMP 42 PIN)

PIN	FUNCTION	SOURCE	COLOR	GA	PIN	FUNCTION	SOURCE	COLOR	GA
1.					2.				
3.					4.				
5.	2.083KHZ	W-8	CO-AX	RG-188	6.				
7.	5MHZ	W-28	CO-AX	RG-188	8.	XMIT+	J2-21	RED-PR	26
9.	XMIT-	J2-22	BLK-PR	26	10.	5V	TB1-4	ORG	20
11.					12.				
13.					14.	RCV+	J2-19	WHT-PR	26
15.	RCV-	J2-20	BLK-PR	26	16.	15V	TB1-6	RED	20
17.	-15V	TB1-5	YEL	20	18.	ANALOG 4+	J1-5		26
19.	ANALOG 4-	J1-22		26	20.	ANALOG 5+	J1-6		26
21.	ANALOG 5-	J1-23		26	22.	ANALOG 7+	J1-8		26
23.	ANALOG 7-	J1-25		26	24.				
25.	SW OUT	W-20	WHT/BLU	26	26.	DET IN	J1-7	WHT/ORG	26
27.					28.				
29.					30.				
31.					32.				
33.					34.	GND	TB1-1	BLK	20
35.	RST+	J2-5	GRN-PR	26	36.	RST-	J2-6	BLK-PR	26
37.					38.	130HZ O	W-12	CO-AX	RG-188
39.	1PPS	W-6	CO-AX	RG-188	40.	130HZ IN	W-10	CO-AX	RG-188
41.	LOCK DET	W-22	WHT/GRN	26	42.				

OSP CONNECTORS

PIN	FUNCTION	SOURCE	TYPE	SHIELD	SOURCE	NOTES
P1						
P2						
P3						
P4						
P5						
P6						
P7						
P8						
P9	1.953KHZ	W-74	RG-188	SHIELD	W-73	USE SMA AT P9
P10	2.083KHZ	W-72	RG-188	SHIELD	W-73	USE SMA AT P10

INTERNAL WIRING HARNESS (cont.)

PART IV-POWER DISTRIBUTION TERMINAL BLOCK

POWER SUPPLY INPUT					POWER DISTRIBUTION		
PIN	FUNCTION	SOURCE	COLOR	GA	SOURCE	COLOR	GA
TB1-1	GND	P11-34	BLK	20	GND REF	BLK	22
TB1-2							
TB1-3							
TB1-4	5V	P11-10	ORG	20	J1-50, J2-14, W-2, W-100	ORG	22
TB1-5	-15V	P11-17	YEL	20	J1-39, J2-16, W-96	YEL	22
TB1-6	15V	P11-16	RED	20	J1-40, J2-15, W-94	RED	22
TB1-7							

PART V-FRONT PANEL BNC TEST POINTS

PIN	FUNCTION	SOURCE	COLOR	GA	RET SOURCE	COLOR	GA
BNC-1	2.08 KHz	W-54		RG-188	W-53	SHIELD	
BNC-2	1.95 KHz	W-56		RG-188	W-55	SHIELD	
BNC-3	130 Hz REF	W-58		RG-188	W-57	SHIELD	
BNC-4	130 Hz SIG	W-60		RG-188	W-59	SHIELD	

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
E	4-88	K. TATE		UPDATED TO NRAO STANDARDS
F	12-88	K. TATE	W. ZAMORA	ADDED MORE ANALOG CHANNELS

DIVIDE 5

DIVIDE 16

DIVIDE 16

DIVIDE 15

90 DEGREE

0 DEGREE

DIVIDE 8

90 DEGREE

0 DEGREE

MOUNT C4 A BINFO CAPACITOR ACROSS PIN 8. THE POSITIVE SIDE, TO PIN 8.

NOTE: 2.2M CAP ON 9E NON-POL.

WIRE 16B TO 16B VCC INPUT

ADDRESS MAP

Y0	00	0 DEGREE LSB
	01	0 DEGREE MSB
	10	90 DEGREE LSB
	11	90 DEGREE MSB
		SERIAL NUMBER
		DGV/MON TEST SWITCH
		ANALOG 100KHZ DET
		08 BIT 0 = LOCK DET
		10 ANALOG 0 VOLTS
		+15/8 VOLTS
		-15/8 VOLTS
		+5 VOLTS
		EXTERNAL ANALOG 4
		EXTERNAL ANALOG 5
		ADDR. 6 = ADDR. 16
		EXTERNAL ANALOG 7

ORCAD : 53304S03

ASSB04N002	WIRE LIST
ASSB04B010	BOM
DSSB04A010	ASSEMBLY
NEXT ASSEMBLY	DWG TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
3 PLACE DECIMALS (.000): ±
2 PLACE DECIMALS (.00): ±
1 PLACE DECIMALS (.0): ±

MATERIAL:

FINISH:

VLBA PROJECT

LO REF DISTRIBUTION

L103 MODULE
ROUND TRIP MONITOR
SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	N. WINEHAM	DATE	11-87
DESIGNED BY		DATE	
APPROVED BY		DATE	
SHEET NUMBER	1 OF 1	DRAWING NUMBER	D5SB04B008 REV F SCALE -

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
C	1-91	ANDREATTA		REDRAWN WITH ACAD ;

CPU ADDRESS/DATA BUS

CONTROL/MONITOR LINE BUFFERS

PARALLEL I/O P1

SERIAL I/O P2

U1 INTEL P8032AH uCONT — CONTROL PROCESSOR

U2 INTEL D8755A-2 — EPROM PROGRAM MEMORY

U5 INTEL P8156H-2 — RAM-I/O

U10 74LS245

U11 74LS245

U8 75174 DIFF DRIVER

U9 75175 DIFF RECEIVER

U3 74LS173

U7A 74LS221

U7B 74LS221

U12B 96LS02

U15 LS00

U16 LS04

U17 LS10

U18 LS04

RELATIVE ADDR TO ADDR BUS DRIVER U4 (SHT 2)

12 BIT ANALOG CONV. FROM U14 (SHT 2)

R/W U13-1 (SHT 2)

IOR U17-4 (SHT 2)

INSTALL HAND WIRE LINK TO P1.7 OR DESIRED SIGNAL

RESET LINK
R to b — FOR SYSTEM RESET INPUT (P2-24,6)
R to a — FOR EXTERNAL RESET INPUT (P2-23)

WARNING :
CPU U1 WILL NOT RUN IF LINK "R" IS LEFT FLOATING. IT MUST BE TERMINATED TO LINK "a" OR "b".

EXTERNAL INDICATOR DRIVER

ACTIVITY INDICATORS (EXTERNAL)

NOTES :
1. ALL IC's ARE "LS" LOGIC UNLESS OTHERWISE INDICATED.
2. USE EXACT PART NUMBERS ONLY ON U1, U2, AND U5. DO NOT SUBSTITUTE.
3. BYPASS CAPACITORS (.01 "Cx" ON ASSEMBLY DWG.) NOT SHOWN.
4. * = NOT USED.
5. ALL RESISTOR VALUES ARE IN OHMS.

ACAD : SIBDSK-1

A55002B002	BOM
D55002A002	ASSEMBLY
D55002P002	DRILL DWG.
D55002Q002	ARTWORK
NEXT ASSEMBLY	DWG. TYPE

CPU, MEMORY, AND I/O DRIVERS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL :
FINISH :

VLBA STANDARD INTERFACE BOARD

STANDARD INTERFACE BOARD MODEL "D" SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801

DRAWN BY	HARDEN
DATE	12-85
DESIGNED BY	WEBER
DATE	5-84
APPROVED BY	
DATE	
SHEET NUMBER	1 of 2
DRAWING NUMBER	D55002S002
REV.	C
SCALE	—

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
C	1-91	ANDREATTA		REDRAWN WITH ACAD ;

PARALLEL I/O P1

+5V 50 ← +5V DISTR
5V COMM 34 ← DIGITAL GND
+15V 40 ← +15V DISTR
HIQ GND 38 ← ANALOG GND
−15V 39 ← −15V DISTR
DEV ACK 36 ← DEVICE ACKNOWLEDGE
ANENB 37 ← ANALOG ENABLE

R/W U16-12 (SHT 1)
IOR U2-30 (SHT 1)

+5V
R7 1K
74LS74 PR D Q U13 CLR
PU1
LS10 U17
LS00 U15
U16 LS04
U12A 96LS02 Rx Cx CLR
R6 15K
C8 220pF
STRB/72SR 1uS
TO U1-12 CPU INTR-0 (SHT 1)

H = D0−D11 IS IN HI-Z STATE
L = D0−D11 DUMPED ON BUS

S/H CONT (L = CONVERSION IN PROGRESS)
BUSY
STRB
EN1 EN2 EN3 OUTPUT D0−D11
DT1 EN
SHORT CYCLE
ANALOG COMM

ANLG-0 H 1 L 18 ← DIFFERENTIAL ANALOG INPUTS → CH1+ 11, CH1− 70
ANLG-1 H 2 L 19 → CH2+ 10, CH2− 71
ANLG-2 H 3 L 20 → CH3+ 9, CH3− 72
ANLG-3 H 4 L 21 → CH4+ 8, CH4− 73
ANLG-4 H 5 L 22 → CH5+ 7, CH5− 74
ANLG-5 H 6 L 23 → CH6+ 6, CH6− 75
ANLG-6 H 7 L 24 → CH7+ 5, CH7− 76
ANLG-7 H 8 L 25 → CH8+ 4, CH8− 77

U14
SDM854BG (BURR-BROWN)
ANALOG DATA ACQUISITION SYSTEM

CONFIGURED FOR
8-CHAN DIFFERENTIAL INPUTS
BIPOLAR OPERATION (±10V RANGE)
12-BIT RESOLUTION (4.8828 mV/BIT)
2's COMPLIMENT OUTPUT CODING
OUTPUT IS ONE 12-BIT WORD, HI-Z DRIVERS

D0 29 LSB → CON/MON-4
D1 30 → CON/MON-5
D2 31 → CON/MON-6
D3 32 → CON/MON-7
D4 33 → CON/MON-8
D5 34 → CON/MON-9
D6 35 → CON/MON-10
D7 36 → CON/MON-11
D8 37 → CON/MON-12
D9 38 → CON/MON-13
D10 39 → CON/MON-14
D11 40
DT1 44 MSB → CON/MON-15

CON/MON BUS (12-BIT ANALOG CONVERSION) TO P1 (SHT 1)

MUX EN1 12
MUX EN2 13
CLR 19 +5V
S/H OFFSET 67
+15V
RV3 1K
R9 24K
FINE OFFSET ADJ

A0 A1 A2 A3 DIG GND LOAD DLY OUT TRIG DLY ADJ BPO 2.5V REF OUT IN MUX OUT − + 20V RANGE S/H OUT S/H IN
R10 340
RG1 RG2
NC OFFSET
−15V +15V

HI/LO SEL 17
+5V 470
U6 74LS157 SEL 1A 1B 2A 2B 3A 3B 4A 4B 1Y 2Y 3Y 4Y
ADDR-0 ADDR-1 ADDR-2 ADDR-3 ADDR-4 ADDR-5
250 uS LOAD ADC TRIG A/D
C11 .01 uF
RV2 50 ZERO
RV1 100 GAIN

FOR 4.8828 mV/bit INSTALL JUMPER IN LIEU OF R10
FOR 5.0 mV/bit INSTALL 240 OHM WW RESISTOR PER BURR-BROWN SPECS

U19
BURR-BROWN INA101CM INSTR. AMPL.
U19 PIN OUT (TOP VIEW)

+5V 74LS245 ADDR BUS DRIVER
FROM U2 (SHT 1)
RA0 A0 B0 ADDR-0
RA1 A1 B1 ADDR-1
RA2 A2 B2 ADDR-2
RA3 A3 B3 ADDR-3
RA4 A4 B4 ADDR-4
RA5 A5 B5 ADDR-5
RA6 A6 B6 ADDR-6
RA7 A7 B7 ADDR-7
PU2 DIR U4
ADDRESS BUS

PARELLEL I/O P1
ADDR-0 48 → RA-0
ADDR-1 47 → RA-1
ADDR-2 46 → RA-2
ADDR-3 45 → RA-3
ADDR-4 44 → RA-4
ADDR-5 43 → RA-5
ADDR-6 42 → RA-6
ADDR-7 41 → RA-7

SERIAL I/O P2
+5V DISTR 1, 14 → +5V
DIGITAL GND 13, 25 → LOGIC COMM
+15V DISTR 15 → +15V
ANALOG GND 17 → ±15V COMM
−15V DISTR 16 → −15V
EXTERNAL ACCESSORY DC POWER AVAILABLE FOR TEST AND ALIGNMENT PURPOSES

U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 (SEE DETAIL) U15 U16 U17 U18
P2 SERIAL I/O
P1 PARALLEL I/O
FINE O.S. ADJ RV3
ZERO RV2
GAIN RV1
R10 R9 C11 LOCATED UNDERNEATH U14 TOP SIDE
BYPASS CAPACITORS NOT SHOWN
U14 PIN OUT (TOP VIEW)

ACAD : SIBDSK-2

A55002B002	BOM
D55002A002	ASSEMBLY
D55002P002	DRILL DWG.
D55002Q002	ARTWORK
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL :
FINISH :

ANALOG CIRCUITRY

VLBA CORRELATOR: STANDARD INTERFACE BOARD

STANDARD INTERFACE BOARD MODEL "D" SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801

DRAWN BY HARDEN	DATE 12-85
DESIGNED BY WEBER	DATE 5-84
APPROVED BY	DATE
SHEET NUMBER 2 of 2	DRAWING NUMBER D55002S002
REV. C	SCALE —

TYPES DS7831, DS7832, DS8831, DS8832 LINE DRIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. OL-S 7712496, JANUARY 1977

- TTL Compatible
- Propagation Delay Time . . . 15 ns Typ
- Very Low Output Impedance with High Drive Capability
- 40-mA Sink and Source Capability
- Gating Control to Allow Either Single-Ended or Differential Operation
- Three-State Outputs for Party-Line (Data-Bus) Operation

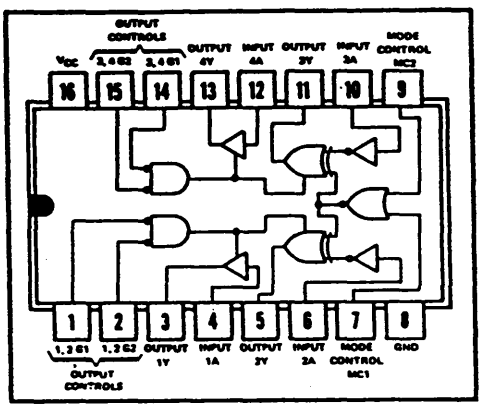
description

The DS7831, DS7832, DS8831, and DS8832 can be used as either quadruple single-ended line drivers or as dual differential line drivers. This multi-mode operation and simple logic control make these devices especially useful for party-line or bus-organized systems. The DS7831 and DS8831 have output clamp diodes to V_{CC}; the DS7832 and DS8832 do not.

For one of these circuits to operate as four independent single-ended line drivers, both mode-control pins must be low. In this mode, no signal inversion takes place between inputs and outputs. To operate as a dual differential line driver, at least one of the mode control inputs must be high. Inputs 1A and 2A should be connected together as should 3A and 4A. Then signals applied to the inputs will appear noninverted at 1Y and 4Y and inverted at 2Y and 3Y, provided the output control pins are low.

While enabled, these outputs provide good drive capability for capacitive loads, and fast transitions from both low-to-high levels and high-to-low levels.

DS7831, DS7832.....J PACKAGE
DS8831, DS8832.....J OR N PACKAGE
(TOP VIEW)



Taking either of the associated output controls high disables the outputs. When disabled, these three-state outputs neither load nor drive a line and hundreds of these devices may be connected to a common bus line. Only one output should be enabled at a time.

The DS7831 and DS7832 are characterized for operation over the full military temperature range of −55°C to 125°C. The DS8831 and DS8832 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

OUTPUT CONTROLS		MODE CONTROLS		DATA INPUT	OUTPUT	DATA INPUT	OUTPUT
G1	G2	MC1	MC2	1A/4A	1Y/4Y	2A/3A	2Y/3Y
L	L	L	L	H	H	H	H
L	L	L	L	L	L	L	L
L	L	X	H	H	H	H	L
L	L	H	X	L	L	L	H
H	X	X	X	X	Z	X	Z
X	H	X	X	X	Z	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range: DS78' . . . . . −55°C to 125°C
DS88' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, DS7831 and DS7832 chips are alloy-mounted; DS8831 and DS8832 chips are glass-mounted.

recommended operating conditions

	DS78'			DS88'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_O			5.5			5.5	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature range, T_A	−55		125	0		70	°C

5

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −2 mA	DS7831,DS7832	2.4	3.1		V
			I_{OH} = −5.2 mA	DS8831,DS8832	2.4	3.0		
			I_{OH} = −40 mA		1.8	2.5		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 32 mA			0.26	0.4	V
			I_{OL} = 40 mA			0.3	0.5	
V_{OK}	Output clamp voltage	V_{CC} = 5 V, T_A = 25°C	I_O = −12 mA				−1.5	V
			I_O = 12 mA	DS7831,DS8831			V_{CC} + 1.5	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, T_A = 25°C	V_O = 2.4 V				40	μA
			V_O = 0.4 V				−40	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V					40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_O = 0,		T_A = MAX	−40	−70	−120	mA
I_{CC}	Supply current	V_{CC} = MAX				50	90	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V.
§ Only one output should be shorted at a time.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

National Semiconductor

Voltage Comparators

LM160/LM260/LM360 High Speed Differential Comparator

General Description

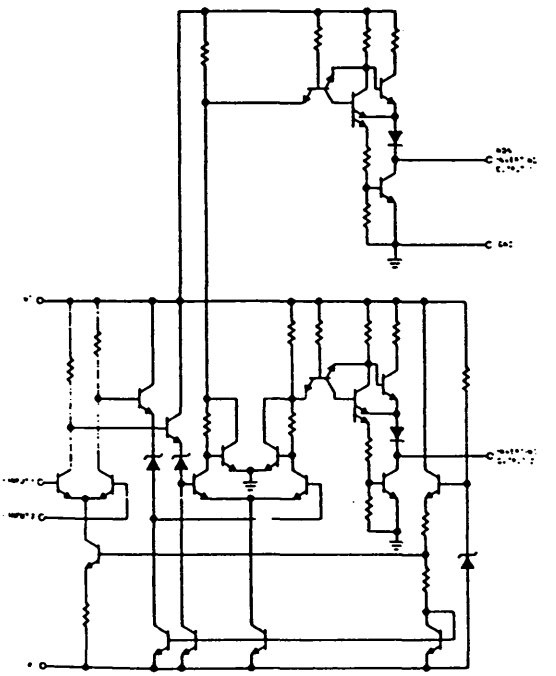
The LM160/LM260/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 500 mV.

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disc file systems.

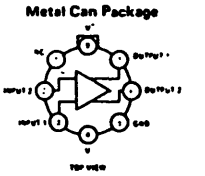
Features

- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

Schematic and Connection Diagrams

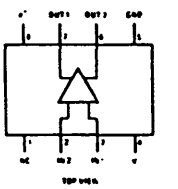


Metal Can Package



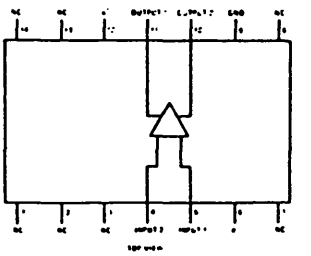
Order Number LM160H, LM260H or LM360H
See NS Package H08C

Dual-In-Line Package



Order Number LM360N
See NS Package N08B

Dual-In-Line Package



Order Number LM360N 14
See NS Package N14A

Order Number LM160J-14, LM260J-14
See NS Package J14A

Absolute Maximum Ratings

Positive Supply Voltage	+8V	Operating Temperature Range	
Negative Supply Voltage	−8V	LM160	−55°C to +125°C
Peak Output Current	20 mA	LM260	−25°C to +85°C
Differential Input Voltage	±5V	LM360	0°C to +70°C
Input Voltage	$V^+ \geq V_{IN} \geq V^-$	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Conditions					
Supply Voltage V_{CC}^+		4.5	5	6.5	V
Supply Voltage V_{CC}^-		−4.5	−5	−6.5	V
Input Offset Voltage	$R_S \leq 200\Omega$		2	5	mV
Input Offset Current			.5	3	μA
Input Bias Current			5	20	μA
Output Resistance (Either Output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	$T_A = 25°C$, $V_S = \pm5V$ (Note 1)		13	25	ns
	$T_A = 25°C$, $V_S = \pm5V$ (Note 2)		12	20	ns
	$T_A = 25°C$, $V_S = \pm5V$ (Note 3)		14		ns
Response Time Difference Between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
Input Resistance	f = 1 MHz		17		kΩ
Input Capacitance	f = 1 MHz		3		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		8		μV/°C
Average Temperature Coefficient of Input Offset Current			7		nA/°C
Common Mode Input Voltage Range	$V_S = \pm6.5V$	±4	±4.5		V
Differential Input Voltage Range		±5			V
Output High Voltage (Either Output)	$I_{OUT} = -320\mu A$, $V_S = \pm4.5V$	2.4	3		V
Output Low Voltage (Either Output)	$I_{SINK} = 6.4$ mA		.25	.4	V
Positive Supply Current	$V_S = \pm6.5V$		18	32	mA
Negative Supply Current	$V_S = \pm6.5V$		−9	−16	mA

Note 1: Response time measured from the 50% point of a 30 mV_{p-p} 10 MHz sinusoidal input to the 50% point of the output.

Note 2: Response time measured from the 50% point of a 2 V_{p-p} 10 MHz sinusoidal input to the 50% point of the output.

Note 3: Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold