

NATIONAL RADIO ASTRONOMY OBSERVATORY
Socorro, New Mexico

VLBA TECHNICAL REPORT NO. 34

FRONT-END F110 (43 GHz) CARD CAGE CIRCUITRY

Addendum to VLBA TECHNICAL REPORT NO. 11

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1.0 INTRODUCTION

Technical Report No. 34 is an addendum to VLBA TECHNICAL REPORT NO. 11 (F110, 43 GHz, 7 mm). This report augments the RF, thermal and physical descriptions contained in the TECHNICAL REPORT NO. 11 (TR 11) by describing the card cage circuitry and its interfaces with the RF amplifiers, vacuum and temperature sensors, vacuum valve, refrigerator, heater, calibration, and Monitor and Control system. The temperature and pressure transducer characteristics are also described. Since the Front-End's RF and thermal characteristics are described in TR 11, these topics are not included in this addendum.

An important graphic feature of the Theory of Operation (Section 2.0) is a detailed Front-End block diagram that shows all Front-End interconnect and interface circuitry. Reduced scale copies of the schematic and assembly drawings for the four card types and the associated BOMs are included. The card descriptions include alignment procedures.

Section 3 contains a list of relevant NRAO Technical Reports and memoranda.

Section 4 contains data sheets for special-purpose components used in the card cage circuitry.

Since TR 11 contains card cage BOM drawings and the wire list, they are not included in this addendum. These drawings are referenced in the circuitry descriptions as required.

Q-band Front-Ends have been fabricated in two different NRAO laboratories: Greenbank, West Virginia and Socorro, New Mexico. From the perspective of this card cage circuitry manual, both versions are virtually identical; the only significant construction difference is the DC Feedthrough panel. F110, the Greenbank Q-band Front-End, uses the B53213M008 DC Feedthrough; drawing A53213A008, the DC Feedthrough Cable assembly listed in the F110 assembly drawing D53213A001-1, does not exist. The BOM for this assembly is A53213B006 and is shown on TR 11 Appendix page II-9. The Socorro 6 mm Front-End uses a Bendix hermetically-sealed connector and a 21-wire cable instead of B53213M008. The two versions are described in Section 2.10.

2.0 THEORY OF OPERATION

2.1 Front-End Block Diagram and Card Cage Drawings

Drawing C53213K002, following this text, is the 43 GHz Front-End block diagram and provides a functional overview of the F110 circuitry. It shows the card cage, dewar, RF Plate, pressure and temperature transducers, vacuum valve, refrigerator control, and Monitor and Control interface circuitry. The five card types are shown in block form; the card's schematic, assembly and BOM drawings are included for reference in the circuit card descriptions.

I/O connector pins and signals are tabulated in Section 2.3.

The card cage assembly drawing listed on the Front-End Assembly Drawing is D53213A006; this drawing does not exist. TR 11, Appendix page II-1 lists D53206A005 (used in F016, the 8.4 GHz Front-End) as the card cage assembly drawing. This drawing follows the 43 GHz Block Diagram. The card cage BOM is TR 11, Appendix page II-10.

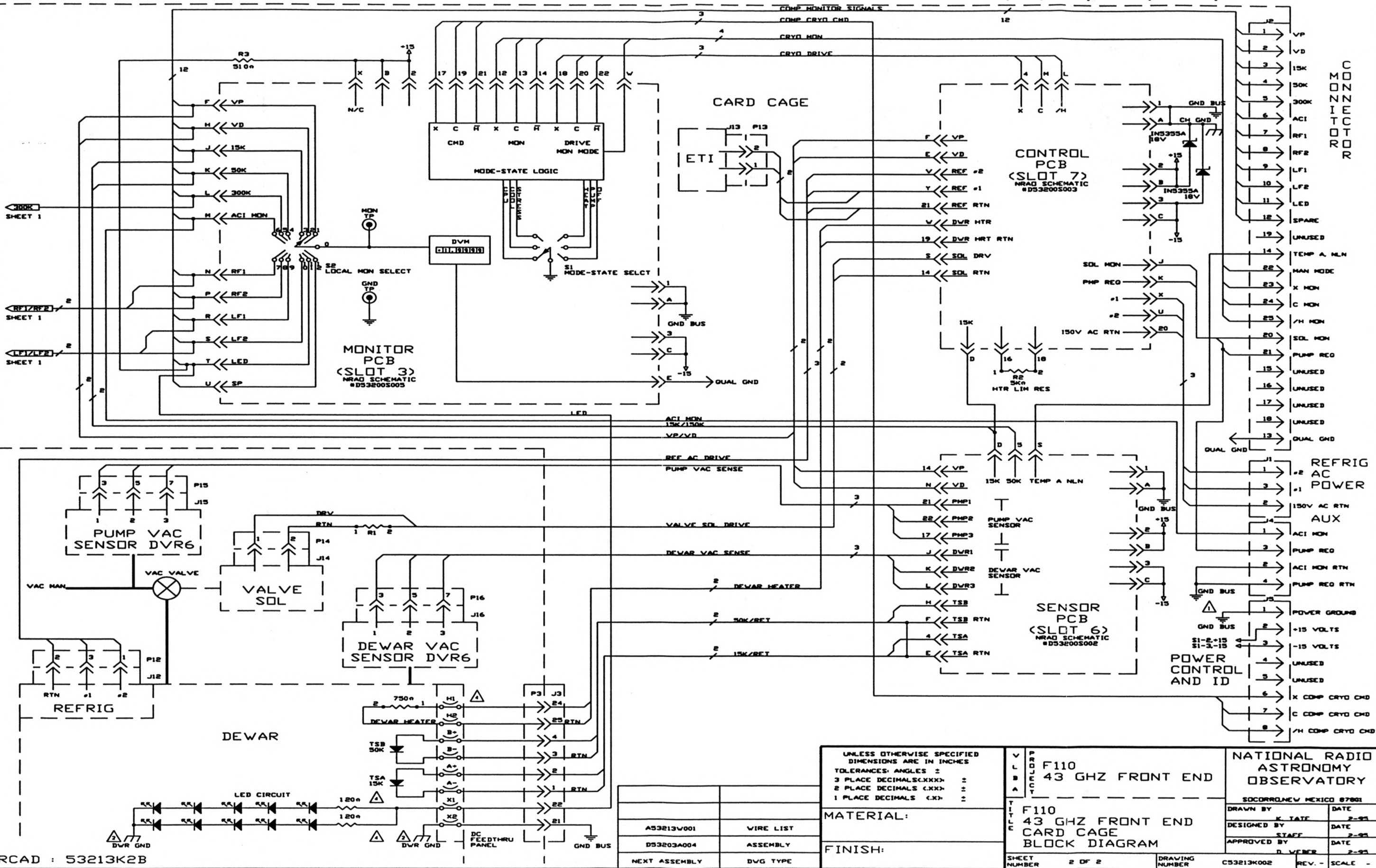
4

3

2

1

REV.	DATE	DRAWN BY	APPROV'D BY	DESCRIPTION



ORCAD : 53213K2B

PROPERTY OF NRAD

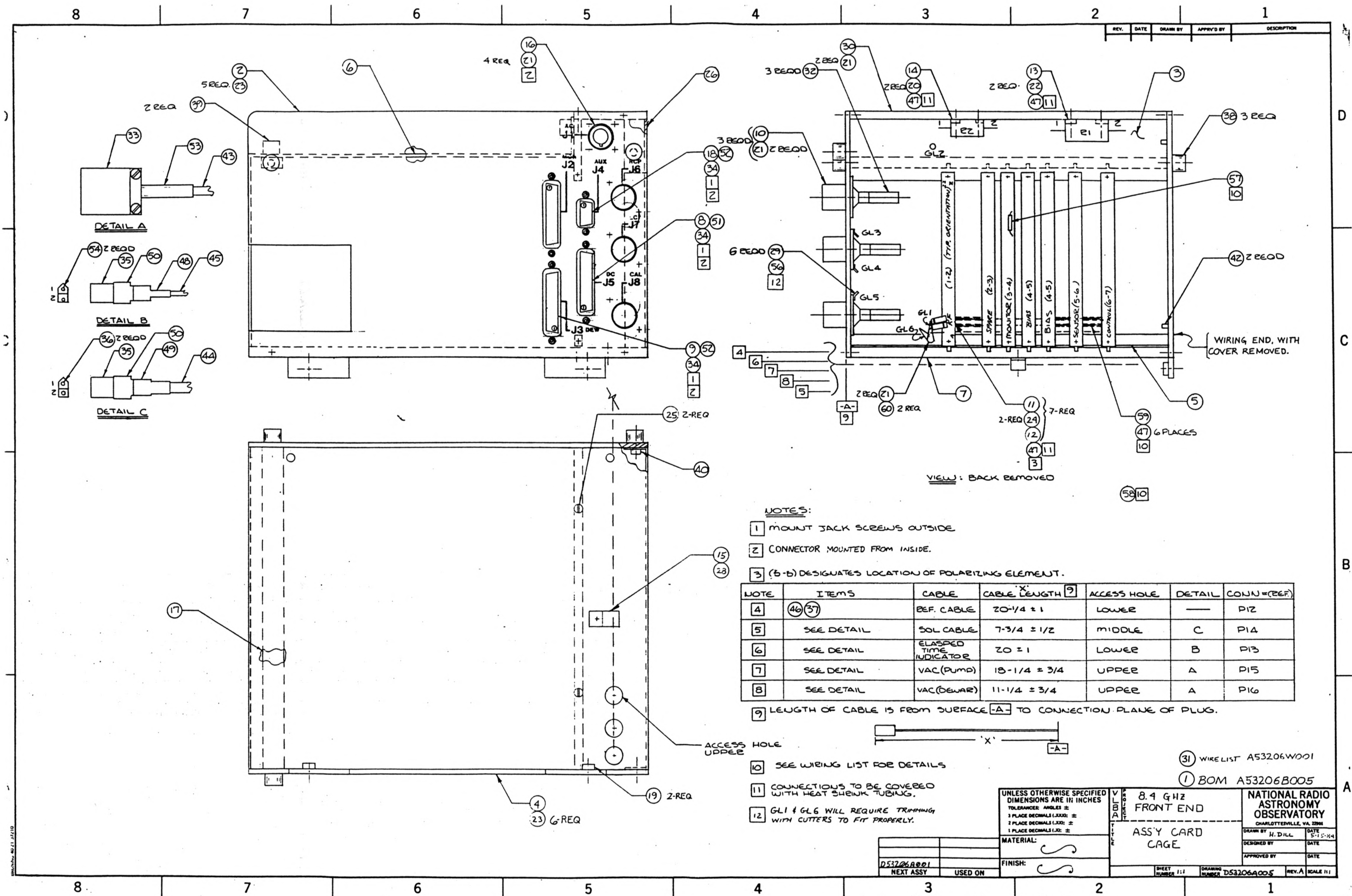
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES :
3 PLACE DECIMALS (XXX) :
2 PLACE DECIMALS (XX) :
1 PLACE DECIMALS (X) :

MATERIAL:
FINISH:

V L P F110
B L J 43 GHZ FRONT END
A E C T
T I L E F110
43 GHZ FRONT END
CARD CAGE
BLOCK DIAGRAM

NATIONAL RADIO
ASTRONOMY
OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY K TATE DATE 2-95
DESIGNED BY STAFF DATE 2-95
APPROVED BY D VEBER DATE 2-95
SHEET NUMBER 2 OF 2 DRAWING NUMBER C53213K002 REV. - SCALE -

ASSEMBLY	DWG TYPE
A53213V001	WIRE LIST
D53203A004	ASSEMBLY
NEXT ASSEMBLY	DWG TYPE

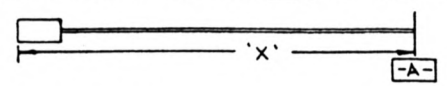


NOTES:

- 1 MOUNT JACK SCREWS OUTSIDE
- 2 CONNECTOR MOUNTED FROM INSIDE.
- 3 (b-b) DESIGNATES LOCATION OF POLARIZING ELEMENT.

NOTE	ITEMS	CABLE	CABLE LENGTH	ACCESS HOLE	DETAIL	CONN. (REF.)
4	(46) (37)	REF. CABLE	20-1/4 ± 1	LOWER	—	PI2
5	SEE DETAIL	SOL CABLE	7-3/4 ± 1/2	MIDDLE	C	PI4
6	SEE DETAIL	ELAPSED TIME INDICATOR	20 ± 1	LOWER	B	PI3
7	SEE DETAIL	VAC (PUMP)	18-1/4 ± 3/4	UPPER	A	PI5
8	SEE DETAIL	VAC (DEWAR)	11-1/4 ± 3/4	UPPER	A	PI6

9 LENGTH OF CABLE IS FROM SURFACE -A- TO CONNECTION PLANE OF PLUG.



- 10 SEE WIRING LIST FOR DETAILS
- 11 CONNECTIONS TO BE COVERED WITH HEAT SHRINK TUBING.
- 12 GL1 & GL6 WILL REQUIRE TRIMMING WITH CUTTERS TO FIT PROPERLY.

(31) WIRE LIST A53206W001
(1) BOM A53206B005

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (L&D); ± 2 PLACE DECIMALS (L&D); ± 1 PLACE DECIMALS (L&D); ±		8.4 GHz FRONT END		NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA 22901	
MATERIAL:		ASS'Y CARD CAGE		DRAWN BY: H. DILL DATE: 5-15-84	
FINISH:				DESIGNED BY: DATE:	
				APPROVED BY: DATE:	
DS3206A001 NEXT ASSY		USED ON		SHEET NUMBER 1:1 DRAWING NUMBER DS3206A005 REV. A SCALE 1:1	

2.2 Front-End Interface Signals and Characteristics

Card Cage Panel Connectors

J2-Monitor			J5-PMR, Control & ID			J3-Dewar Bias, LED & Temp		
Pin	Name	Function/Type	Pin	Name	Function/Type	Pin	Name	Function/Type
1	VP	PUMP VAC Mon/analog	1	GND	POWER GROUND	1	TSA Ret (15K)	Ret/analog
2	VD	DEWAR VAC Mon/analog	2	+15	+15V/FE Power	2	TSA Sig (15K)	Sig/analog
3	15K	15K TEMP Mon/analog	3	-15	-15V/FE Power	3	TSB Ret (50K)	Ret/analog
4	50K	50K TEMP Mon/analog	4	Not Used		4	TSB Sig (50K)	Sig/analog
5	300K	300K TEMP Mon/analog	5	Not Used		5	LCP GATE 1 BIAS	/analog
6	AC1	AC CURRENT Mon/analog	6	X	CONTROL BIT/TTL	6	LCP DRAIN 1 BIAS	/analog
7	RF1	RCP STAGE 1 Mon/analog	7	C	CONTROL BIT/TTL	7	LCP GATE 2 BIAS	/analog
8	RF2	OTHER STAGES Mon/analog	8	H	CONTROL BIT/TTL	8	LCP DRAIN 2 BIAS	/analog
9	LF1	LCP STAGE 1 Mon/analog	9	PA	FE PARITY/TTL	9	LCP GATE 4 BIAS	/analog
10	LF2	OTHER STAGES Mon/analog	10	Not Used		10	LCP DRAIN 3 BIAS	/analog
11	LED	LED VOLTAGE Mon/analog	11	CAL	+28V DRIVE/CMD	11	LCP GATE 4 BIAS	/analog
12	Not Used		12	HI CAL	+28V DRIVE/CMD	12	LCP DRAIN 4 BIAS	/analog
13	QGND	QUALITY GND/analog	13	GND	Not Used*	13	RCP GATE 1 BIAS	/analog
14	SENS	TEMP SENSE A Mon/analog	14	F0	LSB /TTL	14	RCP DRAIN 1 BIAS	/analog
15	Not Used		15	F1	FREQUENCY /TTL	15	RCP GATE 2 BIAS	/analog
16	Not Used		16	F2	ID /TTL	16	RCP DRAIN 2 BIAS	/analog
17	Not Used		17	F3	MSB /TTL	17	RCP GATE 3 BIAS	/analog
18	Not Used		18	S0	LSB /TTL	18	RCP DRAIN 3 BIAS	/analog
19	Not Used		19	S1	LSB /TTL	19	RCP GATE 4 BIAS	/analog
20	S	SOLENOID MON/TTL	20	S2	SERIAL /TTL	20	RCP DRAIN 4 BIAS	/analog
21	P	PUMP REQUEST MON/TTL	21	S3	NUMBER /TTL	21	DEWAR GND	Not Used*
22	M	MANUAL MON/TTL	22	S4	ID /TTL	22	LED	LED DRIVE/analog
23	X	CONTROL MON/TTL	23	S5	MSB /TTL	23	Not Used	
24	C	MODE MON/TTL	24	M0	MODIFICATION/TTL	24	DEWAR HEATER/150 VAC	
25	H	MONITOR MON/TTL	25	M1	MSB /TTL	25	DEWAR HEATER RET/AC	
J4-Auxiliary			J1-AC Power Interface			J17-RF Plate		
Pin	Name	Function/Type	Pin	Name	Function/Type	Pin	Name	Function/Type
1	AC+	CURRENT MON/analog	1	φ1	SHIFTED PHASE/150 VAC	1	Ground	
2	AC-	CURRENT MON/analog	2	φ2	LINE PHASE/150 VAC	2	+15 volts	
3	P	PUMP REQUEST CMD/TTL	3	RETURN		3	-15 volts	
4	GND	GROUND PUMP REQ RET/GND				4	Ground	
5 through 9	Not Used					5	Low Cal Control	
						6	High Cal Control	
						7	Cal Return	
						8	300 °K Temp Mon	
						9	Not Used	

Dewar DC Feedthrough - See Figure 4 in Section 2.10.

RF I/O Connectors: J6-RCP RF Out; J7-LCP RF Out; J8-Phase Cal Input

AC Power Cables: P12 Refrigerator AC Power J12; P13 AC power to Elapsed Time Indicator J13; P14 AC drive to Solenoid J14. See Wire List A53213W001, Sheet 8 (TR 11 Appendix page II-27) and 43 GHz FE Block Diagram C53213K002 for connections.

Vacuum Sensor Cables: P15 Pump Vacuum Sense to Pump DV-R6 J15; P16 Dewar Vacuum Sense to Dewar DV-R6 J16. See Wire List A53213W001, Sheet 7 (TR 11 Appendix page II-26) and 43 GHz FE Block Diagram C53213K002 for connections.

* Although VLBA Front-End manuals typically designate this pin as Ground, it is not wired in F110; see Wire List Sheet 12, TR 11 Appendix page II-31.

2.3 Front-End Modes and Cryogenics Control States

The F110 Front-End operates in two **Modes**: **Local** (manual) and **CPU** (remote). The mode is manually selected by S1, the Heat, Pump, Off, Load, Cool, CPU manual selector switch on the card cage Control-Monitor panel. When the switch pointer is in the CPU position, the mode is computer-remote; if the pointer is in any other position, the mode is Local-manual. When the switch is in the Local mode, the control computer cannot override the mode switch setting.

In both modes, there are five Cryogenic States selected by either the manual selector switch in the Local mode or by the control computer in the CPU mode. These five states are: Heat, Pump, Off, Load, and Cool. The table below briefly describes the operations performed by the cryogenic components as a function of the Cryogenic State. The three control discretes X, C, and \bar{H} (described in the Monitor Card description) determine the operation of the refrigerator, vacuum valve and pump request drive circuitry in the Control Card (described below).

State	X	C	\bar{H}	Cryogenic Functions
OFF	1	0	1	No refrigerator power, heater power or vacuum pumping.
COOL	1	1	1	Normal cooled operation.
STRESS	1	0	0	COOL with a small added heat load to stress-test the cryogenic system.
HEAT	1	1	0	Fast warm-up of the dewar with 35 watts of heat added. PUMP REQ goes high when dewar vacuum is greater than 10 microns.
PUMP	0	1	0	No refrigerator or heater power. PUMP REQ is high. The vacuum solenoid is open when the manifold pressure is less than the dewar pressure.

In the CPU mode, three computer-commanded X, C, and \bar{H} control discretes from the F117 (VLBA) or the F14 (VLA) control the cryogenic state. \bar{H} is the standard terminology for this term and the bar on top does not imply logic negation. The * suffix denotes a logic negation; thus \bar{H} is true and \bar{H}^* is false.

2.4 Cryogenic Control Equations

From the table above, it would appear that when the X, C and \bar{H} control bits are set to the state appropriate for a desired cryogenic state, the cryogenic functions are automatically activated. This implied automatic activation is not the case; the commanded action will happen only if TA (15 °K stage temperature), VD (dewar vacuum), and VP (pump vacuum) parameters are in ranges appropriate for these actions and the relationship between VD and VP is correct. Control logic equations for these cryogenic functions contain discrete terms which are a function of the parameter level and an associated threshold value. If the parameter is within the specified range, the term is true and is an enabling factor in the activation of the function. If a parameter is outside the specified range, it is false and the term inhibits

the activation of the function. With the exception of the OFF state, which is unconditional, all equation terms must be true to activate the selected action. The + symbol denotes an OR function and the • symbol denotes an AND function. Parenthesis brackets delimit an AND term and a * suffix denotes a logic negation.

When the logic equations are true, they activate the following:

- L — activates a 1/2 W dewar power load to stress-test the refrigerator.
- P — the Pump Request activates the vacuum pump.
- Q — activates a 30 W power load to heat the dewar.
- R — activates refrigerator AC power.
- S — activates the solenoid valve to enable the vacuum pump to reduce dewar pressure.

The equations are:

$$\begin{aligned}
 L &= C \bullet \bar{H} \bullet (TA < 360 \text{ } ^\circ\text{K}) \\
 P &= (C + C \bullet \bar{H} \bullet) \bullet (VD > 3 \mu\text{m}) \\
 Q &= (X \bullet + C \bullet) \bullet \bar{H} \bullet (TA < 360 \text{ } ^\circ\text{K}) \\
 R &= (C \bullet \bar{H} \bullet + C \bullet \bullet \bar{H}) \bullet (VD < 50 \mu\text{m}) \\
 S &= (C + C \bullet \bar{H} \bullet) \bullet \{ (VD > 5 \mu\text{m}) \bullet (VP < VD) \bullet (TA > 30 \text{ } ^\circ\text{K}) + (VD > 50 \mu\text{m}) \bullet (TA > 280 \text{ } ^\circ\text{K}) \}
 \end{aligned}$$

These equations are implemented on the Control Card, schematic D53200S003, described below. The X, C and H control discretes come from the Monitor Card, schematic D53200S005, described below. The TA, VD and VP analog signals come from the Sensor Card, schematic DD53200S002, described below.

2.5 Control Card Description

The Control Card (schematic D53200S003) is installed in slot 7 and implements the cryogenic control logic equations described above. During the following discussion, refer to the reduced copy of this drawing following this text. A description of the implementation of these control equations follows a description of the card inputs and outputs.

The card inputs are the TTL level X, C and \bar{H} control terms from the Monitor Card and the TA, VD and VP analog signals from the Sensor Card. TA is the 15 °K stage dewar temperature, VD is dewar vacuum and VP is the pump vacuum.

The card outputs are P, the pump request discrete, and 150 VAC power to the refrigerator, vacuum solenoid, 760 Ω dewar heater resistor and the 5 kΩ dewar heater limiting resistor. The AC power outputs are switched by relays K1 through K5. During the following discussion refer to Figure 1.3.3 on page 22 (in TR 11), which shows the Front-End AC wiring. Note that a PCB track connects the 150 VAC unshifted phase input on pin X (designated 150V A on the schematic) to pins Y, W and S. Also note that a PCB track connects the 150 VAC shifted phase input on pin U (designated 150V C on the schematic) to pin V. The AC circuitry is described in Section 2.11.

See Block Diagram C53213K002 for the Control Card connections. Wire list A53213W001, Appendix page II-27 (in TR 11), also describes the Control Card wiring connections.

The control equations are implemented in LS-TTL digital logic. The analog signals are threshold-compared and the comparator outputs are compatible with TTL logic. The comparator threshold levels are described below.

Three LM339N analog comparator outputs change state at three preset levels of TA. The U1-1, U1-2 and U1-14 outputs switch states when $T_A > 30\text{ K}$, $T_A > 280\text{ K}$ and $T_A < 360\text{ K}$, respectively.

Three LM339N analog comparator outputs change state at three preset levels of VD. The U2-1, U2-2 and U2-14 outputs switch states when $V_D > 3\mu\text{m}$, $V_D > 5\mu\text{m}$ and $V_D < 50\mu\text{m}$, respectively. One LM339N comparator, U2-13, compares VD with VP and switches high when $V_P < V_D$.

An analog comparator is a form of operational amplifier whose output makes large level changes for small differences in the two input terminals. Typically, one of the inputs, either the + or - input, is connected to a preset reference level. When the other input slightly exceeds or is slightly less than the reference input, the output makes a large change.

The LM339N comparator output is high when the voltage on the negative (-) input is more negative than the voltage on the positive (+) input. Comparators can be either inverting or non-inverting depending upon the choice of inputs for reference level and input signal. U1-14 is an inverting comparator because the + input is connected to a reference voltage and the negative (-) input is connected to the variable signal. The output swings low if the variable signal is more positive than the reference level. The operation is analogous to an inverting operational amplifier. The non-inverting comparator has the - input connected to the reference level and the variable signal is connected to the + input. The output swings high (positive) when the variable signal is more positive than the reference level. The operation is analogous to a non-inverting operational amplifier. U1-1, U1-2, U2-1, U2-2 and U2-14 are non-inverting comparators. U2-13 is a basic comparator because both inputs are variable levels. An LM339 data sheet is included in Section 4.

The comparator outputs have positive feedbacks so that the comparator's switching thresholds exhibit hysteresis. The hysteresis effect (or signal overdrive requirement) requires that the variable analog signal swing past the level that would cause the output to switch if hysteresis were not a factor. The hysteresis property applies to both positive-going and negative-going levels of the variable signal. Hysteresis is often used in analog comparator circuits to eliminate noise-induced switching when the variable level is near the reference level. Low-level noise is generally present in analog signals and comparator hysteresis prevents noise-induced switching in this situation.

TA scaling is $10\text{ mV}/^\circ\text{K}$. The TA comparator reference levels and associated temperatures are: U1-1, $+0.297\text{ V}$ ($29.7\text{ }^\circ\text{K}$); U1-2, $+2.816\text{ V}$ ($282\text{ }^\circ\text{K}$); U1-14, $+3.602\text{ V}$ ($360\text{ }^\circ\text{K}$). The VD comparator reference levels and associated vacuums are: U2-1, $+0.745\text{ V}$ ($3\text{ }\mu\text{m}$); U2-2, $+1.334\text{ V}$ ($5\text{ }\mu\text{m}$) and U2-14, $+4.521\text{ V}$ ($50\text{ }\mu\text{m}$). These vacuum levels are based upon the chart of vacuum monitor voltage versus vacuum on page 13 (in TR 11).

The TA comparator hysteresis values are: U1-1, 50 mV ($5\text{ }^\circ\text{K}$); U1-2, 50 mV ($5\text{ }^\circ\text{K}$), U1-14, 10 mV ($10\text{ }^\circ\text{K}$). The VD comparator hysteresis values are: U2-1, 278 mV ($\approx 1.8\text{ }\mu\text{m}$); U2-2, 350 mV ($\approx 3\text{ }\mu\text{m}$); U2-14, 10 mV ($\approx 0.4\text{ }\mu\text{m}$) and U2-13, 50 mV ($\approx 2\text{ }\mu\text{m}$).

U10, an Analog Devices AD581JH precision voltage reference, provides a $+10\text{ volt}$ DC reference for the comparator reference voltage dividers. Since the load on the AD581 does not vary and the Front-

Ends operate at about 25 °C, the +10 reference is stable within a few millivolts. An AD581 data sheet is included in Section 4.

Refer to the equations above. Examination of the equations shows that the terms $C \bullet \bar{H}^*$ and $C^* \bullet \bar{H}$ are used in four of the five equations. These two terms are formed in OR-gates U6-6 and U6-11 and are combined as required in the equations. Since the X, C, and \bar{H} control discretes are used in all the equations, the yellow CR6 (X), red CR8 (C) and CR9 (\bar{H}) LEDs are provided to make it easier to check the card logic.

The solid-state relays K1, K2, K3 and K4 and their associated LEDs are driven by 75452 dual peripheral drivers. Each driver has a two input AND gate that drives an open-collector, high current sinking capacity output transistor. K1 through K5 are all solid-state relays with an LED input optically coupled to a solid-state AC switch.

L, the 1/2 watt load equation $L = C^* \bullet \bar{H} \bullet (TA < 360K)$, causes a 5 k Ω limiting resistor to be inserted in series with the 760 Ω dewar heater resistor. The resistor is inserted by closing relay K2; K3 is open in this state. (See the Front-End AC wiring schematic on page 22 in TR 11.) The term T3 ($TA < 360^\circ K$) from comparator U1-14 is AND-ed with \bar{H} in U6-4. This is AND-ed with C^* in U7-3 (a 75452) and the output is low when all three terms are high-true. The low-true output sinks current from +15 V through the coil of relay K2 and CR4, a yellow LED (5 k Ω). The relay's output switch connects the lower end of the 5 K Ω resistor to AC low.

Q, the dewar heater equation $Q = (X^* + C^*) \bullet \bar{H} \bullet (TA < 360K)$, uses the $T3 \bullet \bar{H}$ product from U6-6. It is AND-ed with $X^* + C^*$ from U11-1 in gate U8-5 (a 75452). The output is low-true when all three terms are high-true and sinks current from +15 V through the LED of relay K3 and the red LED (HEATER), CR3. K3's output applies 150 VAC to the 760 Ω dewar heater resistor.

P is the pump request equation $P = (C + C^* \bullet \bar{H}) \bullet (VD > 3\mu m)$. AND gate U6-3 uses the $C + C^* \bullet \bar{H}$ term from U5-3 (mentioned above) and the V1 term from comparator U2-1 ($VD > 3\mu m$). The output is high-true if both input terms are high-true. This P (pump request) output goes to the auxiliary connector pin J4-3 to drive an external vacuum pump control circuit. It is also connected to the monitor connector J2-21 to enable the monitor and control system to read the P state. CR7 (PUMP), a yellow LED, sinks current through inverter U3-2 from +5 volts when P is high.

R, the refrigerator power equation $R = (C \bullet \bar{H}^* + C^* \bullet \bar{H}) \bullet (VD < 50\mu m)$, uses the $(C \bullet \bar{H}^* + C^* \bullet \bar{H})$ term from U5-6 (described above). This term is inverted to low-true by U3-8, which drives a 74LS32 gate U5-8. In this application, the 74LS32 functions as a low-true AND. The U5-8 output is low-true only if both inputs are low. V3, $VD > 50\mu m$ is the other U5 input. This term is high when $VD > 50\mu m$ and low when $VD < 50\mu m$. Thus the U5-8 output is low when $(C \bullet \bar{H}^* + C^* \bullet \bar{H}) \bullet (VD < 50\mu m)$. U8 is a 75452. The pin 1 input is connected to +5 through a 4.7 K Ω resistor so that output U8-3 is high when the equation is true. The U8-3 output sinks current from +15 V through K4's LED and a 750 Ω resistor. When K5 is actuated, it connects the 150 VAC return (or common) to the refrigerator. Note from the block diagram above that card pin X is connected to 150 VAC, Phase 1, the unshifted phase. This line drives a rectifier-divider-filter circuit consisting of CR2 (1N4007), R35 (10k Ω), R36 (1k Ω) and C9 (100 μF). When the 150 VAC, Phase 1 power is present at the filter input, C9 charges to about 19.3 volts. Note that K4's contacts are connected to the junction of the 10 k Ω and 1 k Ω resistors and to the low side of the capacitor so that when K4 is actuated, the filter input is shorted. When the equation is true, K4

is not actuated, its contacts are open, and the capacitor is charged to about 19 volts. This DC voltage drives K5's LED, which closes its output contacts to pass the 150 VAC return (or common) to the refrigerator. Section 4 has data sheets for the 75452 and the relays.

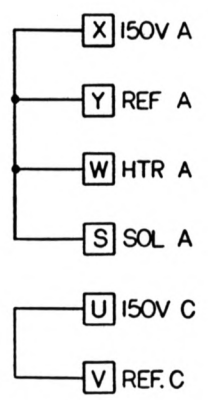
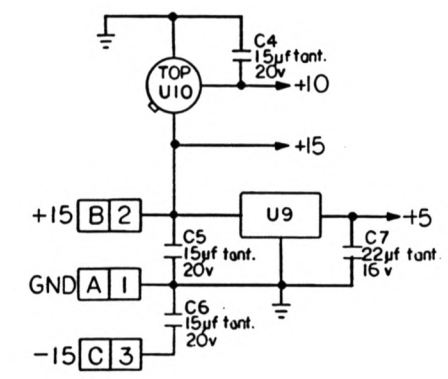
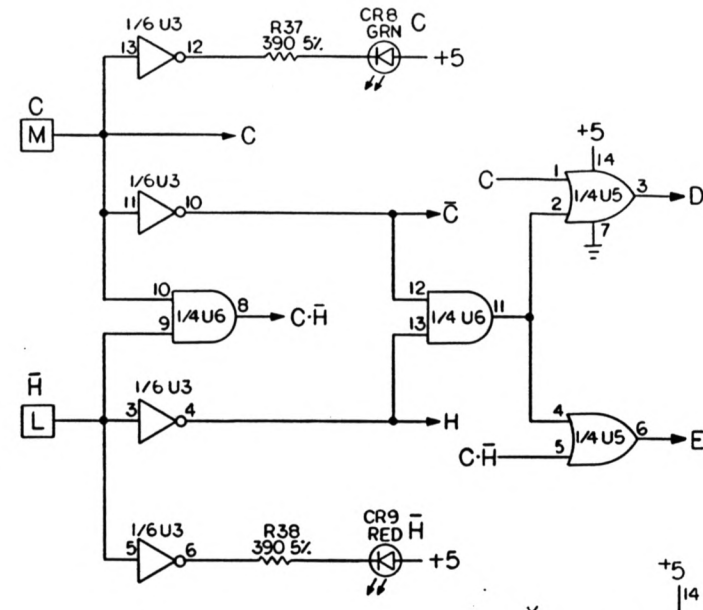
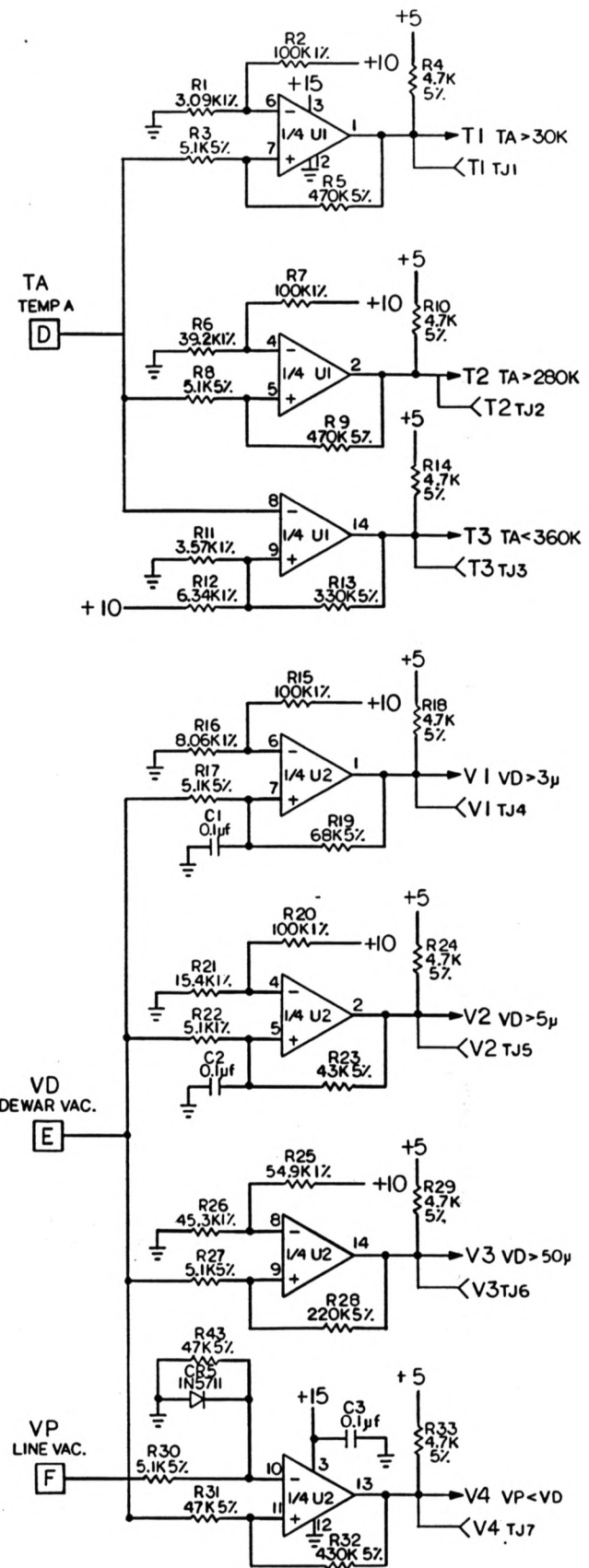
S, the solenoid equation, is the most complicated and is the OR sum of two sets of AND products. $S = (C + C \cdot H) \bullet \{ (VD > 5\mu m) \bullet (VP < VD) \bullet (TA > 30K) + (VD > 50\mu m) \bullet (TA > 280K) \}$. The term D ($C + C \cdot H$) is common to both products. Consider the first set of products. The first term, $C + C \cdot H$, is formed by U5-3. The second term, V2 ($VD > 5\mu m$), is the output of comparator U2-1. The third term, V4 ($VP < VD$), is the output of comparator U2-13. The fourth term T1, ($TA > 30^\circ K$), is the output of comparator U1-1. ($VD > 5\mu m$), ($VP < VD$) and ($TA > 30^\circ K$) are AND-ed in gate U4-6. The output is ORR-ed in gate U5-11, a 75452 driver, with the second product. The second product is formed in U4-12, which has the inputs V3 ($VD > 50\mu m$) and T2 ($TA > 280^\circ K$). The U5-11 output drives one input on U7-5. The other input is the D ($C + C \cdot H$) term from U5-3. U7-5 sinks current through K1's LED and CR1 (SOL), a yellow LED. The SMON term, a monitor discrete, is formed in gate U4-8 by the output of U5-11 and D. The Solenoid valve is an inductive device and if it does not actuate, the solenoid's AC current demand can be as high as 0.40 amperes. To protect K1 from current-induced voltage surges, an MOV and series RC circuit are connected across K1's output. The MOV clips voltage peaks and the RC circuit provides additional surge protection to K1.

For convenience in maintenance, the card LEDs mentioned above and circuit level test jacks are placed on the card edge for easy access. LED and test jack labels are silkscreened on the card. See the card assembly drawing D53200A004 for the locations.

The card's +5 volt logic power is derived from +15 volt power by U9, a MC7805, 5-volt DC regulator.

Control Card Alignment

The Control Card does not have any alignment adjustments. There is not a Control Card tester or formal card alignment procedure but the circuit operations can be evaluated using the card's maintenance features, the Monitor Panel DVM and the Monitor Panel State Select switch, S1. The levels of four analog signals, TA ($15^\circ K$), VD, VP and ACI (AC current load), can be measured using the DVM. The states of the comparator outputs (via card test jacks) can be related to these analog signal levels. LEDs on the X, C and H control discretes enable verification of the control inputs from the Monitor Card. LEDs on the outputs of the five equation's logic circuits indicate the state of the equation's logic output. The Monitor Panel's State switch S1 can be set to select any of the five possible manual-mode states. This will cause the X, C and H states to activate the logic equations as described above. In most cases, the card circuitry can be evaluated by selecting a cryogenic state, noting the TA, VD, VP, and ACI analog levels, the associated comparator outputs, and the response of the solenoid, the refrigerator, vacuum pump, dewar heater, and 1/2 watt load to these signal levels and control states.



CONTROL LOGIC*

L=1/2 W Load
P=Pump Request
Q=Heater 30 W
R=Refrigerator PWR
S=Valve Open (Sol. On)

$= \bar{C} \cdot H \cdot (TA < 360K)$
 $= (C + \bar{C} \cdot H) \cdot (VD > 3\mu)$
 $= (\bar{X} + \bar{C}) \cdot H \cdot (TA < 360K)$
 $= (C \cdot H + \bar{C} \cdot H) \cdot (VD < 50\mu)$
 $S = (C + \bar{C} \cdot H) \cdot (VD > 5\mu) \cdot (VP < VD) \cdot (TA > 30K) + (VD > 50\mu) \cdot (TA > 280K)$

NOTES

- U1-U2 - LM339N
- U3-74LS04
- U4-74LS11
- U5-74LS32
- U6-74LS08
- U7-U8-75452
- U9-7805CT
- U10-AD581JH
- ALL CAPS. ARE 50V UNLESS OTHERWISE MARKED.
- ALL RES. AS FOLLOWS:
1% 1/8WATT
5% 1/4WATT
- K1-K3-645-2
- U11-74LS02
- K4-643-1
- K5-MP240D4

CONTROL STATES*

STATE	CONTROL BIT			OCTAL VALUE	SYSTEM MODE
	X	C	H		
COOL	1	1	1	7	NORMAL
LOAD	1	0	0	4	1/2 W LOAD
OFF	1	0	1	5	NO COOL, HEAT OR PUMP
PUMP	0	1	0	2	PUMP ONLY
HEAT	1	1	0	6	PUMP AND HEAT (30W)
UNUSED	0	0	0	0	LOAD
UNUSED	0	0	1	1	OFF
UNUSED	0	1	1	3	COOL

*TTL LOGIC 1=ON =HI LEVEL
0=OFF=LO LEVEL

REV	DATE	DRAWN BY	APPROVED BY	DESCRIPTION
1	4-87	W. WINTER		ADDED TO NOTES:
2	1-88	G. MOERIS		CO-260130-06
3	8-88	G. MOERIS		
4	8-88	H. DILL		CO-840817-20
5	8-88	S. WEINREB		
6	8-88	S. WEINREB		
7	8-88	S. WEINREB		
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99	8-88	S. WEINREB		
100	8-88	S. WEINREB		

2.6 Monitor Card Description

The Monitor Card is installed in Slot 3 and has two functions: mode-state control via S1 (the Monitor Panel Mode-State switch) and its associated logic and local analog monitoring using the Monitor Panel DVM and S2, the Monitor Select Switch. Drawing C53200S005 shows the Monitor Card circuitry. Section 4 contains a data sheet for the DVM, a Texmate PM-45XU 4½ digit panel meter.

The Monitor Panel is attached to the Monitor Card so that the card and panel are a single assembly. Figure 1 shows the Monitor Panel.

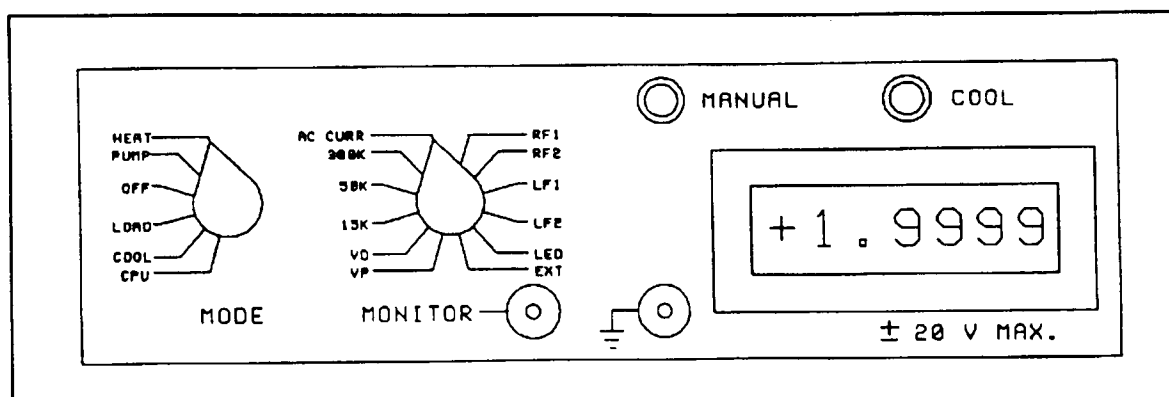


Figure 1 Monitor Panel

See Block Diagram C53213K002 for the Monitor Card connections. Wire list A53213W001, Appendix page II-23 (in TR 11), also describes the Monitor Card wiring connections.

S1, the mode-state selector switch has six positions: HEAT, PUMP, OFF, LOAD, COOL and CPU. When the switch is in the CPU position, the Front-End is controlled by the control computer via F117 (VLBA) or F14 (VLA). In the other five positions, the Front-End cryogenic state is controlled by the setting of S1 as shown in the table in Section 2.3 above.

The Monitor mode-state logic is simple encoding and multiplexing logic. S1, the mode-state switch wiper, is connected to ground. The HEAT, PUMP, OFF, STRESS and COOL contacts are connected to +5 volt pull-up resistors and the inputs of U1, a 74LS148, 8-line to 3-line priority encoder. The sixth position, CPU A0, A1 and A2 outputs are the X, C, and \bar{H} control discretes, respectively. Since S1 has physical stops and the encoder inputs are low-true, the other three encoder inputs can safely float.

The X, C, and H encoder outputs are connected to the B inputs of U2, a 74LS157 quad 2-input multiplexer. The multiplexer A inputs are the X, C, and \bar{H}^* cryogenic state command inputs from the CPU (via F14 or F117). The multiplexer outputs drive the X, C, and \bar{H}^* inputs of the Control Card described in Section 2.5 above. The multiplexer A/B input selection is controlled by S1. When S1 is in the CPU position, the 2 k Ω pull-up resistor to +5 volts causes the multiplexer to select the A inputs; in any of the other five positions, the encoder outputs are selected. The three multiplexer outputs are

connected to the Control Card.

The choice of encoder states is rather important. If through some mischance or malfunction the C and H* bits are stuck high or low, the Control Card will assume either the COOL or LOAD states, the desired default cryogenic states.

Three OR gates in U3, a 74LS32, are used as isolating buffers on the X, C, and \bar{H} lines to J2, the cryogenic state monitor outputs to F117 or F14 via J2. In the event of an inadvertant short on these lines, the buffers protect the X, C, and \bar{H} inputs to the Control Card.

Gate U4-8 decodes the COOL state to sink current from a Monitor Panel red LED, CR2. When S1 is in the CPU position, gate U4-12 sinks current from a Monitor Panel red LED, CR1. The state of U4-12 is output to F117 and F14 via J2.

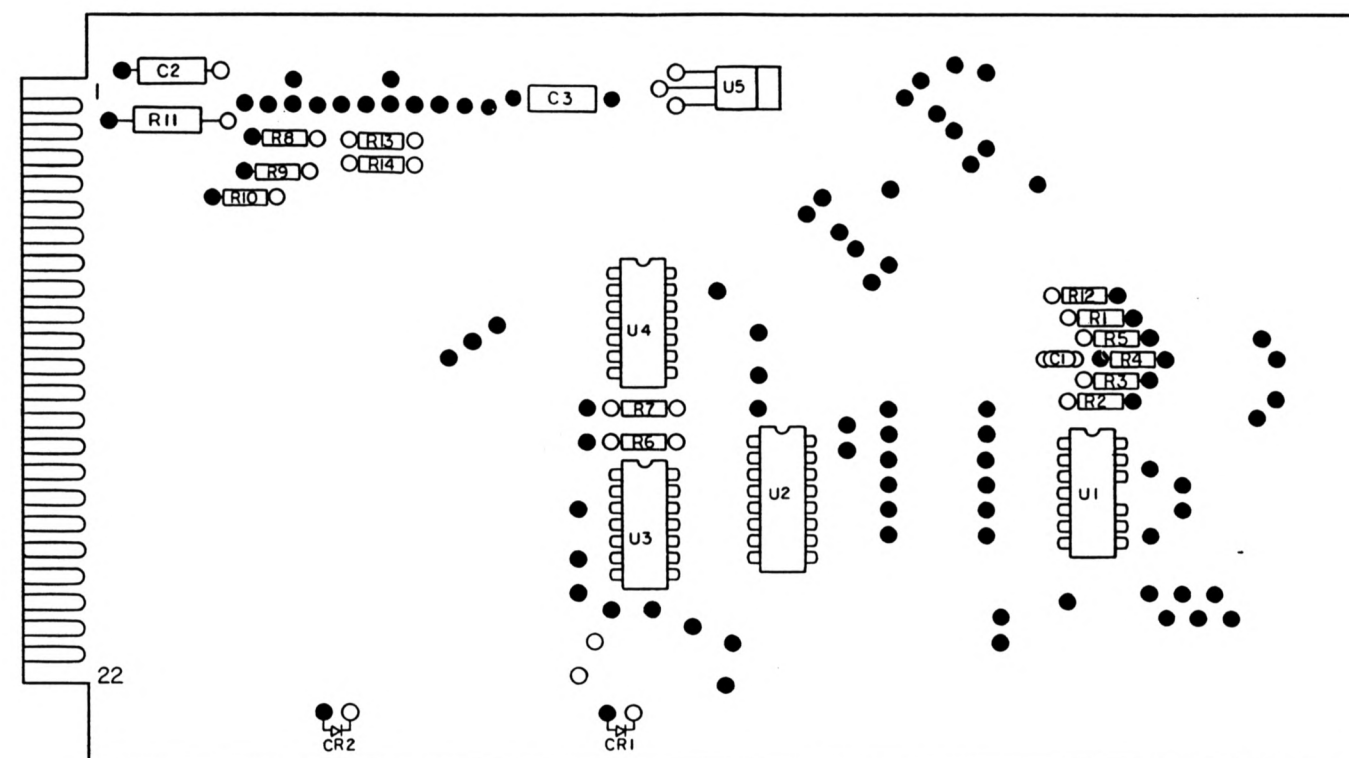
Five volt logic and DVM power is provided by U5, a 7805CT series regulator. Note that the DVM signal ground reference is Quality Ground from J2-13.

The Texmate PM-45-XU has jumper connectors to control its mode and the decimal point is selected by section 1 of the Monitor Select switch, S2. A pair of test jacks on the panel permits an external meter to be connected to the DVM input if there is some question about the DVM values. Since a DVM data sheet is included in Section 4, it is not described here.

Typical values and tolerances for the analog parameters measured by the DVM are described in Section 2.12.

There are no alignment adjustments for the Monitor Card. The card logic is so simple that it can be checked by setting the mode-state switch to the six positions and noting the states of the Monitor Panel LEDs (COOL and MAN) and the Control Card X, C, and H LEDs.

REF. DES.	PART DESCRIPTION	PART NO.	ITEM NO.
C1	CAP 1µf 50V	C330C105M5U5CA	11
C2	CAP 15µf 20V TANT.	CSRI3E156KP	12
C3	CAP 22µf 20V TANT.	CSRI3E226KP	13
CR1	DIODE RED	MU5752	24
CR2	DIODE GREEN	MU64521	24
R1	RES 2K 1/4W 5%	RC07GF202J	2
R2	RES 2K 1/4W 5%	RC07GF202J	6
R3	RES 2K 1/4W 5%	RC07GF202J	8
R4	RES 2K 1/4W 5%	RC07GF202J	8
R5	RES 2K 1/4W 5%	RC07GF202J	8
R6	RES 200 1/2W 5%	RC20GF201J	7
R7	RES 200 1/2W 5%	RC20GF201J	7
R8	RES 1M 1/4W 5%	RC07GF105J	4
R9	RES 1M 1/4W 5%	RC07GF105J	4
R10	RES 1M 1/4W 5%	RC07GF105J	4
R11	RES 30 1W 5%	RC32GF300J	6
R12	RES 2K 1/4W 5%	RC07GF202J	8
U1	IC 74LS148	SN74LS148N	15
U2	IC 74LS157	SN74LS157N	16
U3	IC 74LS32	SN74LS32N	17
U4	IC 74LS12	SN74LS12N	18
U5	VOLTAGE REG 5V	7805CT	14
R13	RES 1M 1/4W 5%	RC07GF105J	4
R14	RES 1M 1/4W 5%	RC07GF105J	4



COMPONENT SIDE

NOTES: HOLES THAT ARE SHADED TO
BE PLATED THRU.

DRILL DWG. D53200P004
SCH. DWG. C53200S005

A 1/16" (1/16") A'ED ITEM NOS
REV DATE BY DESCRIPTION

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NATIONAL RADIO
ASTRONOMY
OBSERVATORY

CHARLOTTEVILLE, VA 22901

DRAWN BY G. MORRIS DATE 8-6-85

DESIGNED BY S. WENGER DATE

APPROVED BY DATE

SHEET NUMBER DRAWING NUMBER D53200A006 REV A SCALE 2X

2.7 Sensor Card Description

The Sensor Card, slot 6, contains the interface circuitry for two Teledyne-Hastings DV-6R vacuum gauges and two Lake Shore DT-500-KL diode temperature sensors. The vacuum gauges sense dewar vacuum (VD) and the pump or manifold vacuum (VP) and the two diodes sense the 15 °K (TA) and 50 °K (TB) dewar temperature stages.

The conditioned VD, VP, and TA outputs of the Sensor Card are connected to the Control Card, slot 7, for use in controlling the Front-End's cryogenic states. They are also connected to the Monitor Card for local monitor readout on the DVM and to J2 for readout by the Monitor and Control System. A non-linear form of TA is also connected to J2 for Monitor and Control System readout. This signal has a higher sensitivity and potentially greater accuracy because it is not subjected to linearizing corrections. TB is not used by the Control Card but is connected to the Monitor Card for DVM readout and is also connected to J2 for Monitor and Control System readout. See Block Diagram C53213K002 for the Sensor Card connections. Wire list A53213W001, Appendix page II-26 (in TR 11), also describes the Sensor Card wiring connections. The Sensor Card schematic is D53200S002 and the assembly drawing is D53200A003.

Teledyne-Hastings DV-6R Vacuum Gauges

The Hastings DV-6R vacuum gauge is a ruggedized, precision vacuum sensing gauge with a specified range of 0 to 1000 μm of Hg (sea-level atmospheric pressure is 760,000 μm of Hg.). The DV-6R is a thermopile consisting of three identical noble-metal alloy thermocouples; see Figure 2 which shows the sensor and its connections to the VD interface amplifier. The + symbol indicates the thermal EMF polarity. The thermocouple alloys are Gold/Platinum and Platinum/Rhodium. All three thermocouples sense the gas pressure and the - (negative thermal EMF polarity) sides of all three are connected to DV-6R pin 8, which is simply a tie-point that is not connected to any external circuitry. The + sides of two thermocouples are connected to pins 3 and 5 and are heated by the AC excitation. The + side of the third thermocouple is connected to pin 7, is not heated by the AC excitation, and is analogous to the reference junction in a conventional thermocouple circuit. The thermal EMF of this third thermocouple is determined by the temperature of the sensed gas, is very small, and its polarity is in opposition to the thermal EMF of the heated thermocouples.

The vacuum-sensing properties of the DV-6R are a function of the sensed air's thermal conductivity, which decreases when the air pressure is decreased. A decreasing thermal conductivity increases the hot junction's temperatures, which increases the thermopile DC output. At a high vacuum, the hot junction temperature is about 300 °C. In the dewar and manifold vacuum-sensing applications, the DV-6R sensitivity is determined by the AC heating power delivered to the thermocouple junction; the Sensor Card VD ZERO and VP ZERO adjustments determine this power level. Hastings does not have an explicit

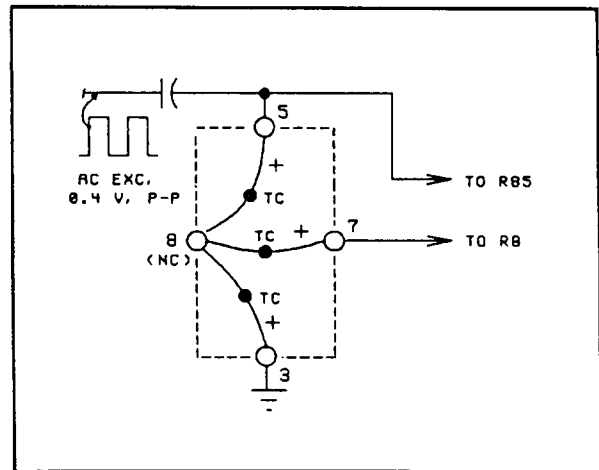


Figure 2 DV-6R Connections

mathematical expression for DC output as a function of the sensed air pressure but the DV-6R's output is roughly a logarithmic function of pressure. Hastings states that the DV-6R accuracy is about $\pm 2\%$ at a high vacuum ($\approx 1\ \mu\text{m}$).

Page 13 (in TR 11) shows a graph of the Sensor Card vacuum interface circuit readout voltage versus dewar pressure. At a vacuum of $1\ \mu\text{m Hg}$, and with the appropriate AC excitation, the nominal DV-6R sensitivity (output voltage change /vacuum change) is $-161\ \text{mV}/\mu\text{m}$; this is the DV-6R's highest sensitivity. As pressure increases, the sensitivity rapidly decreases. At $1000\ \mu\text{m}$ the interface circuit output is $+9652\ \text{mV}$ and at sea level atmospheric pressure, the interface circuit output is $+10,000\ \text{mV}$. The nominal sensitivity of $-161\ \text{mV}/\mu\text{m}$ at $1\ \mu\text{m}$ is the value used in Sensor Card alignment.

Hastings' vacuum thermopile interface circuit uses a center-tapped transformer secondary that drives pins 3 and 5 with a $0.38\ \text{volt}$, P-P square wave; this heats the two thermocouples connected back-to-back across pins 3 and 5. The primary is driven by a $5\ \text{kHz}$ power oscillator. The thermopile's DC output connections are pin 7 (the + side of the unheated thermocouple) and the transformer center-tap. Relative to pin 7, the heated thermocouple's DC voltages on pins 3 and 5 are identical because the two heated thermocouples are in parallel. Hastings typically connects the DC output to an analog current meter with a $40\ \Omega$ current limiting resistor. The Hastings' interface's meter scale is calibrated for the sensor's working range.

The DV-6R interface circuits are aligned by substituting a Hastings DB-20 reference tube for the DV-6R. The DB-20 simulates the DV-6R at some high vacuum level, typically $2\ \mu\text{m}$. In a recent lab test, a Hastings DB-20 Reference Tube marked $2\ \mu\text{m}$ was substituted for the DV-6R. The DB-20 DC output measured on pin L of the Sensor Card was $-287\ \text{mV}$. Although this was slightly under the expected $322\ \text{mV}$, the Sensor Card circuit aligned normally. The vacuum interface alignment procedure is described below. A Hastings DV-6R data sheet is included in Section 4.

The vacuum gauge interface circuitry is shown on the left half of the Sensor Card schematic drawing, D53200S002. Note that there are three connections to the DV-6R.

Vacuum Gauge Interface Circuitry

The DV-6R vacuum gauges require an AC excitation. An oscillator and two power buffers provide the AC power to drive the thermopiles. The oscillator is U4-8, a TI TL084BCN operational amplifier used in an RC relaxation oscillator circuit. The oscillation results from an alternating sequence of capacitor charge-discharge ramps. One output cycle consists of a capacitor charge period and a capacitor discharge period; therefore the capacitor's voltage waveform is a sawtooth and the oscillator's output is a square wave. The amplifier's negative (-) input is connected to the capacitor-resistor junction. The amplifier's positive (+) input is connected to a center-tapped $48\ \text{k}\Omega$ resistive voltage divider, connected to the amplifier's output; therefore, the amplifier's + input voltage is always half the output voltage. Capacitor C14 is charged (or discharged) through resistor R81 until a switching threshold is reached; at the threshold, the amplifier's output switches to the opposite polarity. This causes the charging current polarity to reverse, so the capacitor begins to discharge (or charge). The TL084's two output levels are the positive and negative saturation limits, about $+13.5$ and $-13.5\ \text{volts}$. The two switching thresholds are the levels at which the voltage difference between the two amplifier inputs is zero. Since the amplifier's + input is connected to the midpoint of the $48\ \text{k}\Omega$ resistive voltage divider, the switching thresholds are $+6.25$ and $-6.25\ \text{volts}$.

The oscillator period is $2.2R_8C_{14}$, which is $52.8 \mu\text{s}$, so the frequency is about 18.9 kHz.

The + input connected to the voltage divider experiences positive feedback, which adds hysteresis to the switching thresholds. This prevents spurious noise-induced switching that might otherwise occur when the differential voltage between the inputs is very small. Low level noise is always present in virtually any analog circuit.

The voltage on the TL084 inputs are ± 6.5 volts above or below ground. This could be a problem in a conventional operational amplifier. The TL084 has JFET-inputs and is capable of operating with a differential input voltage of ± 30 volts and an input voltage of ± 15 volts. Section 4 has a data sheet for the TL084.

The oscillator output is clipped to a ± 6.2 volt square wave by a zenar diode clipping circuit. R79, a $2 \text{ k}\Omega$ resistor, isolates the amplifier from the clipper to prevent clipper overload. A pair of paralleled 1N821, 6.2 volt zenar diodes make a precise + and - 6.2 volt square wave that is nearly independent of temperature. The 1N821 has a temperature coefficient of $0.01 \text{ }^\circ\text{C}$. The 1N823, which may be used as an alternate zenar, has the same zenar voltage but a $0.005\text{ }^\circ\text{C}$ temperature coefficient.

Since there are two vacuum sensors, two independent sets of DV-R6 drivers and conditioning amplifiers are required. The driver circuits are power buffers and the conditioning amplifiers are a differential amplifier driving an inverting amplifier. The Hastings catalog does not specify a resistance value for the thermopile but it's reasonable to assume that it is small, probably less than an ohm. This low resistance requires a low impedance, high current drive.

We first consider the VD power buffer, driven by the clipper circuit described above. The power buffer is U8-1, an inverting operational amplifier with Q1, an emitter-follower power transistor in the feedback loop. The transistor provides the low impedance, high current drive required by the DV-6R.

The DV-6R must be driven by an AC signal. Therefore, the buffer amplifier input and output are both AC-coupled. The input is AC-coupled via C_1 ($0.01 \mu\text{F}$). At 18.9 kHz, C_1 's impedance is about 800Ω , small in comparison to R_7 ($130 \text{ k}\Omega$) and R_3 ($50 \text{ k}\Omega$). The amplifier output drive to the DV-6R is AC-coupled via C_2 , $10 \mu\text{F}$. C_2 's impedance is about 0.8Ω , small in comparison to the DV-6R impedance.

Note that Q1's collector is connected to ground; a 0.3 mA offset current from +10 volts into U8-2, the summing junction, shifts Q1's emitter Q-point to about -3.0 volts. This avoids clipping the DV-6R drive. Diode CR₅ across the transistor base-emitter junction prevents base-emitter reverse voltage protection.

The amplifier gain is controlled by the ratio of feedback to input resistance. The feedback resistor is R_1 , ($10 \text{ k}\Omega$) and the input resistance is R_7 ($130 \text{ k}\Omega$), and R_3 , (a $50 \text{ k}\Omega$ pot). The maximum and minimum gains are 0.076 and 0.055, respectively as a function of R_3 's setting. The clipper output is a 12.4 volt, P-P signal; with these two gain extremes, the corresponding Q1 output is about 0.95 volts P-P, and 0.69 volts, P-P. With R_3 set mid-range, the buffer output is about 0.79 volts P-P. Hastings uses a 0.38 volt drive across pins 5 and 3.

The drive is AC-coupled to the DV-6R pin 5 and the thermopile heating current flows through the two thermocouples to ground via DV-6R pin 3. The 100 pF capacitor across the $10 \text{ k}\Omega$ feedback resistor R_{19} provides some high frequency pre-emphasis.

The DV-6R pin 7 output is amplified by cascaded amplifiers, U5-13 (noninverting) and U6-6 (inverting). The DV-6R thermal EMF output on pins 5 and 7 is a DC output that is connected to the inputs of differential amplifier U6-13. Note from Figure 2 that the two heated thermocouple's thermal EMFs are in opposition, thus pin 5 is actually at DC ground; this was verified in a recent measurement.

The DV-6R's negative polarity, thermal EMF output on pin 7, drives U5-4, the amplifier's noninverting (+) input. Since the noninverting input is driven and the noninverting input is static at DC ground, the amplifier's output signal polarity is the same as the DV-6R pin 7 polarity.

Note that the DV-6R AC excitation is also a normal-mode input to U5-13. The AC level on DV-6R pin 7 is half the AC excitation voltage. The normal-mode component is reduced by resistor R_{86} so that the AC level on U5-3 is also half the excitation level. The normal-mode component of the AC excitation is also reduced by the two amplifier's low-pass filtering.

U5-13's gain is 50, determined by the R_9/R_{85} ratio. The 19.8 kHz AC signal on U5-13's inputs is filtered by capacitor C_4 across U5-13's feedback path. This capacitor in conjunction with R_{84} forms a single-pole, low-pass filter having a -3 dB frequency of about 3 Hz. Inverting amplifier U5-6 has a gain of 10, and capacitor C_8 provides additional AC filtering. U5-6's -3dB frequency is about 32 Hz.

When the pressure is 1 μm , the U5-13's output is - 8.050 volts (50×-0.161). When the air pressure is high, U5-13's output is very small.

The next amplifier stage, U5-6, is an inverting amplifier with a gain of 10. Note that the + input of U5-6 is biased to about +1 volt by the resistive voltage divider to +10 volts. This also causes the - input to be biased to the same +1 volt level. If the U5-13 output is about zero volts, which is the atmospheric pressure level output of the DV-6R, the U5-6 output is +10 volts. If the U5-13 output is - 8.050 volts, the result of a 1 μm pressure in the DV-6R, the U5-6 output is zero volts.

The VD amplifier output may be measured at TJ-5; TJ7 is analog ground. The amplifier's three outputs (MON OUT, METER, and VD) have isolation resistors R_{16} (2 k Ω), R_{17} (10 k Ω) and R_{18} (100 Ω), respectively. The METER OUT signal could be used to drive an analog meter but is not used in F103. The MON OUT is also not used in F103. The VD output is connected to the Control Card (slot 7), the Monitor Card (slot 3), and to J2-2 for readout by the Monitor and Control System.

The VP power buffer (U8-14 and Q2) is similar to the VD power buffer but provides a slightly lower drive for its DV-6R; R_7 in the series attenuator is 200 k Ω . The maximum and minimum drives as a function of the R_7 setting are 0.49 and 0.30 volts, P-P respectively. With R_{21} set mid-range, the AC drive is 0.40 volts, P-P, close to Hastings drive level.

Vacuum Sensor Interface Circuit Alignment

This alignment procedure was abstracted from VLBA Technical Report No. 1.

The two DV-6R interface circuits are aligned by using a Sensor Card Tester. The tester contains a Hastings DB-20 Reference Tube, which simulates the output of a DV-6R at a specified vacuum level, typically 2 to 3 μm , printed on the side of the Reference Tube. The vacuum interface circuitry in the tester has a VD/VP selector switch to connect the DB-20 to either interface circuit and a ZERO/ATMOS toggle switch for the two adjustments. The DV-6R interface circuits have two alignment adjustments, VP

ZERO (or VD ZERO) and VP ATMOS (or VD ATMOS). The VP ZERO adjustment determines the AC drive level to the buffer circuit and the VP ATMOS adjustment determines the DC offset to the U6-6 (or U5-6) output amplifiers. In aligning the card's two DV-6R interface circuits, the tester's ZERO/ATMOS switch is first set to the ZERO position and the card's VP (or VD) ZERO potentiometer is adjusted to produce an output of 161 mV times the DB-20 reference pressure value. The output can be measured at TJ6 (or TJ5) on the tester on the EXT DVM jack or by the Monitor Panel DVM. Next, the ZERO/ATMOS is set to the ATMOS position and the VP (or VD) ATMOS potentiometer is adjusted to produce an output of +10230 mV (about positive full-scale on a 5 mV/LSB, 12-bit A/D converter). In the ATMOS position, the tester presents an open circuit to the interface circuit in place of the DV-6R; this causes the full-scale output. Section 4 contains a Hastings DB-20 data sheet. A field calibration procedure for the DV-6R vacuum sensors is included in the Appendix, Section 5.

DT-500 Temperature Sense Diodes, TSA and TSB

The temperatures of the dewar 15 °K and 50 °K stations is sensed by two Lake Shore DT-500-KL diode temperature sensors, TSA and TSB. The 15 °K stage conditioned signal is TA and TB is the 50 °K stage conditioned signal. Section 4 contains a data sheet for a similar Lake Shore diode temperature sensor. The 300 °K temperature is measured by a National Semiconductor LM335 chip and is described in the RF Card description, Section 2.9, below. Figure 2, on the next page, shows a plot of the DT-500 diode voltage vs. temperature. This plot was abstracted from NRAO EDIR Report No. 204, May 1980 by Michael Balister.

The diode's characteristics are determined by the diode equation: $I_F = I_S (e^{\frac{qV}{kT}} - 1)$. I_F is the diode forward current and I_S is the reverse-bias saturation current. Constants are: I_S , e , the electronic charge, and k , Boltzman's constant. Variables are I_F , V , the diode voltage, and T , the diode temperature, °K. If I_F is maintained at a constant value, there are only two variables, V and T . By using a suitable conversion table and holding I_F at a constant value, T may be determined by measuring V . Note from the Lake Shore data sheets that if I_F is 10 μ A, V is 1.345 volts at 13 °K and 0.519 volts at 300 °K.

Diode Interface Circuitry

Block Diagram C53213K002 shows the TSA and TSB diode wiring connections to the Sensor Card, which has two identical temperature interface circuits. The diode anodes are connected to analog ground (pins E and F) and the cathodes are connected to the current sources and temperature sense interface circuit inputs (pins 4 and H). The TA and TB diode interface circuits are shown in the right half of Schematic diagram D53200S002.

Implementation of a two-segment linearization circuit is suggested by the character of the DT-500 thermal response curve shown in Figure 3. The Sensor Card's diode interface circuitry is an adaptation of the design described in EDIR No. 204.¹

Consider the TA circuit. Transistor Q3 and associated components are the 10 μ A current sources for TSA. The base of Q3 is held at -8.8 volts by zenar diode CR₁ ($V_Z = 6.2$ volts). Q3's collector current is determined by V_{CE} and the resistance between the emitter and -15 volts. Potentiometer R₃₉ adjusts the

¹ Page 37, VLBA TECHNICAL REPORT NO. 1, August 29, 1984

diode current to the 10 μ A value.

Noninverting, unity-gain voltage followers U1-1 and U2-1 isolate the diode's current source circuitry from the linearization circuitry. Since they simply buffer the diode's voltage, the amplifier's outputs are a nonlinear function of temperature. The TSA signal is connected to its linearization circuitry and to J2-14 for readout by the Monitor and Control System. R_{87} , a 1 k Ω resistor, isolates the TA amplifier from the test point terminal TP1 and the nonlinear TA output on pin S. The nonlinear form of TA is not used by the Control Card and is not available to the Monitor Card DVM. The nonlinear TSB signal is only used by the TB linearization circuitry.

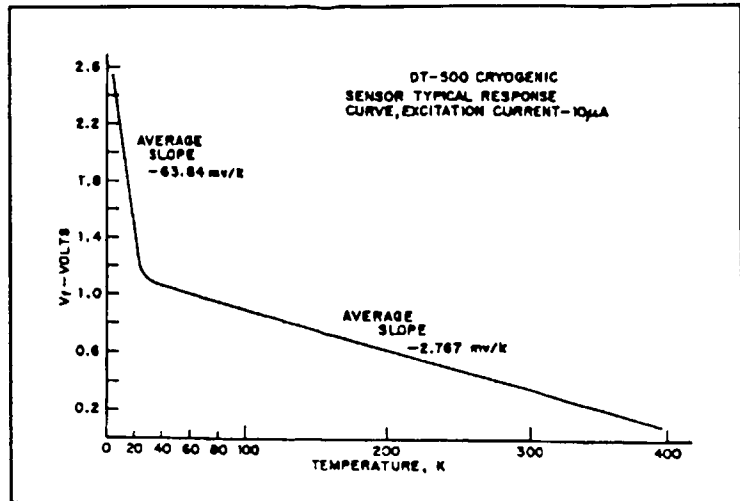


Figure 3 DT-500 Sensor Temperature Response

Note from the Lake Shore data sheets in Section 4 that at 13 $^{\circ}$ K, the nonlinear TA signal has a sensitivity (slope) of 21.9 mV/ $^{\circ}$ K. The sensitivity decreases to 15.9 mV/ $^{\circ}$ K at 24 $^{\circ}$ K. In this 11 degree region, the nonlinear TSA signal is more sensitive than the linearized TA and TB signals, which have a sensitivity of 10 mV/ $^{\circ}$ K. In addition, in this region the nonlinear TA is more accurate than the linearized TA because the linearized signals are segmented approximations to the diode curve.

The TA and TB linearization circuitry approximates the diode's V versus T curve with two straight-line segment approximations, only one of which is operative at any given time. When the sensed temperature changes from one segment's range to the other segment's range, it crosses a segment transition temperature which causes the other segment's output signal to be selected for output. The segment amplifier's gains and offsets are adjusted for the best fit for its portion of the diode's V-T curve. The segment transition temperature is 27 $^{\circ}$ K. The linearized TA and TB signals can be adjusted to be in exact agreement with the diode V-T curves at 13, 18, 50 and 300 $^{\circ}$ K. Since TSB monitors the 50 $^{\circ}$ K stage, the lower temperature segment is never operative.

The linearization implementation consists of two independent segment gain paths with gain and offset adjustments appropriate for the segment, a segment signal level comparator, and a segment selector switch driven by the comparator.

The TA and TB linearization circuits are identical.

In each circuit both paths are driven by the input, unity-gain voltage follower, U1-1 or U2-1. The circuitry consists of two parallel-path independent, inverting operational amplifiers with different gains, an analog comparator that compares the two amplifier's outputs, an analog switch driven by the comparator that selects the most appropriate amplifier for output, and an inverting output amplifier.

Note from the schematic that one TA path is a HI GAIN path used for the higher temperature segment and the other path is the LO GAIN path used for the lower temperature segment. From the

paragraph above describing the nonlinear TA signal, note that in the 13 to 24°K range, the diode's sensitivity is greater than 10 mV/°K so the lower segment amplifier's gain must be less than 1. Also note that for temperatures greater than 25 degrees, the upper segment amplifier's gain must be greater than 1. 20 k Ω gain control potentiometers R₄₃ and R₄₄ control the gain of the two TA amplifiers U1-7 and U1-8. For extreme settings of these two potentiometers, the resultant gains are: 4.02 and 3.29, HI GAIN and 0.21 and 0.16, LO GAIN.

Both amplifiers use an offset current from an Analog Devices, AD581JH precision +10.000 reference voltage source. This chip was described in the Control Card description, Section 2.5. Potentiometers R₄₀ and R₄₇, 100 k Ω , and 50 k Ω , respectively, are the offset current adjustments.

Comparator U3-1, a National Semiconductor LM393AN, compares the levels of the high and low gain amplifiers. If the HI GAIN level on the negative input (-) is more positive than the LO GAIN positive input (+), the output is low. In the converse case, the output is high. The comparator output is an open-collector transistor; a 22 k Ω pull-up resistor to +15 makes the output levels 0 and +15 volts. The LM393 features a very low input offset, typically 1 mV, important in this application.

U4 is an Analog Devices AD7512DIKN, dual-channel analog switch that selects either the HI GAIN signal or the LO GAIN signal as a function of the address (select control) input, pin 4. If pin 4 is high, the HI GAIN amplifier input on pin 9 is connected to the output, pin 10; if low, the LO GAIN signal on pin 11 is connected to the output. R₇₄ provides isolation from the comparator for the control input and diode CR4 protects it in the event of a negative control input. The AD7512 features a low "ON" resistance, 75 Ω , and low leakage currents. Section 4 contains an AD7512DI data sheet.

Unity-gain, inverting amplifier U1-14 provides output buffering for the TA output on card pin D. R₅₆, a 100 Ω resistor, provides short-circuit protection for this output. The EXT MON output on pin 6 is not used in F110.

0.47 μ F Capacitors across the operational amplifiers provide low-frequency filtering of the temperature signals.

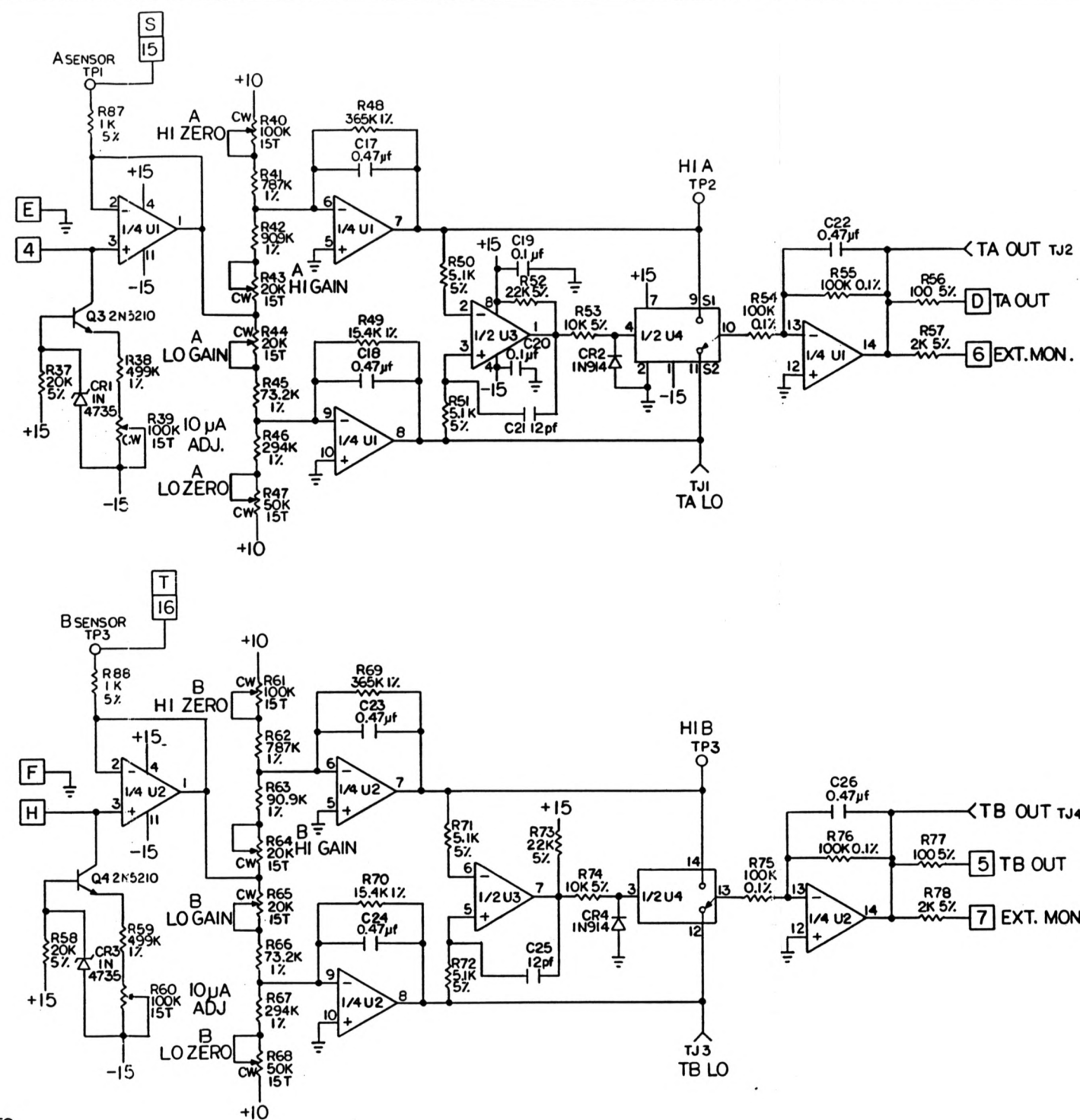
TJ1 and TJ3 enable measurement of the LO GAIN amplifier outputs and TJ2 and TJ4 enable measurement of the TA and TB outputs, respectively. TP2 and TP3 terminals enable measurement of the HI GAIN amplifier's outputs.

The Sensor Card Tester uses potentiometers and a buffer amplifier simulates the diode temperature sensors. Using this tester, the TA and TB interface circuits are aligned as follows:

1. Set the DVM switch to TA.
2. Set the Mode switch to A-10 μ A and adjust the A-10 μ A potentiometer for a reading of 1000 on the DVM.
3. Set the MODE switch to TA/TB and the TEMP switch to SHORT and adjust the TA HI GAIN potentiometer for 4350 mV on the DVM. Adjust the TA LO GAIN potentiometer for 445 mV, on the A LO GAIN test terminal, read by an external DVM.
4. Set the TEMP switch at 50 and adjust the TA HI GAIN potentiometer for 500 mV on the tester DVM.
5. Set the TEMP switch at 300 and readjust the TA HI GAIN potentiometer for a reading of 3000 mV on the tester DVM. Repeat steps 4 and 5 until 500 mV and 3000 mV readings are

obtained.

6. Set the TEMP switch at 13 and adjust the TA LO GAIN potentiometer for 130 mV on the tester DVM.
7. Set the TEMP switch at 18 and readjust the TA LO GAIN potentiometer for 180 mV on the tester DVM. Repeat steps 6 and 7 until 130 mV and 180 mV readings are obtained.
8. Repeat steps 1 through 7 for the TB circuit.



C	1-86	G. MOERIS		CO 860130-07
B	11-85	G. MOERIS		
A	8/84	H. DILL		CO-840817-20
REV.	DATE	DRAWN BY	APPROV'D BY	DESCRIPTION
V O A	FRONT ENDS			NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTEVILLE, VA. 22904 DRAWN BY H. DILL DATE 8/87 DESIGNED BY S. WEINREB DATE 8/86 APPROVED BY DATE
SENSOR CARD				
SHEET		of	OF THIS DRAWING	REV. C SCALE

8

7

6

5

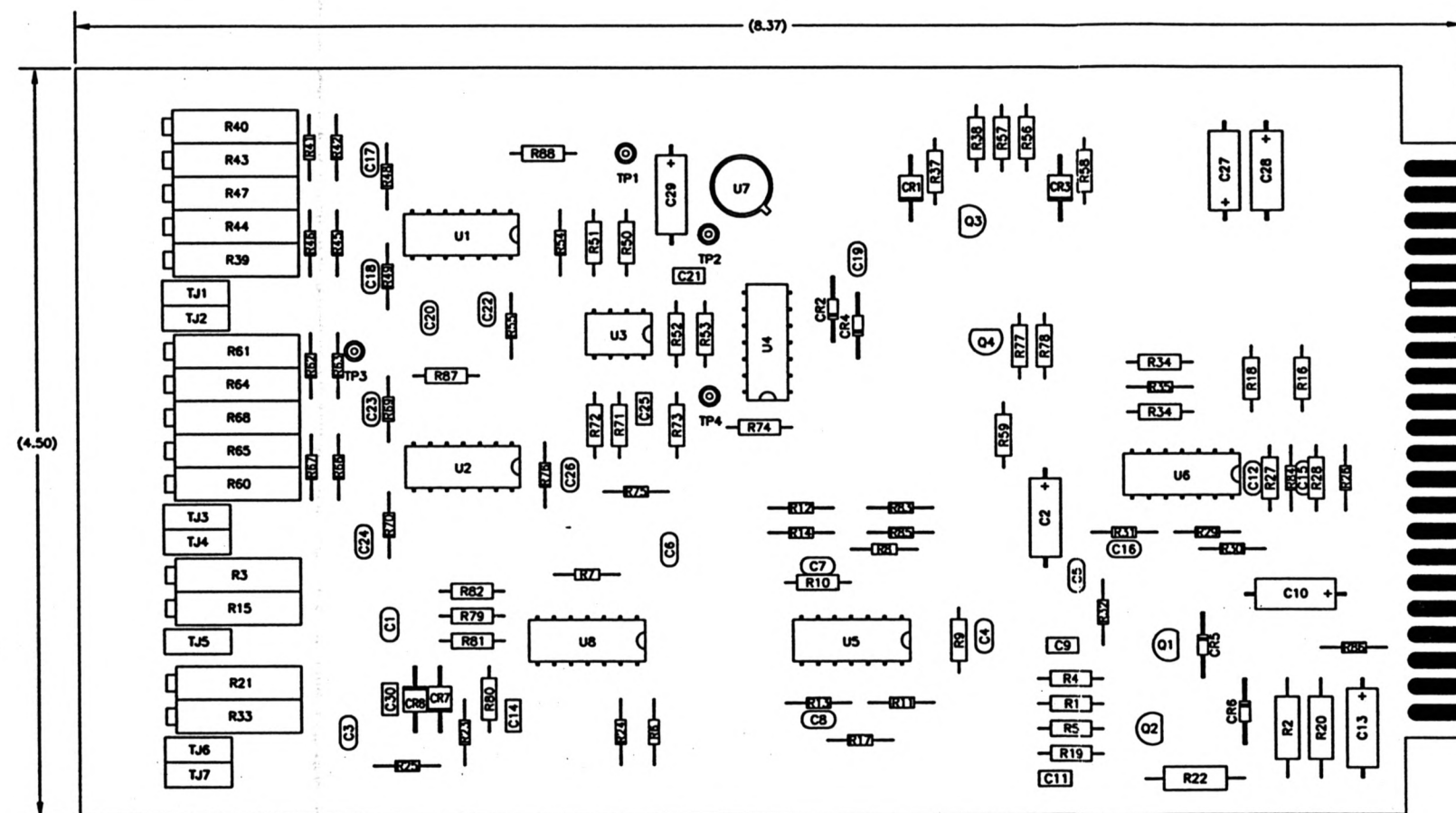
4

3

2

1

REV	DATE	DRAWN BY	APPRVD BY	DESCRIPTION
B	1-87	WIREMAN		ADD TEMP SENSOR HOLES
C	2-87	MORRIS		CHG ORDER 870218-5
D	8-94	TATE	PETENCIN	REVISED AND REDRAWN



CIRCUIT BOARD

COMPONENT SIDE

ACAD : 53200A03

D53200S002	SCHEMATIC
D53200Q002	ARTWORK
D53200P002	DRILL DWG
D53200I013	SILKSCREEN
D53200I007	SOLDER MASK
NEXT ASSEMBLY	DWG. TYPE

57	U3	AUGAT	608-CG1	SOCKET, 8-PIN	1
56	U4	AUGAT	614-CG1	SOCKET, 14-PIN	7
55	U7	ADI	AD581JH	IC, 14-PIN	1
54	U5,U6	PMI	OP10CY	IC, 14-PIN	2
53	U4	ADI	AD7512DIKN	IC, 14-PIN	1
52	U3	MOTOROLA	LM393N	IC, 8-PIN	1
51	U1,U2	TI	TL084CN	IC, 14-PIN	3
50	TF-TP4	KEYSTONE	1562-2	TURRET, TEST POINT	4
49	TJ7			TEST JACK, BLACK	1
48	TJ6			TEST JACK, GREEN	1
47	TJ5			TEST JACK, GRAY	1
46	TJ3			TEST JACK, ORANGE	1
45	TJ2			TEST JACK, RED	1
44	TJ1,TJ3			TEST JACK, WHITE	2
43	R80-R82	ALLEN-BRADLEY	RC07GF243J	RESISTOR,24K,1/4W,5%	3
42	R54,R55	DALE	RN55C1003F	RESISTOR,100K,1/8W,1%	4
41	R52,R73	ALLEN-BRADLEY	RC07GF223J	RESISTOR,22K,1/4W,5%	2
40	R50,R51	ALLEN-BRADLEY	RC07GH512J	RESISTOR,5.1K,1/4W,5%	4
39	R49,R70	DALE	RN55C1542F	RESISTOR,15.4K,1/8W,2%	2
38	R48,R69	DALE	RN55C3653F	RESISTOR,356K,1/8W,1%	2
37	R46,R67	DALE	RN55C2943F	RESISTOR,294K,1/8W,1%	2
36	R45,R66	DALE	RN55C7322F	RESISTOR,73.2,1/8W,1%	2
35	R43,R44	CEMET	3006P 20K	TRIM POT,20K,15T	4
34	R42,R63	DALE	RN55C9092F	RESISTOR,90.9K,1/8W,1%	2
33	R41,R62	DALE	RN55C7873F	RESISTOR,787K,1/8W,1%	2
32	R39,R40	CEMET	3006P 100K	TRIM POT,100K,15T	4
31	R37,R58	ALLEN-BRADLEY	RC07GF203K	RESISTOR,20K,1/4W,5%	2
30	R25	DALE	RN55C2003F	RESISTOR,200K,1/8W,1%	1
29	R22	ALLEN-BRADLEY	RC20GF680J	RESISTOR,68,1/2W,5%	1
28	R18,R19	ALLEN-BRADLEY	RC07GF101J	RESISTOR,100,1/4W,5%	4
27	R17,R20,R35	DALE	RNC55C1002F	RESISTOR,10K,1/8W,1%	7
26	R16,R33,R57	ALLEN-BRADLEY	RC07GF202J	RESISTOR,2K,1/4W,5%	5
25	R15,R33	CEMET	3006P 5K	TRIM POT,5K,15T	2
24	R14,R32	DALE	RN55C4752F	RESISTOR,47.5K,1/8W,1%	2
23	R13,R31	DALE	RN55C4992F	RESISTOR,49.9K,1/8W,1%	2
22	R11,R12,R30	DALE	RN60D4993F	RESISTOR,499K,1/4W,1%	6
21	R10,R17,R30	DALE	RN55C4991F	RESISTOR,4.99K,1/8W,1%	6
20	R7	DALE	RN55C1303F	RESISTOR,130K,1/8W,1%	1
19	R5,R24	DALE	RN55C3322F	RESISTOR,3.2K,1/8W,1%	2
18	R4,R5	ALLEN-BRADLEY	RC07GF102J	RESISTOR,1K,1/4W,5%	4
17	R3,R6	CEMET	3006P 50K	TRIM POT,50K,15T	4
16	R2,R20	ALLEN-BRADLEY	RC20GF201J	RESISTOR,200,1/2W,5%	2
15	R19,R21	ALLEN-BRADLEY	RC07GF103J	RESISTOR,10K,1/4W,5%	4
14	Q3,Q4	MOTOROLA	2N5210	TRANSISTOR, NPN	2
13	Q1,Q2	MOTOROLA	2N3904	TRANSISTOR, NPN	2
12	CR7,CR8	AMD	1N821	DIODE	2
11	CR4,CR6	AMD	1N914	DIODE	4
10	CR1,CR3	MOTOROLA	1N4735	DIODE	2
9	C21,C25	KEMET	CK05BX120K	CAPACITOR,12pf,50V	2
8	C14,C30	KEMET	CK05BX102K	CAPACITOR,.001uf,50V	2
7	C13,C27-C29	MALLORY	CSR13E156KP	CAPACITOR,TANT,.15uf,20V	4
6	C9,C11	KEMET	CK05BX101K	CAPACITOR,100pf,50V	2
5	C15,C16,C20	KEMET	C330C104M5U5CA	CAPACITOR,.1uf,50V	6
4	C17,C18,C20	KEMET	C330C474M5U5CA	CAPACITOR,.47uf,50V	10
3	C2,C10	MALLORY	CSR13E106KP	CAPACITOR,TANT,.10uf,20V	2
2	C1,C3	KEMET	C330C103M5U5CA	CAPACITOR,.01uf,50V	2
1		NRAO	D53200Q002	BOARD, CIRCUIT	1

ITEM NO.	REF.	DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES						
TOLERANCES : INCHES :						
3 PLACE DECIMALS (MAX) : .005						
2 PLACE DECIMALS (MAX) :						
1 PLACE DECIMALS (MAX) :						
MATERIAL :						
FINISH :						
SHEET NUMBER 1 of 1						
DRAWING NUMBER D53200A003						
REV. D						
SCALE 2/1						

COMMON FRONT END

FRONT END
SENSOR PCB
ASSEMBLYNATIONAL RADIO
ASTRONOMY
OBSERVATORY
SOCORRO, NEW MEXICO 87801DRAWN BY H. DILL
DESIGNED BY S. WEINREB
APPROVED BY S. WEINREB
DATE 9-85
DATE 9-85
DATE 9-85

2.8 FET Bias Card Description

The dewar RCP and LCP amplifiers each use five HEMT (high electron mobility transistor) GASFET amplifiers. The amplifier's RF gain and noise performance can be optimized by providing each HEMT stage an empirically-determined, optimum pair of DC drain voltage and DC drain current values. The amplifier stages are AC-coupled; therefore, each stage can have a distinct DC drain voltage and current. The FET Bias Card performs two functions: 1) it provides the optimal HEMT drain voltages and 2) it controls the gate voltages to maintain the optimal drain currents.

During the test phase of F110 fabrication, optimum VD and ID values at both 15 °K and 300 °K temperatures are determined. These values and the resultant VG are recorded on an amplifier data sheet for future reference. Appendix I, page 7 (in TR 11) is a copy of the F110, dewar S/N 03 data sheet. These data sheets are maintained in the AOC Front-End Laboratory file and the VG values are entered into the VLA and VLBA Data Checker programs for fault monitoring. In order to permit replacement of FET Bias Cards without adjustment, all new or spare cards are adjusted to produce a VD of +3 volts and an ID of 1 mA; these values should enable the HEMT to function until the optimum settings are determined.

Each FET Bias Card contains four identical sets of bias control circuits. Since the F110 uses five HEMTs in each amplifier channel, three FET Bias Cards are used; two cards (slots 4 and 5) provide bias voltages for four of the five HEMTs in each channel. A third card (slot 1) provides HEMT bias voltages for the two stage 5 HEMTs. The RCP bias card is installed in slot 4 and the LCP bias card is installed in slot 5. Dewar ground is the return for these twenty signals. Block Diagram C53213K002 shows the Bias Card-Dewar wiring connections and D53200S001 is the Bias Card Schematic. D53200A002 is the Bias Card assembly drawing.

Each bias circuit has a HEMT drain voltage (VD) and drain current (ID), adjustment potentiometer accessible on the edge of the card. HEMT sources are connected to dewar ground.

All five VD voltages can be measured on card-edge test jacks but cannot be measured by the DVM or the Monitor and Control System.

All five drain currents (ID) can be measured as voltages on card-edge test jacks. The ID voltage scaling factor is 1 mA/100 mV. The drain currents cannot be measured by the DVM or by the Monitor and Control System.

All gate voltages (VG) can be measured on card-edge test jacks. The first stage VG can also be measured by the Monitor Card DVM (with the selector switch S2 in the LF1 and RF1 positions) and by the Monitor and Control System via J2-7 (RF1 signal) and J2-9 (LF1 signal). The second, third, fourth and fifth stage VG voltages cannot be individually measured by the DVM or Monitor and Control System but a composite form of these four VG signals can be measured. Note from the block diagram that four RCP VG monitor signals are connected to the RF2 line to the DVM and to the Monitor and Control system via J2-8. In a similar manner, the four LCP VG monitor signals are connected to the LF2 line to the DVM. This connection sums the four VG signals and the composite signal level measured by the DVM is roughly the average of these four levels. These two composite VG signals are also connected to J2-8 (RF2) and J2-10 (LF2) for readout by the Monitor and Control System. Since the composite VG readout level is the sum of the stage 2, 3, 4 and 5 VG levels, its level will differ from the actual VG2,

.. VG5 levels. It is important to remember this VG monitoring configuration when comparing the amplifier S/N data sheet VG2, ... VG5 values (e.g., TR 11 Appendix I, page 7 example values) with the composite VG values read out as RF2 and LF2.

The normal range of VG is between 0 and -1 volts and is a function of temperature with a typical change of 100 to 300 mV from 300 °K to 15 °K. At 15 °K the VG value should be within ± 20 mV of the data sheet value. An open in the drain circuit will force the measured VG to the VG bias amplifier's positive limit, about +13.5 volts. In this condition, the forward gate current is limited to about 7 mA by a series resistor. A short in the drain or gate circuit (perhaps the result of insulation cold-flow on a dewar wire) will force the measured VG to the amplifier's negative limit, about -13.5 volts. In this condition, the actual HEMT gate voltage is limited to about -5 volts by the 1N821 protection diode.

Consider the first FET bias stage in the upper left quarter of D53200S001. Mentally picture the associated HEMT stage with the source connected to DC (dewar) ground, the gate connected to pin H (VG), and the drain connected to pin N (VD). Also assume that both the gate RF input and drain RF output are AC-coupled.

The bias circuit consists of a set of four interconnected operational amplifiers U1 (a TL084BCN quad operational amplifier) and a transistor Q1 (2N2219). The circuit description can be simplified if it is considered to consist of three sub-circuits: a VD driver circuit (U1-1, Q1 and U1-14), an ID sense circuit (U1-8), and a VG driver circuit (U1-7). The VD driver and ID sense circuit are described first because the VG driver circuit is a control loop that is dependent upon the outputs of the VD driver and ID sense circuits.

The bias circuit's first function is to set the VD voltage; this is the function of the VD driver, which consists of U1-1 and transistor Q1 (2N2219). This circuit is a voltage follower (noninverting operational amplifier with a gain of 1) with a Q1 emitter follower included in the feedback loop. Potentiometer R_{14} is the VD set point adjustment and provides a DC bias to U1-2, the + input. Since Q1 is inside the follower loop, U1's output is Q1's V_{BE} drop above the VD1 set point so the VD level is that set on R_{14} . Diode CR1 is a protective diode across Q1's emitter-base junction. The diode protects Q1 in the event that the U1-14 output ever swings negative (perhaps due to an accidental short while probing the board with a DVM, etc.). CR2 has a zenar voltage of 6.8 volts to protect the HEMT drain in the event of some malfunction or open in the operational amplifier circuit. U1-14 is a voltage follower used to isolate the drain from the VD1 test jack, TJ13. It also drives the ID sense circuit. R_1 , the 2 k Ω series resistor between U1-14 and the VD1 test jack, protects U1-14 in the event that TJ13 is inadvertently shorted to ground. Finally, C_2 , a 1.0 μ F capacitor filters the driver circuit's DC bias value to keep the output noise free.

The ID sense circuit consists of U1-14, a voltage follower and U1-8, a differential amplifier. HEMT drain current flows from the +15 volt power source through Q1, through R_8 (200 Ω), out pin N to the HEMT drain, and through the HEMT to dewar ground. ID is sensed as a voltage drop across R_8 and amplified by differential amplifier U1-8, which has a gain of 0.5. U1-8 is a differential amplifier because VD1 is a common-mode voltage on both U1-8's inputs. U1-8's output is scaled at 100 mV per mA of ID current. 2 k Ω resistor R_2 isolates U1-8's output from TJ12 in the event of an inadvertant short to ground.

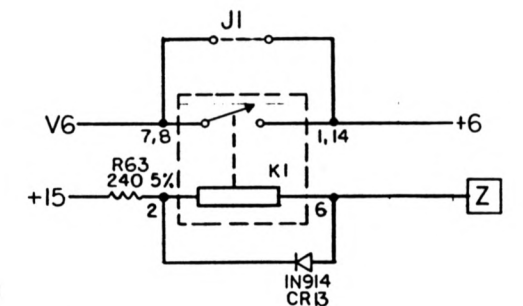
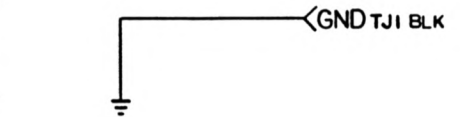
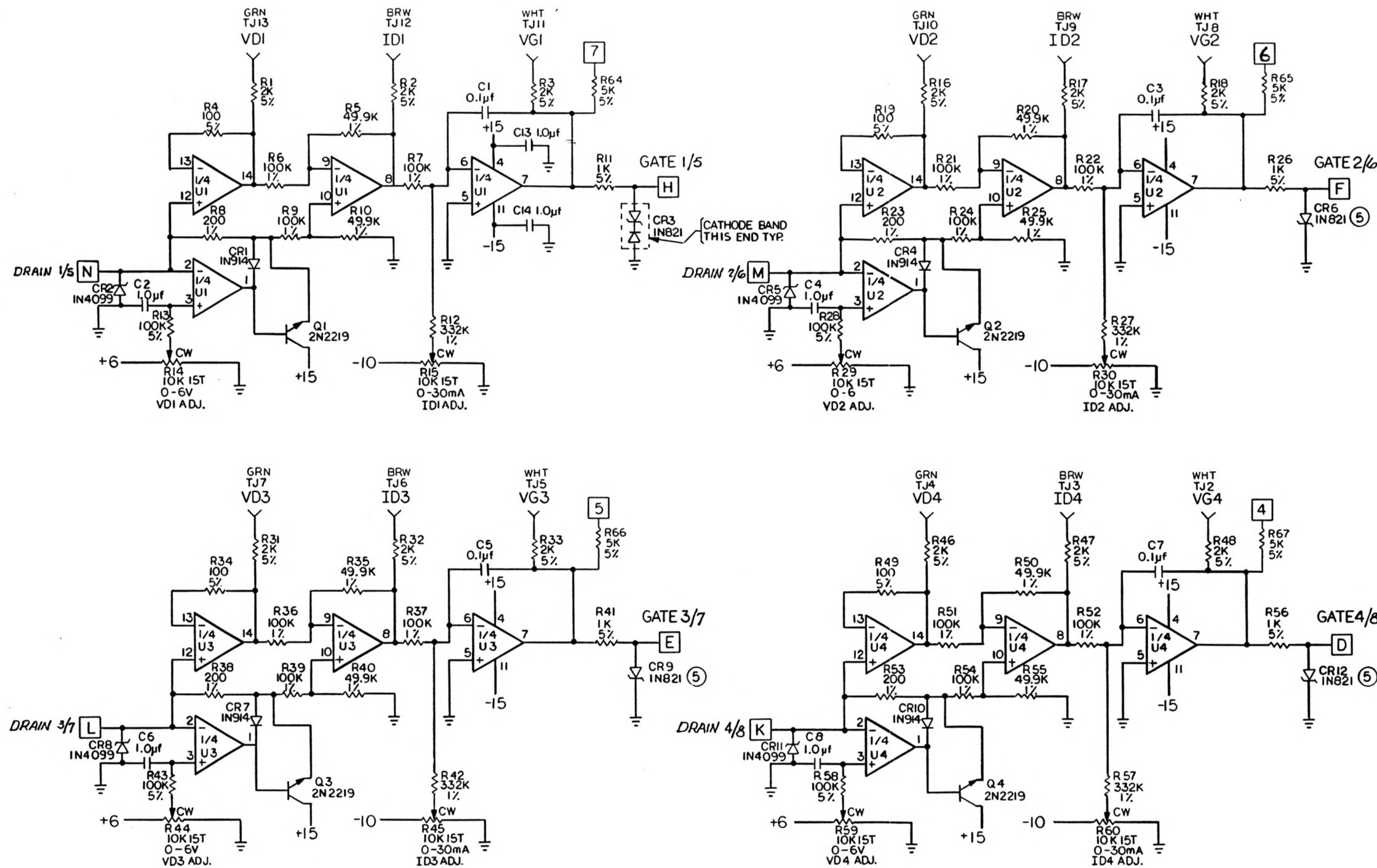
The second function of the FET bias circuit is to control VG so that ID is a constant, preset value; this is done by the VG drive circuit that closes the loop on ID. The VG driver consists of U1-7 with two

summing junction (U1-6) inputs: 1) a positive ID current input from U1-8 and 2) a negative offset current flowing to R_{15} , the ID1 adjustment potentiometer. U1-8's output is a positive voltage that is an analog of ID and is scaled at 100 mV/mA. A current proportional to this voltage is input to the U1-7 summing junction (the - input) via R_7 , 100 k Ω . When the loop is closed, the ID current into U1-6 is equal to the offset current through R_{12} , and the op-amp's output U1-7 is proportional to the offset current through R_{12} . Although it's not obvious, the HEMT's drain-source impedance is a factor in the feedback path.

Two DC reference voltages are used by the bias circuits: -10 volts and +6 volts, derived from a pair of AD581JH +10 volt precision reference voltage sources. Four 10 k Ω VD adjustment pots are connected in parallel and to resistor R_{62} , 1.5 k Ω , which drops four volts to produce the +6 volts for the VD adjustment potentiometers. Data sheets for the AD581JH and TL084BCN are included in Section 4.

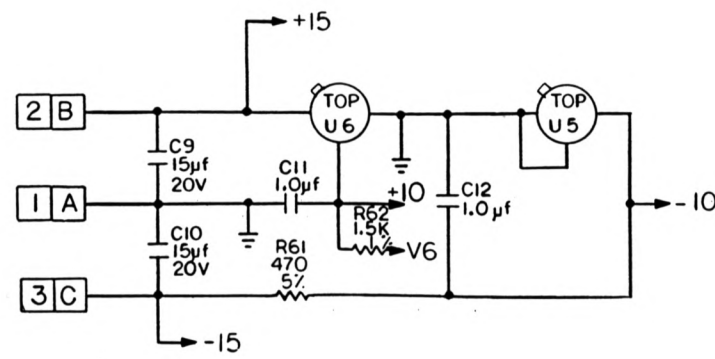
The 6 volt relay circuit on the right side of the schematic diagram is not used.

The FET Bias Card is tested on a Bias Card Tester that contains + and - 15 volt power supplies and four FETs with characteristics similar to cooled GASFETs. The card is plugged into the tester and a DVM is plugged into the card's ground (TJ1), VD, ID and VG test jacks. The four sets of VD and ID potentiometers are adjusted to produce a VD of +3 volts, an ID of 1 mA, and VG is measured to verify that it is about -400 mV with these VD and ID values.



REPRESENTS AMPLIFIER STAGES 1 THRU 4
DRAIN X/Y
REPRESENTS AMPLIFIER STAGES 5 THRU 8

NOTE: 2ND BIAS CARD MAY BE REQUIRED FOR AMPLIFIERS HAVING MORE THAN 4 STAGES.



- NOTES
- ① U1-4 TL084BCN
 - ② U5-6 AD581JH
 - ③ ALL CAPS. ARE 50V UNLESS OTHERWISE MARKED.
 - ④ ALL RES. AS FOLLOWS:
5% 1/4 WATT
1% 1/8 WATT
 - ⑤ SEE CR3 FOR INTERNAL SCHEMATIC.
 - ⑥ KI- MAGNECRAFT W17IDIP-14

C	Z/B7	G. MOERIS	COB70216-4
B	8/125	G. MOERIS	
A	8/11	H. DILL	CO-810816-21
REV	DATE	DRAWN BY	APPR'D BY
V	DATE	DRAWN BY	APPR'D BY
FRONT ENDS			
FET BIAS CARD			
4-STAGE			
SHEET NUMBER	1 OF 1	DRAWING NUMBER	0532006001
REV. D		SCALE	

The schematic diagram illustrates the internal circuitry of the 'СВЕТЛОЗВУКОВИЙ' (Light-Sound) device. It is organized into several functional blocks:

- Power Supply:** A transformer (TJ1-TJ13) provides power to the circuit. The primary winding is connected to a 220V AC source. The secondary winding is connected to a series of resistors (R60, R45, R30, R15) and a capacitor (C1).
- Control Section:** A potentiometer (P1) and a switch (S1) are used to control the device's operation. The potentiometer is connected to a 100kΩ resistor (R1) and a 100kΩ resistor (R2).
- Timing Section:** A capacitor (C1) and a resistor (R1) are used to create a timing delay. The capacitor is connected to a 100kΩ resistor (R1) and a 100kΩ resistor (R2).
- Central Processing:** Four integrated circuits (U1, U2, U3, U4) and a relay (K1) are the core components. U1 and U2 are connected to the power supply and the control section. U3 and U4 are connected to the timing section and the relay. The relay (K1) is connected to the speaker (A).
- Output Section:** The speaker (A) is connected to the relay (K1) and provides the sound output.

The diagram includes detailed component values and connections, such as the 100kΩ resistors (R1, R2), the 100kΩ capacitor (C1), and the 100kΩ resistor (R1). The components are labeled with their respective symbols and values.

##22 BUS WIRE

- ① Bom A53Z00B00Z
- ② SCH. D53Z00S00I
- ③ C53Z00Q00I
- ④ DRILL DWG. D53Z00P00I

B	7-7-87	GM		C0870219-7
REV	DATE	DRAWN BY	APPROV'D BY	DESCRIPTION
V A D L A P P R O V E D		FRONT END		NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA. 2290 DRAWN BY: G. MORRIS 10-6-87 DESIGNED BY: C. WENGER APPROVED BY:
		ASSY - BIAS CARD		
	SHEET NUMBER	DRAWING ORIGIN	D553200A002	REV B KAUF

2.9 RF Plate Description

The RF Plate is installed on the side of the card cage and performs the amplification, frequency conversion, noise calibration and 300 °K temperature measurement functions shown on the F110 Block Diagram C53213K001, page 2 (in TR 11). Since the dewar signal is mixed with an LO signal, the LCP and RCP outputs are 1st IF signals.

The RF Plate is pictured on TR 11 page 33, and is described on pages 18, and 33 through 37. There are no RF Plate Assembly or Block Diagram drawings.

Block Diagram C53213K002 shows the RF Plate functions in the context of this addendum's description. Note that there is not a High Cal noise source. Since the emphasis of this addendum is on the theory of operation of the card cage circuitry, the RF Plate functions are not described here. Refer to TR 11, Pages 18 and 33 for a description of the RF Plate's noise calibration circuitry and to pages 34 and 37 for a description of the room temperature post amplifiers. The specifications on pages 5 through 9 encompass the RF Plate's performance.

The RF Plate has a National Semiconductor LM335Z Precision Temperature Sensor to measure the plate's temperature. The sensor output is designated 300 °K and connected to the Monitor Card for measurement by the DVM and to the Monitor and Control System via J2-5. The LM335 operates as a two-terminal zenar and has a breakdown voltage directly proportional to absolute temperature with a scaling of +10 mV/°K. Section 4 contains a LM335Z data sheet.

2.10 Dewar DC Interface Description

The DC Feedthrough is the interface for the connection of DC power and HEMT bias lines to the dewar RF amplifiers, AC power to the heater, signal lines to temperature sensing diodes, and the LED circuitry. Wire list A53213W001 does not include the wiring between the card cage J3 and the DC Feedthrough. This wiring is shown on C53213K002, the 43 GHz FE Block Diagram.

There are two implementations of the DC Feedthrough: F110 Front-Ends constructed at Greenbank, West Virginia use the DC Feedthrough Assembly; B53213M008 and 6 mm Front-Ends constructed at the Socorro AOC use a hermetically-sealed electrical connector, a Bendix 9242PT1H-18-32P.

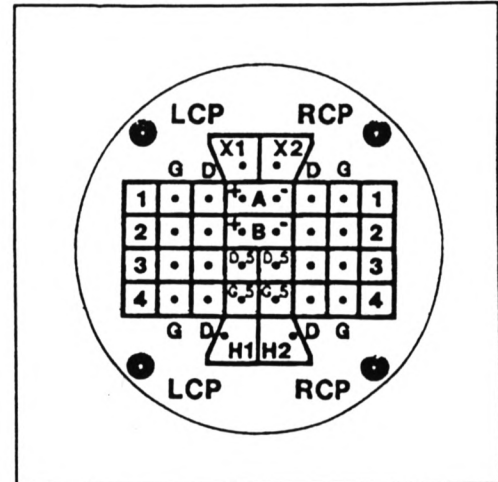


Figure 4 DC Feedthrough

The B53208M008 dewar DC Feedthrough is a hermetically-sealed interface panel that uses RFI feedthrough terminals soldered into a brass plate attached to the dewar inspection cover. Feedthrough terminal designations are shown on the artwork of a printed circuit board installed on the outside of the feedthrough. These designations are those used in C53213K002. Figure 4 shows the PC board terminal designations. The pin assignments for the Bendix connector are tabulated on the next page.

Twenty HEMT drain (VD) and gate (VG) bias lines pass through the DC Feedthrough. The HEMT drain lines are connected to dewar ground. The 15 °K stage temperature sensor diode (TSA) is connected to terminals A+ and A-. The diode anode is connected to A+ and the cathode to A-. Similarly, the 50 °K stage temperature sensor diode (TSB) anode and cathode are connected to terminals B+ and B-.

The HEMT VG and VD bias signals from the DC Feedthrough are connected to the dewar amplifiers via two small 12-pin, Micro-Tech connectors. Figure 5 on the next page, shows a wiring-side view of the 12-pin Micro-Tech connector. HEMT sources are connected to the dewar metal frame ground. Since the emphasis of this report is the card cage circuitry, for simplicity, these connectors are not shown on the block diagram.

The ground end of the LED circuits are connected to J3-21, Dewar Ground. The dewar ground line is also connected to the dewar metal structure.

As shown on C53213K002, the dewar LEDs circuit consists of two series strings, each consisting of a 120 Ω limiting resistor and five LEDs. The bottom of the strings are connected to dewar ground and the tops are connected to terminal X1. Outside the dewar, X1 is connected to P3-22. J3-22 is wired to pin T on the Monitor Card, the LED monitor input for the DVM. A 240 Ω limiting resistor is connected between pin T and Pin X. Pin X is not connected to any Monitor Card circuitry and simply serves as a convenient mounting terminal for the resistor. Pin X is jumpered to Pin 2 and B, the +15 volt bus. This resistor is shown on the Card Cage Assembly Drawing, D5323A005. The typical F110 LED monitor voltage is +10 volts but it can range between +8 to +11 volts. If one of the LED strings opens, the LED monitor voltage is about +13 volts and if both open, the monitor readout is +15 volts. This value can be

read on the DVM but will be full-scale in the Monitor and Control system readout because it exceeds the working range of the Standard Interface Board's A/D converter in F117.

The Socorro-built 6 mm Front-Ends use separate lines for the two LED strings; these are listed below.

The dewar heater AC power is connected to terminals H1 and H2. Inside the dewar, these terminals are connected to the 750 Ω , 75 watt, 240 volt heater.

Figure 5 shows the Bendix connector wire-side view. The Dewar Amplifier, Bendix and J3 connector's signal-pin and color-code assignments are as follows:

Signal	Dewar Amp	Bendix	J3
RCP D1	BRN	A	14
" G1	RED	B	13
" D2	ORG	C	16
" G2	YEL	D	15
" D3	GRN	E	18
" G3	BLU	F	17
" D4	VIO	G	20
" G4	GRAY	H	19
" D5	PINK	J	35
" G5	WHT	K	34
LCP D1	BRN	L	6
" G1	RED	M	5
" D2	ORG	N	8
" G2	YEL	P	7
" D3	GRN	R	10
" G3	BLU	S	9
" D4	VIO	T	12
" G4	GRAY	U	11
" D5	PINK	V	31
" G5	WHT	W	30
15° CATH(+A)	GRN	X	2
15° AN(-A)	BLK	Y	1
50° CATH(+B)	WHT	Z	4
50° AN(-b)	GRN	(A)*	3
RCP LED, GRN		(B)	22
LCP LED, RED		(C)	23
GROUND (both amps)**		(d)	21
N/C		(e)	
HEATER (SWITCHED) RED***		(f)	24
N/C		(g)	
N/C		(h)	
HEATER	BLK***	(b)	24

* Bracketed pins are lower-case letters

** Connected to dewar frame ground.

*** Heater wires are twisted pair.

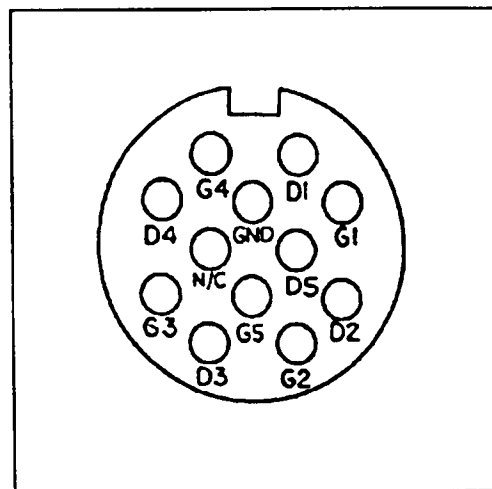


Figure 5 Micro-Tech Connector Pinout

2.11 AC Circuitry Description

The dewar's cryogenic functions are powered by two-phase, 150 volts AC power. Figure 1.3-3 on page 22 (in TR 11) shows the Front-End's AC wiring. Page 14 lists the cryogenic function's AC loads. Because the F110 AC power is peculiar to the refrigerator's requirements, it does not have an internal DC power supply for the card cage circuitry. DC + and - 15 volt power is provided by the control interface via J5. This DC power is described in Section 2.15.

Note that the 150 volt, two-phase power is supplied by a Model P111 power supply, which is briefly described in TR 11, Section 1.3.5, page 19. Figure 2.12-1, page 41, shows the power supply schematic. An important P111 power supply output is the AC current monitor, which is a DC signal scaled at 10 amperes/volt. This is input to the Front End on J4-1 (signal) and J4-2 (return) and the signal polarity is positive. This signal, designated ACI, is connected to the Monitor Panel for DVM measurement and to J2-6 for readout by the Monitor and Control System.

On TR 11, page 22, note the vacuum solenoid current limiting resistor R_1 , 300 Ω , 20 watts, which is installed on the card cage connector mounting plate. This resistor is pictured in the card cage assembly drawing, D53206A005, in Section 2.1 (this report). If the vacuum solenoid is actuated for a long time, the plate will become quite hot from the resistor's power dissipation. Also note that a stuck vacuum solenoid will draw 0.40 amperes. The dewar heater limiter resistor R_2 , 5 k Ω , 10 watts, is also installed on the card cage connector mounting plate; it too is pictured on the card cage assembly drawing.

The cryogenic control equations were described in Section 2.4 and Section 2.5, (Control Card) described the implementation of the control equations. Note that the R, S, H and X contacts shown on the Front End AC Wiring schematic (Figure 1.3-3, page 22) are the Control Card relay contacts.

The dewar heater is a 750 Ω , 75 watt, 240 volt Hotwatt heater installed on the 15 °K stage. Heater current is 0.20 amperes and dissipation is 30 watts. Note from the Front-End AC wiring schematic on page 22 that the heater has an internal thermostat that opens at a high temperature level. This feature prevents overheating in the event of a Control Card failure.

2.12 DVM Readout Values and Tolerances

The table below shows the DVM analog selector switch position Label, Function, Scaling, Normal Value and acceptable Tolerance Range.

DVM S2 Label	Function	1 volt =	Normal Value	Tolerance Range
VP	Pump Vacuum ¹	-----	+10.000 ²	+9.950 to +10.000
VD	Dewar Vacuum ¹	-----	0.000	-0.200 to +0.200
15K	15 °K Stage	100 °K	+0.150	+0.100 to +0.200
50K	50 °K Stage	100 °K	+0.550	+0.400 to +0.700
300K	300 °K Station	100 °K	+2.900	+2.000 to +3.000
AC CURR	AC Current ³	10 Amps	-----	-----
RF1	RCP Gate 1	1 Volt	-0.60 ⁴	-1.00 to +1.00
RF2	RCP Gates 2+3 ⁵	1 Volt	-0.60 ⁴	-1.00 to +1.00
LF1	LCP Gate 1	1 Volt	-0.60 ⁴	-1.00 to +1.00
LF2	LCP Gates 2+3 ⁵	1 Volt	-0.60 ⁴	-1.00 to +1.00
LED	LED Voltage	1 Volt	+10 ⁶	+8.000 to +12.000
EXT	Spare Mon	1 Volt	-----	N/A

Notes:

- 1 Nonlinear vacuum readout scale, see page 13 in TR 11.
- 2 Readout when pump manifold is at sea level atmospheric pressure.
- 3 AC current depends upon cryogenic state, see page 14 in TR 11.
- 4 Typical value. Large changes indicate a dewar amplifier problem.
- 5 Approximate sum of Stage 2 through 5 Gate voltages.
- 6 If one LED string opens, the LED readout voltage is about +13 volts; if both strings open, the LED readout is +15 volts.

2.13 Monitor and Control System Readout Values

The Telescope Operator Front-End Cryogenic and Electronics displays show F110 status; Figures 6 and 7 below, are similar to these displays. Figure 6 shows the calibration mode, monitored calibration current and voltage, and the three HEMT gate bias voltages. Figure 7 shows the commanded cryogenics mode, monitored mode, state, discretes, and selected analog monitor values.

FRONT END ELECTRONICS 7MM			
CAL MODE LOW SWITCHING			
CAL I	11.72 V	27.813	HEMT 10.00
7.5 V	7.505	GRD	-0.005
LF FET#1	-0.327	RT FET#1	-0.508
LF FET#2	-0.884	RT FET#2	-0.864

Figure 6 VLBA F110 Electronics Screen

FRONT END CRYOGENICS 7MM			
CMD COOL MANUAL STATE COOL			
PUMP REQ	OFF	AC 1	0.44
VALVE	CLOSED	15K	20.5
PUMP VAC	9545	50K	64.0
DEWAR VAC	1	300K	294

Figure 7 VLBA F110 Cryogenics Screen

The VLBA control interface is F117. It controls F110, reads F110 discretes, and converts F110 analog signals to digital values for input to the Antenna control computer via the Monitor and Control bus.

The first VLBA screen shows that the calibration level is LOW and is SWITCHING. F117 measures some additional Front-End analog parameters: (CAL I) cal current, cal voltage, the F117 +7.5 volt reference (7.5V), and F117 ground reference (GRD). The example values show a calibration current of 11.72 mA and a cal voltage of 27.813 volts. The HEMT 10.00 voltage is the LED measurement described in Section 2.10. The FET voltages are the Bias Card HEMT gate voltages described in Section 2.8.

The second VLBA screen shows that the Front-End is commanded to the COOL state, is in the MANUAL mode, and the X, C and H monitor discretes show the COOL state. The PUMP REQ(uest) is OFF and the (vacuum) VALVE is CLOSED. The 150 volt AC current load is 0.44 amperes. PUMP (VP) VAC is 9545 because the vacuum manifold is at the antenna's atmospheric pressure (see the vacuum vs. monitor voltage curve on page 13). DEWAR VAC(uum) is 1 μ m. Note that this value has been converted from the voltage readout value to the corresponding vacuum level. The 15K (TA), 50K (TB), and 300K temperatures are shown degrees Kelvin. The SENS temperature (non-linear form of TA) is not shown.

F14 is the VLA 6 mm Front-End control interface. VLA 6 mm Front-End monitor screens are similar to the VLBA examples shown above.

2.14 Band, Serial Number, and Modification Level Encoding

F110 has provisions to identify its serial number, frequency band and modification level as hard-wired binary codes on the J5 connector. These codes are implemented by connecting the appropriate J5 pins to ground lugs near the connector. Grounded pins are 0's and floating pins are 1's. The control interfaces (F14, VLA and F117, VLBA) have pull-up resistors to +5 volts for input to TTL logic. Drawing C53213K002 shows the code bit assignments on J5.

The F110 band code is 9_H and the associated parity bit is a 0. Page 18 (in TR 11) describes the band, serial number and modification level encoding.

2.15 Front End DC power and Quality Ground

The F110 card cage DC power is + and - 15 volts from J5, provided by the associated control interface (F14 in the VLA and F117 in the VLBA). The -15 volt power demand is 100 mA and the +15 volt power demand is 1500 mA. This includes the RF Plate's +15 volt 500 mA demand. The +15 volt current demand is dependent upon F110's cryogenic state. The Control and Monitor card's LS-TTL logic is powered by on-card +5 volt regulators from +15 volt inputs.

Bus-bars running through the card cage PC board connectors (including spare card slots 1 and 2) provide +15 and -15 and power from J5-2 (+15) and J5-3 (-15), respectively. Like other VLBA-style Front-Ends, the F110 has protective 1N5355A 18 volt zenar diodes installed in the card cage +15 and -15 volt bus bars. The Ground bus bar is connected to chassis ground at slot 1, the RCP/LCP stage 5 FET Bias Card. DC power distribution is shown in C53213K002.

Quality Ground is an analog ground reference that does not carry power currents. This reference is supplied to the Monitor Panel DVM and to the control interface via J2-13. The Quality Ground is connected to chassis ground near slot 5, the LCP FET Bias Card. The Quality Ground string is shown on C53213K002.

Dewar ground on J3-21 is connected to chassis ground and also to the dewar metal structure. This is the return path for the HEMT sources and the LED strings.

2.16 Wire List Problems

Wire List A53213W001, Sheet 2, TR 11 Appendix page II-21 has three errors in the pin H, pin K and pin N Function column. The pin H function is named LCP GATES; it should be LCP GATE 5. The pin K function is named RCP DRAINS; it should be RCP DRAIN5. The pin N function is named LCP DRAINS; it should be LCP DRAIN 5.

Sheet 8, Appendix page II-27 has an error in the TO column: the entry is P14-S; it should be P14-1.

Standard Curve 10: Measurement Current = 10 μ A \pm 0.05%

T (K)	Voltage	dV/dT (mV/K)	T (K)	Voltage	dV/dT (mV/K)	T (K)	Voltage	dV/dT (mV/K)
1.40	1.69812	-13.1	16.0	1.28527	-18.6	95.0	0.98564	-2.02
1.60	1.69521	-15.9	16.5	1.27607	-18.2	100.0	0.97550	-2.04
1.80	1.69177	-18.4	17.0	1.26702	-18.0	110.0	0.95487	-2.08
2.00	1.68786	-20.7	17.5	1.25810	-17.7	120.0	0.93383	-2.12
2.20	1.68352	-22.7	18.0	1.24928	-17.6	130.0	0.91243	-2.16
2.40	1.67880	-24.4	18.5	1.24053	-17.4	140.0	0.89072	-2.19
2.60	1.67376	-25.9	19.0	1.23184	-17.4	150.0	0.86873	-2.21
2.80	1.66845	-27.1	19.5	1.22314	-17.4	160.0	0.84650	-2.24
3.00	1.66292	-28.1	20.0	1.21440	-17.6	170.0	0.82404	-2.26
3.20	1.65721	-29.0	21.0	1.19645	-18.5	180.0	0.80138	-2.28
3.40	1.65134	-29.8	22.0	1.17705	-20.8	190.0	0.77855	-2.29
3.60	1.64529	-30.7	23.0	1.15558	-21.7	200.0	0.75554	-2.31
3.80	1.63905	-31.6	24.0	1.13598	-15.9	210.0	0.73238	-2.32
4.00	1.63263	-32.7	25.0	1.12463	-7.72	220.0	0.70908	-2.34
4.20	1.62602	-33.6	26.0	1.11896	-4.34	230.0	0.68564	-2.35
4.40	1.61920	-34.6	27.0	1.11517	-3.34	240.0	0.66208	-2.36
4.60	1.61220	-35.4	28.0	1.11212	-2.82	250.0	0.63841	-2.37
4.80	1.60506	-36.0	29.0	1.10945	-2.53	260.0	0.61465	-2.38
5.00	1.59782	-36.5	30.0	1.10702	-2.34	270.0	0.59080	-2.39
5.50	1.57928	-37.6	32.0	1.10263	-2.08	280.0	0.56690	-2.39
6.00	1.56027	-38.4	34.0	1.09864	-1.92	290.0	0.54294	-2.40
6.50	1.54097	-38.7	36.0	1.09490	-1.83	300.0	0.51892	-2.40
7.00	1.52166	-38.4	38.0	1.09131	-1.77	310.0	0.49484	-2.41
7.50	1.50272	-37.3	40.0	1.08781	-1.74	320.0	0.47069	-2.42
8.00	1.48443	-35.8	42.0	1.08436	-1.72	330.0	0.44647	-2.42
8.50	1.46700	-34.0	44.0	1.08093	-1.72	340.0	0.42221	-2.43
9.00	1.45048	-32.1	46.0	1.07748	-1.73	350.0	0.39783	-2.44
9.50	1.43488	-30.3	48.0	1.07402	-1.74	360.0	0.37337	-2.45
10.0	1.42013	-28.7	50.0	1.07053	-1.75	370.0	0.34881	-2.46
10.5	1.40615	-27.2	52.0	1.06700	-1.77	380.0	0.32416	-2.47
11.0	1.39287	-25.9	54.0	1.06346	-1.78	390.0	0.29941	-2.48
11.5	1.38021	-24.8	56.0	1.05988	-1.79	400.0	0.27456	-2.49
12.0	1.36809	-23.7	58.0	1.05629	-1.80	410.0	0.24963	-2.50
12.5	1.35647	-22.8	60.0	1.05267	-1.81	420.0	0.22463	-2.50
13.0	1.34530	-21.9	65.0	1.04353	-1.84	430.0	0.19961	-2.50
13.5	1.33453	-21.2	70.0	1.03425	-1.87	440.0	0.17464	-2.49
14.0	1.32412	-20.5	75.0	1.02482	-1.91	450.0	0.14985	-2.46
14.5	1.31403	-19.9	80.0	1.01525	-1.93	460.0	0.12547	-2.41
15.0	1.30422	-19.4	85.0	1.00552	-1.96	470.0	0.10191	-2.30
15.5	1.29464	-18.9	90.0	0.99565	-1.99	475.0	0.09062	-2.22

Shaded portion highlights truncated portion of Standard Curve 10 corresponding to the reduced temperature range of DT-471 diode sensors.
The 1.4 K to 325 K portion of Curve 10 is applicable to the DT-450 miniature silicon diode sensor.

DT-500-DRC (B) Voltage - Temperature Characteristic

T, Kelvin	Sensor Voltage	T, Kelvin	Sensor Voltage	T, Kelvin	Sensor Voltage
1.0	--	19.0	1.5944	160.0	0.75680
1.5	2.6647	20.0	1.5159	165.0	0.74276
1.6	2.6622	21.0	1.4389	170.0	0.72868
1.7	2.6593	22.0	1.3575	175.0	0.71457
1.8	2.6562	23.0	1.2895	180.0	0.70041
1.9	2.6528	24.0	1.2378	185.0	0.68622
2.0	2.6491	25.0	1.1955	190.0	0.67201
2.2	2.6410	26.0	1.1645	195.0	0.65777
2.4	2.6321	27.0	1.1434	200.0	0.64353
2.6	2.6223	28.0	1.1293	205.0	0.62928
2.8	2.6117	29.0	1.1192	210.0	0.61504
3.0	2.6005	30.0	1.1115	215.0	0.60084
3.2	2.5886	32.0	1.1003	220.0	0.58672
3.4	2.5762	34.0	1.0923	225.0	0.57268
3.6	2.5633	36.0	1.0859	230.0	0.55880
3.8	2.5499	38.0	1.0804	235.0	0.54508
4.0	2.5361	40.0	1.0752	240.0	0.53152
4.2	2.5220	45.0	1.0632	245.0	0.51810
4.4	2.5075	50.0	1.0515	250.0	0.50479
4.6	2.4928	55.0	1.0397	255.0	0.49151
4.8	2.4780	60.0	1.0276	260.0	0.47818
5.0	2.4631	65.0	1.0151	265.0	0.46483
5.5	2.4254	70.0	1.0024	270.0	0.45137
6.0	2.3877	75.0	0.98933	275.0	0.43773
6.5	2.3505	80.0	0.97610	280.0	0.42388
7.0	2.3142	85.0	0.96277	285.0	0.40988
7.5	2.2790	90.0	0.94939	290.0	0.39574
8.0	2.2452	95.0	0.93591	295.0	0.38155
8.5	2.2127	100.0	0.92238	300.0	0.36729
9.0	2.1818	105.0	0.90881	305.0	0.35294
9.5	2.1524	110.0	0.89520	310.0	0.33843
10.0	2.1246	115.0	0.88156	315.0	0.32375
11.0	2.0731	120.0	0.86788	320.0	0.30893
12.0	2.0236	125.0	0.85412	325.0	0.29407
13.0	1.9730	130.0	0.84035	330.0	0.27919
14.0	1.9186	135.0	0.82652	335.0	0.26432
15.0	1.8561	140.0	0.81265	340.0	0.24943
16.0	1.7942	145.0	0.79873	345.0	0.23458
17.0	1.7325	150.0	0.78478	350.0	0.21974
18.0	1.6651	155.0	0.77081	355.0	0.20500
				360.0	0.19037
				365.0	0.17596
				370.0	0.16192
				375.0	0.14846
				380.0	0.13597



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HASTINGS VACUUM GAUGE TUBES

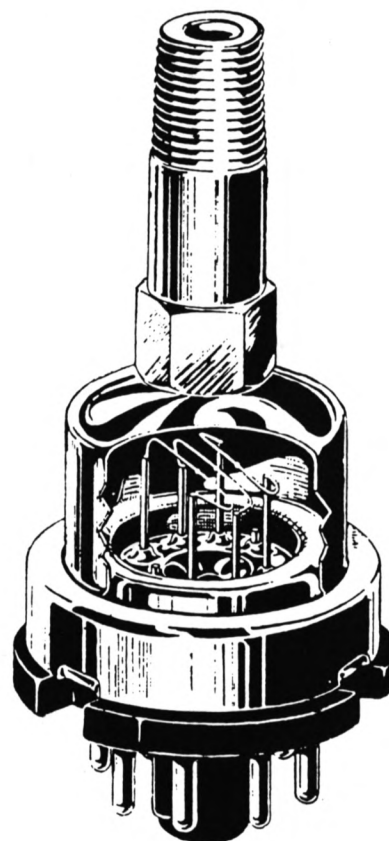
For Economy and Reliability in Vacuum Measurement

- Corrosion-Resistant
- Non-Contaminating
- Stable Calibration
- Rugged Under Demanding Conditions



Standard Metal Type

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Design Features

Hastings Vacuum Gauge Tubes are precision sensing devices designed to provide maximum accuracy in the measurement and control of vacuum. Fully compensated for both temperature and rate of temperature change, the tubes are renowned worldwide for their dependability, and boast a history of success that has endured for over 40 years.

Hastings Gauge Tubes use the rugged but sensitive, time-tested Hastings thermopile sensor. Short, firmly connected thermocouples have no suspended weld to an external heater.

The unique Model DV-760 uses a piezo-resistive strain gauge on a silicon chip. The chip includes a sealed vacuum reference, a resistive bridge circuit, and a temperature compensation network.

Hastings Gauge Tubes are color-coded for matching to the appropriate vacuum gauge or controller.

CHARACTERISTICS OF HASTINGS VACUUM GAUGE TUBES

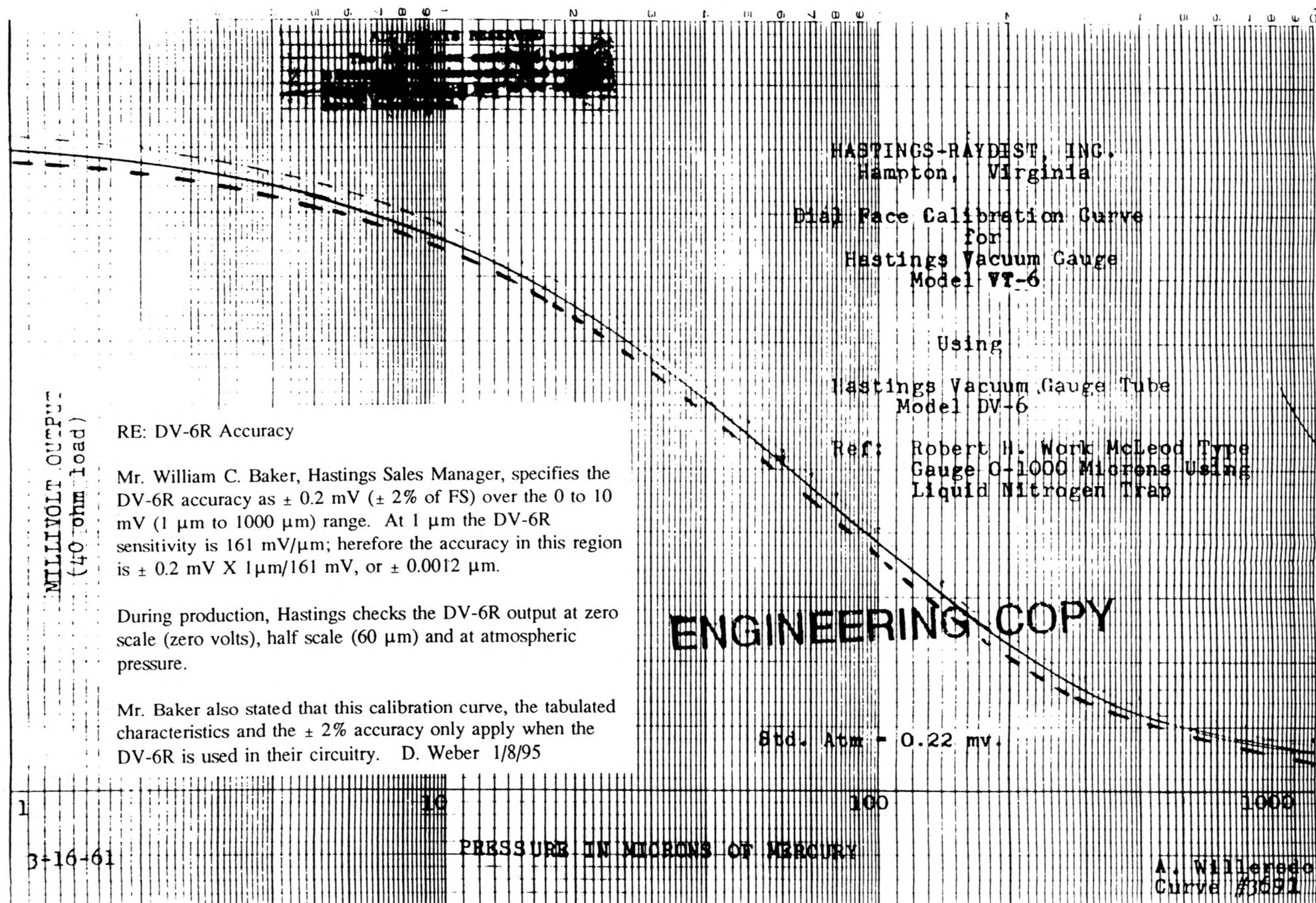
Metal Tube	DV-4D	DV-5M	DV-6M	DV-8	DV-23	DV-24	DV-760
"R" Series	DV-4R	—	DV-6R	—	—	—	—
Stainless/Ceramic	DV-34	—	DV-36	—	—	—	—
Pyrex	DV-16D	DV-18	DV-20	DV-31	DV-43	DV-44	—
Metal w/VCR Connection	DV-4D-VCR	DV-5M-VCR	DV-6M-VCR	—	DV-23-VCR	—	—
Metal w/KF-16 Connection	DV-4D-KF-16	—	DV-6M-KF-16	—	DV-23-KF-16	DV-24-KF-16	—
Best Sensitivity Range	0.2 - 5 torr 0.1 - 5 mbar	2 - 20 mtorr 0.002 - .05 mbar	10 - 200 mtorr .01 - .2 mbar	0.1 - 10 mtorr —	5 mtorr - 1 torr .01 - 2 mbar	.1 - 5 torr .1 - 5 mbar	1 - 800 torr 1 - 1100 mbar
Usable Range	0.1 - 20 torr 0.1 - 20 mbar	0.2 - 100 mtorr 0.001 - .1 mbar	1 - 1000 mtorr .01 - 1 mbar	0.1 - 10 mtorr —	5 mtorr - 5 torr .01 - 5 mbar	.1 - 20 torr .1 - 10 mbar	1 - 800 torr 1 - 1100 mbar
Internal Volume of Gauge Tube	1/20 ⁻³ 0.8cc	1/2 ⁻³ 8.2cc	1/2 ⁻³ 8.2cc	1/2 ⁻³ 8.2cc	1/2 ⁻³ 8.2cc	1/2 ⁻³ 8.2cc	1/20 ⁻³ 0.8cc
Thermopile Temperature In a High Vacuum At Atmosphere	250°C 30°C	48°C 1.5°C	300°C 6°C	120°C 10°C	400°C 10°C	400°C 35°C	N/A N/A
A-C Amperes Through Tube	0.029	0.03	0.021	0.053	.04/.04	.03/.04	N/A
A-C Volts Across Tube	0.32	0.20	0.38	0.32	.20/.20	.19/.19	N/A
Watts Required by Tube	0.009	0.006	0.006	0.017	.016	.11	.018
Output at High Vacuum mv D-C	10	2	10	2	13	13	—
Internal Resistance - ohms	11	6	18	6	5/6	6.5/7.5	—
Response Time							
Zero to ATM - seconds	0.04	0.8	0.06	0.8	0.07	0.05	.002
ATM to Zero - seconds	0.16	25	2.9	25	3.0	.2	.002
A-C Connection Pin #	3-5	3-5	3-5	3-5	2-4, 6-8	2-4, 6-8	—
D-C Connection Pin #	7	7	7	7	—	—	—
Color of Base Metal Tube	Purple	Red	Yellow	Green	Orange	White	Lt. Blue

The above information includes nominal values only. Not to be used for design purposes or acceptance tests.

PRESSURE AND TEMPERATURE DATA

Tube Type	Max. Pressure	Max. Temperature
Metal: DV-4D, DV-4D-VCR, DV-4D-KF-16	150 psig	100°C
All other metal (except Model DV-760)	50 psig	100°C
"R" Series	250 psig	150°C
Stainless/Ceramic	600 psig	300°C
Pyrex	15 psig	400°C
Model DV-760	15 psig	40°C

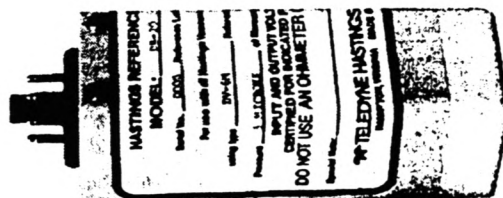
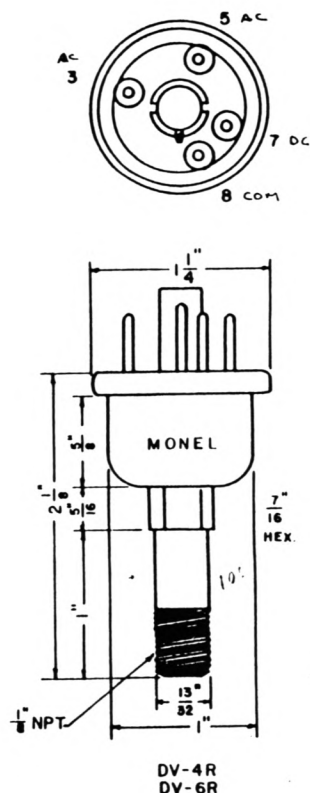
The gauge tubes can be expected to withstand the listed pressure and temperature without rupture but they are not warranted as safe under these conditions. For critical conditions or special testing, contact factory.



HASTINGS REFERENCE TUBE

A Quick Calibration Device for
Hastings Vacuum Gauges

- Instant Calibration Check
- Recalibration of Hastings Gauges
- Adjusts Gauge for Any Length Cable
- Stable, Accurate, Rugged, and Reliable



Reference Tube

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General

The Hastings Reference Tube is an evacuated, sealed vacuum gauge tube accurately calibrated to precisely simulate a gauge tube at a given operating pressure. It is electrically equivalent to the metal and glass gauge tubes used with Hastings Instruments. It permits quick and easy recalibration of Hastings Vacuum Gauge Indicators by merely plugging the instrument into the reference and adjusting the calibration "current set" potentiometer until the instrument reads the exact pressure noted on the reference. Hastings Reference Tubes are available equivalent to most Hastings Gauge Tubes.

Application

Hastings Vacuum Gauge Indicators, Controllers, or Recorders can be checked or recalibrated in seconds by merely plugging the gauge tube cable into the reference tube. If calibration adjustment is necessary, the "Current Set" potentiometer is adjusted until the instrument indicates the pressure marked on the reference tube. The customer now knows his instrument is correctly calibrated.

Whenever cable lengths between gauge tube and instrument are changed, some error may be introduced, requiring that the instrument be readjusted to compensate for any losses involved. By plugging the Reference Tube into the new cable and readjusting the instrument for a correct reading, this "error" is eliminated.

Selection

Choose the reference tube that is equivalent to the glass or metal Hastings Gauge Tube you are now using. The Reference Tube will be matched and sealed at a pressure falling on the lower portion of the scale and calibrated accurately at this exact pressure. For example, if an instrument uses a DV-6M Gauge Tube, a DB-20 Reference Tube is ordered. The customer receives a tube marked, possibly, 10 microns. This is the exact pressure to which the indicator should be adjusted when plugged into the reference tube.

Selection Chart

Equivalent Gauge Tube and Range			Reference Tube	
Metal	Glass	Range	Model No.	Stock No.
*DV-3M		0-1000 μ Hg	DB-16D	55-100
DV-4D		0-20mm Hg		
*DV-5M		0-100 μ Hg	*DB-18	55-103
DV-6M	DV-20	0-1000 μ Hg	DB-20	55-104
DV-8M		0.01-10 μ Hg	DB-31	55-105
DV-23		0-5000 μ Hg	DB-33	55-106
DV-24		0-50 Torr	DB-44	55-107
DV-310		0-1000 mTorr and 0-1400 mbar	DB-300	55-252

*State reference letter of your Gauge Tube type for matching purposes.

Construction

Hastings Reference Tubes employ the same Hastings noble metal thermopile used in all Hastings Vacuum Gauge Tubes. The thermopile is sealed in a glass capsule that has been evacuated, baked, outgassed, sealed, and then aged to ensure stability over long periods of time. The sealed capsule is then housed in a protective metal shell to provide a rugged, trouble-free assembly.

Calibration

Considerable care and time are required in the manufacture to obtain the high degree of precision and stability required for the reference tube.

The thermopile is matched to the reference letter of the customer's tubes and maintains its calibration over long periods of time. However, for applications requiring the highest possible degree of accuracy, a periodic return of the reference tube to the factory for a check and recalibration may be desirable. An annual or semiannual check assures the customer of an accurate and reliable reference at all times.

IMPORTANT NOTE:

These reference tubes are designed specifically for use with instruments employing Hastings circuitry and are NOT interchangeable with instruments using other circuitry. Connection to another manufacturer's instrument may result in burnout.

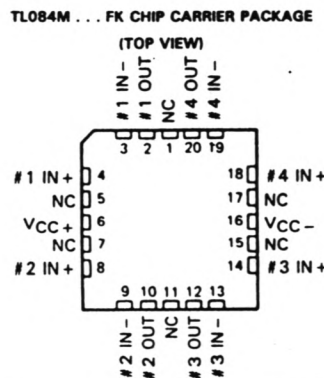
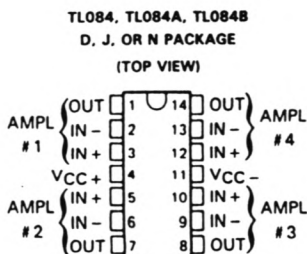
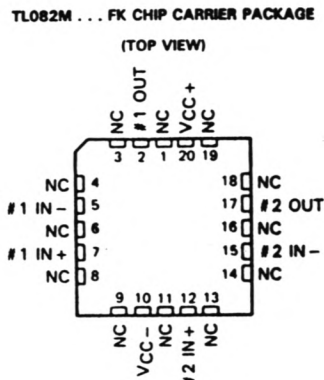
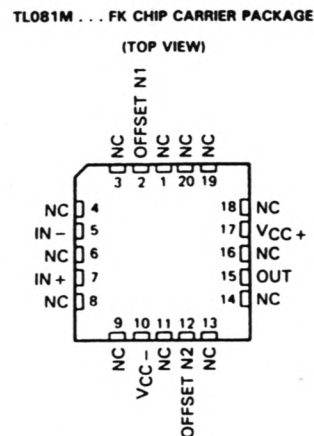
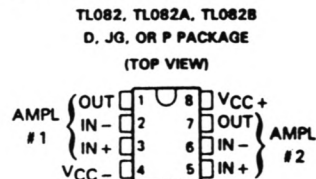
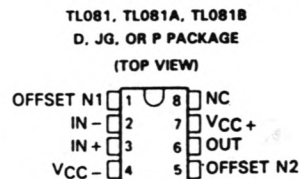
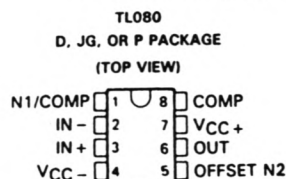
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BROWN ENGINEERING**
Hastings Instruments
P.O. Box 1436 • Hampton, VA 23661

TL080, TL081, TL082, TL084, TL081A, TL082A, TL084A
TL081B, TL082B, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS
 D2287, FEBRUARY 1977—REVISED OCTOBER 1990

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- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
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- Internal Frequency Compensation (Except TL080, TL080A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/ μ s Typ
- Common-Mode Input Voltage Range Includes $V_{CC}+$



NC—No internal connection

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TL080, TL081, TL082, TL084, TL081A, TL082A, TL084A
TL081B, TL082B, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL08_C TL08_AC TL08_BC	TL08_I	TL08_M	UNIT
Supply voltage, $V_{CC}+$ (see Note 1)	18	18	18	V
Supply voltage, $V_{CC}-$ (see Note 1)	-18	-18	-18	V
Differential input voltage (see Note 2)	± 30	± 30	± 30	V
Input voltage (see Notes 1 and 3)	± 15	± 15	± 15	V
Duration of output short circuit (see Note 4)	unlimited	unlimited	unlimited	
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	0 to 70	-40 to 85	-55 to 125	°C
Storage temperature range	-65 to 150	-65 to 150	-65 to 150	°C
Case temperature for 60 seconds	FK package			
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J or JG package			
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, N, or P package			
	280	280		°C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between $V_{CC}+$ and $V_{CC}-$.
 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

electrical characteristics, $V_{CC} \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_O = 0$, $R_S = 50 \Omega$		3	8	3	8		mV
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50 \Omega$, $T_A = -55^\circ\text{C to } 125^\circ\text{C}$		18		18			$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current ²	$V_O = 0$		5	100	5	100		pA
I_{IB} Input bias current ²	$V_O = 0$		30	200	30	200		pA
V_{ICR} Common-mode input voltage range	$T_A = 25^\circ\text{C}$	± 11	to 15		± 11	to 15		V
V_{OM} Maximum peak output voltage swing	$T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$	± 12	± 13.5		± 12	± 13.5		V
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10 \text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 2 \text{ k}\Omega$	25	200		25	200		V/mV
B_1 Unity-gain bandwidth	$T_A = 25^\circ\text{C}$		3			3		MHz
r_i Input resistance	$T_A = 25^\circ\text{C}$		10^{12}			10^{12}		Ω
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR \text{ min}}$, $R_S = 50 \Omega$, $V_O = 0$, $T_A = 25^\circ\text{C}$	80	86		80	86		dB
k_{SVR} Supply voltage rejection ratio ($\Delta V_{CC} \pm \Delta V_{IO}$)	$V_{CC} = \pm 15 \text{ V to } \pm 9 \text{ V}$, $R_S = 50 \Omega$, $V_O = 0$, $T_A = 25^\circ\text{C}$	80	86		80	86		dB
I_{CC} Supply current (per amplifier)	No load, $T_A = 25^\circ\text{C}$		1.4	2.8		1.4	2.8	mA
$V_{O1/V_{O2}}$ Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25^\circ\text{C}$		120			120		dB

- ¹ All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
² Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.



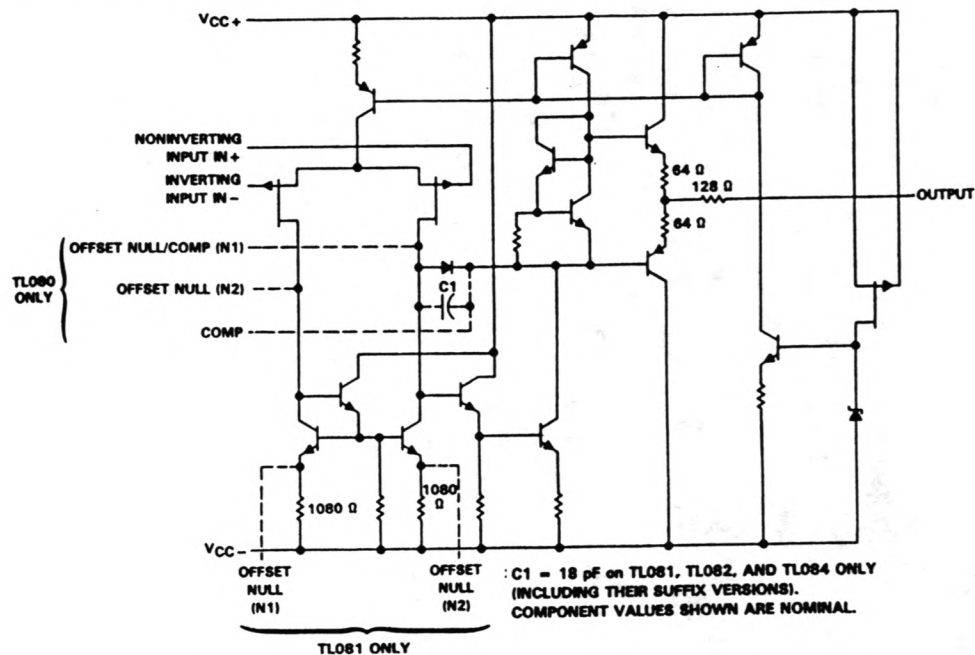
TL080, TL081, TL082, TL084, TL081A, TL082A, TL084A TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

operating characteristics, $V_{CC} \pm = \pm 15$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	$V_I = 10$ V, $R_L = 2$ k Ω , $C_L = 100$ pF, See Figure 1	8*	13		V/ μ s
	$V_I = 10$ V, $R_L = 2$ k Ω , $C_L = 100$ pF, $T_A = -55^\circ\text{C}$ to 125°C See Figure 1	5*			
t_r	$V_I = 20$ mV, $R_L = 2$ k Ω , $C_L = 100$ pF, See Figure 1		0.05		μ s
			20%		
V_n	$R_S = 100$ Ω , $f = 1$ kHz		18		nV/ $\sqrt{\text{Hz}}$
	$f = 10$ Hz to 10 kHz		4		μ V
I_n	$R_S = 100$ Ω , $f = 1$ kHz		0.01		pA/ $\sqrt{\text{Hz}}$
THD	$V_O(\text{rms}) = 10$ V, $R_S \leq 1$ k Ω , $R_L \geq 2$ k Ω , $f = 1$ kHz		0.003%		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

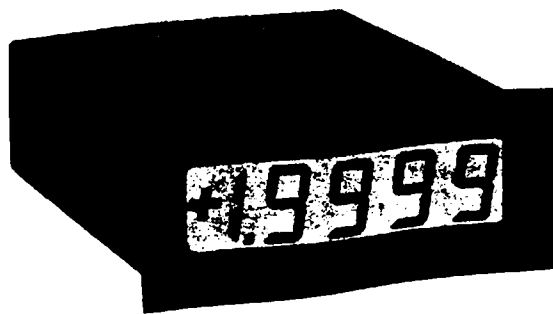
schematic (each amplifier)



electrical characteristics, $V_{CC} \pm = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL080C TL081C TL082C TL084C			TL081AC TL082AC TL084AC			TL081BC TL082BC TL084BC			TL081 TL082 TL083 TL084			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage $T_A = 25^\circ\text{C}$ $R_S = 50$ Ω	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	mV
ΔV_{IO}	Temperature coefficient of input offset voltage $T_A = \text{full range}$	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current† $T_A = 25^\circ\text{C}$	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	pA
I_{IB}	Input bias current† $T_A = 25^\circ\text{C}$	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	$V_O = 0$	± 1	± 25	pA
V_{ICR}	Common-mode input voltage range $T_A = 25^\circ\text{C}$	± 11	± 10	± 12	± 11	± 10	± 12	± 11	± 10	± 12	± 11	± 10	± 12	V
V_{OM}	Maximum peak output voltage swing $T_A = 25^\circ\text{C}$	± 12	± 13.5	± 12	± 12	± 13.5	± 12	± 12	± 13.5	± 12	± 12	± 13.5	± 12	V
ΔV_D	Large signal differential voltage amplification $T_A = 25^\circ\text{C}$	$V_O = \pm 10$ V, $R_L \geq 2$ k Ω	± 10	± 12	± 10	± 12	± 10	± 10	± 12	± 10	± 10	± 12	± 10	V/mV
B_1	Unity-gain bandwidth $T_A = 25^\circ\text{C}$	3			3			3			3			MHz
r_i	Input resistance $T_A = 25^\circ\text{C}$	10^{12}			10^{12}			10^{12}			10^{12}			Ω
CMRR	Common-mode rejection ratio $T_A = 25^\circ\text{C}$	70	86		80	86		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC} \pm / \Delta V_{IO}$) $T_A = 25^\circ\text{C}$	70	86		80	86		80	86		80	86		dB
I_{CC}	Supply current (per amplifier) $T_A = 25^\circ\text{C}$	1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8		mA
$V_{O1/2}$	Crosstalk attenuation $\Delta V_D = 100$, $T_A = 25^\circ\text{C}$	120			120			120			120			dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL080, TL081, TL082, TL083, TL084, and -40°C to 85°C for TL081A, TL082A, TL084A. Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.



TEXMATE

PM-45X & PM-45XU 4 1/2 DIGIT PANEL METERS

ACCURACY LCD METERS WITH 10 μ V RESOLUTION, TRUE DIFFERENTIAL INPUTS, ULTRA LOW POWER <25mW AT +5VDC, AND STANDARD MUX-BCD OR OPTIONAL PARALLEL BCD OUTPUTS

DESCRIPTION

The PM-45X and PM-45XU are truly unique and extremely versatile instruments. Believed to be the world's smallest and most energy efficient 4 1/2 Digit LCD Panel Meters, they nevertheless offer more high performance features than most larger and more expensive DPM's.

Both meters incorporate a crystal controlled 100KHz clock that provides an exceptionally high normal mode rejection of 120dB at multiples to 50/60Hz. Bipolar differential and single-ended DC voltages from $\pm 199.99\text{mV}$ to $\pm 1200.0\text{V}$ full scale can be measured and scaled in almost any known engineering unit. Provision has been made for signal offsetting and the capability of attenuating both high and low signal inputs. Resolution is $10\mu\text{V}$ over ± 19999 counts, and errors due to zero drift are virtually eliminated by autozeroing. Other modes of operation, selectable by the user, include an ohmmeter mode, current meter mode and ratiometric mode.

Multiplexed BCD data is available internally from a row of auxiliary solder pads. Both meters may be ordered with an internally mounted Tri-state Buffered Parallel BCD Output Board. This option, which is described in detail on a separate data sheet, can also be purchased for field retrofit.

The PM-45X features an ultra stable temperature compensated reference with selected low TC components. The PM-45XU is a derated economy priced model that provides all the features of the PM-45X but utilizes a standard reference, and components with less stringent specifications.

The true differential input capabilities and high 86dB common mode rejection ratio, combined with their low signal measurement range and high noise immunity, make these meters ideal for measuring various balanced transducers and bridge inputs. When measuring bridge circuits, long term drift of the excitation voltage can be compensated by using the ratiometric voltmeter mode of operation.

The proprietary high contrast, long life liquid crystal display provides excellent readability under high and low ambient light conditions. Since the meters normally draw only a small constant current (<25mW), operation from almost any DC power supply is simplified. If the supply has a stability of only 10%, a voltage dropping resistor in series with the meter is often sufficient. (See Application notes.)

SPECIFICATIONS

Input Configuration:	True differential and single-ended
Full Scale Ranges:	$\pm 199.99\text{mVDC}$ $\pm 1.9999\text{VDC}$ (standard) $\pm 19.999\text{VDC}$ $\pm 199.99\text{VDC}$ $\pm 1200.0\text{VDC}$ (max. Input Signal; higher voltages can be measured if voltage dividing resistors are located externally)
Input Impedance:	Exceeds $1000\text{M}\Omega$ on 200mV and 2V ranges. $10\text{M}\Omega$ on all other ranges
Input Protection:	$\pm 170\text{VDC}$ or 120VAC on 200mV and 2V ranges. $\pm 1200\text{VDC}$ or 850VAC on all other ranges
Normal Mode Rejection:	120dB at multiples of 50/60Hz
Common Mode Rejection:	86dB at DC; greater than 120dB at multiples of 50/60Hz
Common Mode Voltage:	-2.8V to $+2.8\text{V}$ (standard) $\pm 2.8\text{V}$ or more if differential dividers are used (see Typical Application Circuits and Connection Instructions)
Accuracy:	PM-45X $\pm (0.01\%$ of reading + 1 digit) $\pm (0.015\%$ of reading + 2 digits) for 200mV range. PM-45XU $\pm (0.015\%$ of reading + 2 digits). $\pm (0.02\%$ of reading + 3 digits) for 200mV range
Maximum Resolution:	$10\mu\text{V}$ over ± 19999 counts in 200mV range. $100\mu\text{V}$ over ± 19999 counts in 2V range
Temperature Coefficient:	PM-45X: 5PPM/ $^{\circ}\text{C}$ ratiometric. 20PPM/ $^{\circ}\text{C}$ using internal adjustable T.C. Reference. PM-45XU: 5PPM/ $^{\circ}\text{C}$ ratiometric. 50PPM/ $^{\circ}\text{C}$ using internal reference
Zero Stability:	Autozeroed $\pm 10\mu\text{V}$ at all ranges: $\pm 1\mu\text{V}/^{\circ}\text{C}$ Typical
Conversion Rate:	2.5 readings per second
Clock Frequency:	100KHz system clock derived from 200KHz quartz crystal controlled oscillator of 0.05% accuracy
Display:	0.48" LCD
Polarity:	Automatic; displays both "+" and "-" signs; polarity symbols may be blanked (see page 6)
Overload Indication:	When input exceeds full scale on any range being used, the most significant "1" digit and "+" or "-" symbol is displayed with all other digits blank
Power Requirements:	Low ripple $+4.5\text{V}$ to $+5.5\text{VDC}$ at 3mA to 5mA
Warmup Time:	10 seconds to specified accuracy
Operating Temperature:	0°C to $+60^{\circ}\text{C}$

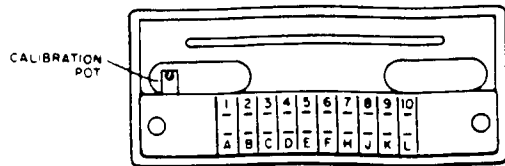
ORDERING INFORMATION

	Order Part No.		Order Part No.
Standard High Accuracy 4 1/2 Digit Panel Meter (2V Range)	PM-45X	Range Change Kits: (matched resistors for user installation)	
Standard Utility Version 4 1/2 Digit Panel Meter (2V Range)	PM-45XU	200mV Range	VG-200MV
PM-45X W/Tri-State Parallel BCD Output	PM-45XBCD	20V Range	VKA-0020V
PM-45XU W/Tri-State Parallel BCD Output	PM-45XUBCD	200V Range	VKA-0200V
Retrofit Tri-State Parallel BCD Board for PM-45X/PM-45XU	PM-45XBCDO	1200V Range	VKA-1200V
Accessories: Edge Connector (20 pin solder tabs)	CN-L10	Optional Cases*: (see back page for details)	
Options: Factory Installed 200mV Range	VG-200MVFI	End Mount Case (twin meter mounting)	EM-CASECLR
Factory Installed 20V Range	VFA-0020V	Center Mount Case (multiple array mounting)	CM-CASECLR
Factory Installed 200V Range	VFA-0200V	Slim Bezel Case (supplied as standard)	SL-CASECLR
Factory Installed 1200V Range	VFA-1200V		
Factory Installed Special Scaling (Specify input signal, the span, and digital reading required, e.g. 1 to 5V input to display 0 to 10,000; 4 to 20mA input to display 0 to 15,000; 0 to 50mA input to display -1,000 to +8,000)	VS 4 5		

*Meters purchased prior to August 1989 require cases with a polarizer bonded to the rear side of the lens. To order these cases, use the following part numbers EM-CASELCD; CM-CASELCD; SL-CASELCD.

CONNECTOR PINOUTS

The Texmate Model PM-45X/PM-45XU is interconnected by means of a standard PC board edge connector having two rows of 10 pins, spaced on 0.156" centers. The optional parallel BCD Output is interconnected by a standard PC board edge connector having two rows of 13 pins spaced on 0.1" centers. (A standard 26 pin, PCB to Ribbon Cable Connector is recommended.) Connectors are available from Texmate, or from almost any connector manufacturer.

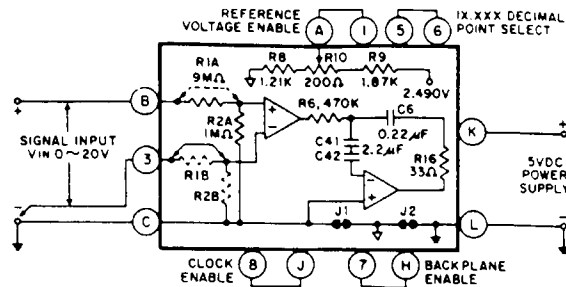


REAR VIEW OF METER CASE

A — Reference Output	1 — Reference Input
B — Signal High Input	2 — Offset Voltage Output
C — Analog Common	3 — Signal Low Input
D — Decimal Select (1XXX.X)	4 — Decimal Select (1XX.XX)
E — Decimal Select (1.XXXX)	5 — Decimal Select Common
F — Decimal Select (.1XXXX)	6 — Decimal Select (1X.XXX)
H — Back Plane Output	7 — Back Plane Input/Display Test
J — Clock Output	8 — Clock Input
K — +5VDC System Power Input	9 — Busy Output
L — Power Ground Input	10 — Run/Hold

CAUTION: This meter employs high impedance CMOS inputs. Although internal protection has been provided for several hundred volt overloads, the meter will be destroyed if subjected to the high kilovolts of static discharge that can be produced in low humidity environments. Always handle the meter with ground protection.

FUNCTIONAL DIAGRAM



SINGLE-ENDED METER — >2V RANGES WITH VOLTAGE DIVIDER

1) High single ended voltages, up to 1200V max. can be measured and/or scaled by installing the appropriate voltage dividing resistors in R1A and R2A positions. Matched dividing resistors for the 20V (1/10), 200V (1/100), and 1200V (1/1000) ranges are available from Texmate. 2) Connect Pin 3 to the nearest end of the signal source ground to avoid possible errors caused by ground loop currents.

PIN DESCRIPTIONS

Pin A — Reference Output: Internal precision voltage reference. Standard output is 1.0000V, adjustable $\pm 5\%$ by R10 potentiometer. Usable voltages from 0.05V to 2.49V for special high impedance scaling can be obtained by changing the value of internal dividing resistors R8 and R9. The primary reference voltage of the PM-45X is trimmed by potentiometer R20 to obtain the optimum compensated temperature coefficient. This temperature compensation network is omitted on the PM-45XU utility meter. Please read CALIBRATION PROCEDURE (Page 7).

Pin B — Signal High Input: Pin B is the signal high input for all input signal ranges. When attenuation is not required the resistor position R1A must be shorted by a jumper. Dividing resistors may be mounted internally in R1A and R2A positions to attenuate voltages up to 1200V max. Matched dividing resistors for the 20V (1/10), 200V (1/100) and 1200V (1/1000) ranges are available from Texmate. Shunt resistors for current measurements up to 200mA may also be internally mounted in the R2A position. The current loop is then applied to Pin B and returned through Analog Common Pin C.

Pin C — Analog Common: Pin C is signal return common for differential inputs, ratiometric inputs, or external reference inputs. For single-ended inputs, Signal Low Input Pin 3 must be connected to Analog Common Pin C. To minimize any errors caused by ground loop currents it is recommended that this connection be made as close as possible to the input signal source ground. (See Typical Application Circuits and Connection Instructions, Pages 4-6.)

Pins D, E, F, 4 and 6 — Decimal Select: Decimal points may be displayed as required by connecting the appropriate pin to Decimal Select Common Pin 5. Any number of decimal points can be turned on at the same time. An open circuit will turn off the decimal points. However, static current pickup and/or PCB leakage of more than 100nA can cause decimal points to turn on undesirably. Therefore, it is recommended that the unused decimal points be connected to Back Plane Output Pin H either directly or by a resistor of less than 5M Ω to insure an off condition. **CAUTION:** Any DC component introduced to the display drive circuitry can, in time, cause permanent damage. PLEASE READ PAGES 7 AND 8 FOR A DETAILED EXPLANATION OF LCD OPERATION.

Pin H — Back Plane Output: Liquid crystal displays are operated from an AC signal. Back Plane Output Pin H provides a square-wave signal of 60~160HZ that must be connected by the user to back plane input Pin 7 for normal operation. Pin 7 is internally connected to the LCD back plane which is the common base of the LCD capacitance structure. Those segments that are driven 180° out-of-phase with the back plane will turn on. Those segments that are driven in-phase with the back plane will turn off. PLEASE READ PAGES 7 AND 8 FOR A DETAILED EXPLANATION OF LCD OPERATION.

Pin J — Clock Output: A quartz crystal controlled oscillator provides a stable clock signal output of 100KHz.

Pin K — +5VDC System Power Input: The meter requires a low ripple DC power supply of 4.5V to 5.5VDC at 3mA to 5mA. The low power consumption of only 25mW enables the meter to be easily operated from various power sources with simple voltage regulating circuitry. The positive terminal of the power supply should be connected to Pin K.

Pin L — Power Ground Input: Negative terminal of the +5VDC power supply should be connected to Pin L. All digital signals, Display Test, and Run/Hold should be returned to this ground point. Pin L is internally connected to Analog Common Pin C.

Pin 1 — Reference Input: Reference voltage input for A to D converter. Normally supplied from Pin A. An external reference source referred to Pin C may be used instead. Pin 1 may be used as an input for ratiometric measurements. Minimum usable voltage is .05VDC, with a maximum voltage of 4.0V. For ratiometric operation: Displayed Reading = 10000 X (Signal Input Voltage \div Reference Input Voltage). The maximum signal input

voltage is $\pm 4V$. Higher voltages must be scaled down through a voltage divider. Reference input voltage must remain stable during measurement period.

Pin 2 — Offset Voltage Output: 0 to +2.490V is available with the addition of a $\frac{1}{4}$ " 20K Ω to 100K Ω pot in the R15 position on the printed circuit board. The offset voltage is derived from the internal precision voltage reference and is available for applications requiring a zero offset such as 4~20mA receiver and temperature measurements.

Pin 3 — Signal Low Input: Pin 3 is the signal low input for all input signals. A special feature of the meter is the provision for dividing resistors to be mounted internally in the R1B and R2B positions. This enables low signal inputs up to 1200V max to be attenuated, which is particularly useful when measuring small differential signals with a large common mode voltage. Matched dividing resistors for the 20V (1/10), 200V (1/100) and 1200V (1/1000) ranges are available from Texmate. Differential current measurements up to 200mA may also be made by internally mounting shunt resistors in the R2B position. The current loop is then applied to Pin B and returned through Analog Common Pin C. When attenuation is not required the resistor position R1B must be shorted by a jumper.

Pin 5 — Decimal Select Common: Pin 5 is 180° out-of-phase with back plane output Pin H. Thus it serves as a common for the decimal select Pins D, E, F, 4 and 6. To turn on any required decimal point, connect the appropriate Decimal Select Pin to Decimal Select Common Pin 5.

Pin 7 — Back Plane Input/Display Test: Pin 7 is connected to the display's back plane which forms the common base of the LCD capacitance structure. Join Pin 7 to back plane output Pin H for normal operation. For Display Test connect Pin 7 instead to Power Ground Pin L and all operative segments will turn on, indicating +18888. **CAUTION:** The Display Test function is only intended for momentary operation. Continuous application of Display Test will, in time, damage the display. SEE PAGES 7 AND 8 FOR A DETAILED EXPLANATION OF LCD OPERATION.

Pin 8 — Clock Input: Normally Pin 8 is connected to the 100KHz clock output from Pin J, thereby providing the optimum rejection of 50/60 Hz noise. However, an external clock source may be used instead (5V referenced to power ground with a recommended duty cycle of 50%). Minimum frequency is 10KHz, and maximum frequency is 1MHz (12.5 readings per sec.). For inputs below 100KHz or above 300KHz, changes to the integrator time constant and some component values are necessary.

Pin 9 — Busy Output: Pin 9 goes to logic "1" at the beginning of the signal integration and remains at "1" until the first clock pulse after the zero-crossing is detected at the completion of deintegration. In addition to its use as a Busy or End-of-Conversion signal, the output on Pin 9 can be used in some control applications to indicate the digital reading of the meter as a function of time or clock pulses. Displayed Reading is equal to the total clock pulses during Busy less 10,000, or total elapsed time during Busy, less 100 milliseconds if the clock frequency is 100KHz.

Pin 10 — Run/Hold: If Pin 10 is left open (or connected to +5VDC System Power Input Pin K for logic control purposes), the meter will operate in a free-running mode. Under control of the internal 100KHz quartz crystal clock, readings will be updated every 400mS (2.5 per sec.). If Pin 10 is connected to Power Ground Input Pin L (logic low), the meter will continue the measurement cycle that it is doing, then latch up and continuously hold the reading obtained as long as Pin 10 is held low. If Pin 10 is released from Pin L (Pin 10 then goes logic high) for more than 300ns and returned to Pin L (logic low), the meter will complete one conversion, update, and then hold the new reading. For all practical purposes, a manually actuated normally closed pushbutton switch will provide sufficient timing for "press-to-update" operation.



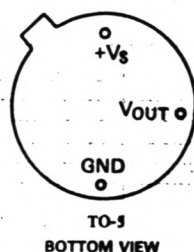
High Precision 10V IC Reference

AD581*

FEATURES

- Laser-Trimmed to High Accuracy:
10.000 Volts $\pm 5\text{mV}$ (L and U)
- Trimmed Temperature Coefficient:
5ppm/ $^{\circ}\text{C}$ max, 0 to $+70^{\circ}\text{C}$ (L)
10ppm/ $^{\circ}\text{C}$ max, -55°C to $+125^{\circ}\text{C}$ (U)
- Excellent Long-Term Stability:
25ppm/1000 hrs. (Noncumulative)
- Negative 10 Volt Reference Capability
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability
- 3-Terminal TO-5 Package

AD581 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at $+25^{\circ}\text{C}$ as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/ $^{\circ}\text{C}$ guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical Zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750 μA . The long-term stability of the band-gap design is equivalent or superior to selected Zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to $+70^{\circ}\text{C}$; the AD581S, T, and U are specified for the -55°C to $+125^{\circ}\text{C}$ range. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

PRODUCT HIGHLIGHTS

- Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of $\pm 7.25\text{mV}$ from 0 to $+70^{\circ}\text{C}$, while the AD581U guarantees $\pm 13\text{mV}$ maximum total error without external trims from -55°C to $+125^{\circ}\text{C}$.
- Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
- The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
- Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 13 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.

SPECIFICATIONS (@ $V_{IN} = +15\text{V}$ and 25°C)

Model	AD581J			AD581K			AD581L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10.000V output)			± 30			± 10			± 5	mV
OUTPUT VOLTAGE CHANGE Maximum Deviation from + 25°C Value, T _{min} to T _{max} (Temperature Coefficient)			± 13.5			± 4.75			± 2.25	mV
			30			15			5	ppm/°C
LINE REGULATION 15V ≤ V _{IN} ≤ 30V			3.0 (0.002)			3.0 (0.002)			3.0 (0.002)	mV %/V
13V ≤ V _{IN} ≤ 15V			1.0 (0.005)			1.0 (0.005)			1.0 (0.005)	mV %/V
LOAD REGULATION 0 ≤ I _{OUT} ≤ 5mA		200	500		200	500		200	500	μV/mA
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
TURN-ON SETTLING TIME TO 0.1%		200			200			200		μs
NOISE (0.1 to 10Hz)		50			50			50		μV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT Source (t _r = + 25°C Source T _{min} to T _{max} Sink T _{min} to T _{max} Sink - 55°C to + 85°C	10 5 5 -			10 5 5 -			10 5 5 -			mA mA μA mA
TEMPERATURE RANGE Specified Operating	0 - 65	+ 70 + 150		0 - 65	+ 70 + 150		0 - 65	+ 70 + 150		°C °C
PACKAGE OPTION ¹ TO-5 (H-018)	AD581JH			AD581KH			AD581LH			

Model	AD581S			AD581T			AD581U			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10.000V output)			± 30			± 10			± 5	mV
OUTPUT VOLTAGE CHANGE Maximum Deviation from + 25°C Value, T _{min} to T _{max} (Temperature Coefficient)			± 30			± 15			± 10	mV
			30			15			10	ppm/°C
LINE REGULATION 15V ≤ V _{IN} ≤ 30V			3.0 (0.002)			3.0 (0.002)			3.0 (0.002)	mV
13V ≤ V _{IN} ≤ 15V			1.0 (0.005)			1.0 (0.005)			1.0 (0.005)	%/V
LOAD REGULATION 0 ≤ I _{OUT} ≤ 5mA		200	500		200	500		200	500	μV/mA
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
TURN-ON SETTLING TIME TO 0.1%		200			200			200		μs
NOISE (0.1 to 10Hz)		50			50			50		μV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT Source (t _r = + 25°C) Source T _{min} to T _{max} Sink T _{min} to T _{max} Sink -55°C to + 85°C	10 5 200 5			10 5 200 5			10 5 200 5			mA mA μA mA
TEMPERATURE RANGE Specified Operating	55 65	+ 125 + 150		55 65	+ 125 + 150		55 65	+ 125 + 150		°C °C
PACKAGE OPTION ² TO-5 (H-018)	AD581SH			AD581TH			AD581UH			

NOTES

¹See Figure 7

²See Section 13 for package outline information

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAX RATINGS

Input Voltage V_{IN} to Ground	40V
Power Dissipation ($t_r = +25^{\circ}\text{C}$)	600mW
Operating Junction Temperature Range	-55°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering 10sec)	$+300^{\circ}\text{C}$
Thermal Resistance Junction-to-Ambient	150 $^{\circ}\text{C}/\text{W}$

*Covered by Patent Nos. 3,887,863; RE 30,586

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., $10\text{ppm}/^\circ\text{C}$. However, because of non-linearities in temperature characteristics, which originated in standard Zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 4. Five-point measurement of each device guarantees the error band over the -55°C to $+125^\circ\text{C}$ range; three-point measurement guarantees the error band from 0 to $+70^\circ\text{C}$.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at $+25^\circ\text{C}$; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is $\pm 10\text{mV}$, the temperature error band is $\pm 15\text{mV}$, thus the unit is guaranteed to be 10.000 volts $\pm 25\text{mV}$ from -55°C to $+125^\circ\text{C}$).

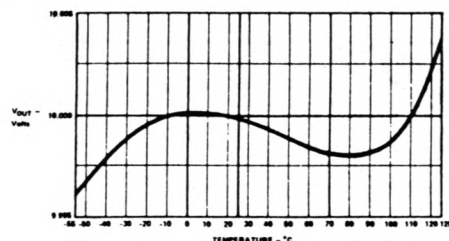


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device are shown in Figure 5. Source current is displayed as negative current in the figure; sink current is displayed as positive current in the figure.

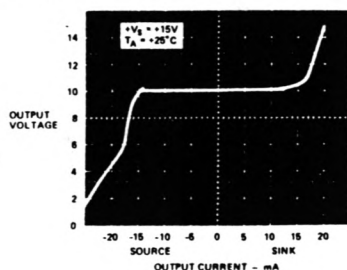


Figure 5. AD581 Output Voltage vs. Sink and Source Current

rent is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA ; when shorted to $+15$ volts, the sink current goes to about 20mA .

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ± 1 millivolt is about $180\mu\text{s}$, and there is no long thermal tail appearing after the point.

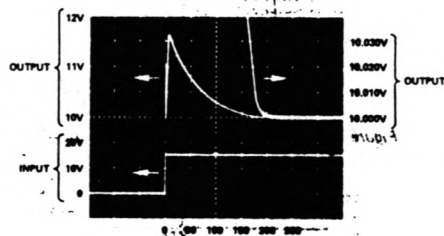


Figure 6. Output Settling Characteristic

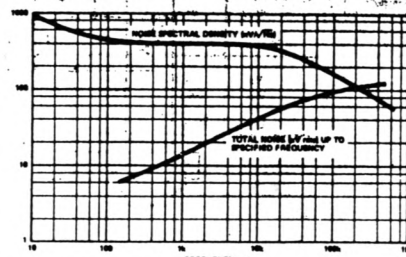


Figure 7. Spectral Noise Density and Total rms Noise vs. Frequency

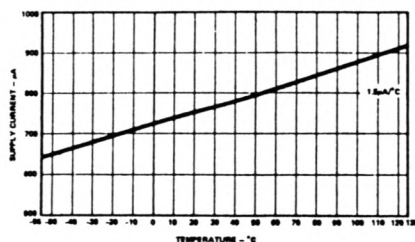


Figure 8. Quiescent Current vs. Temperature

Applying the AD581

APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 30 volts.

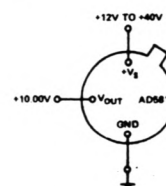


Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a millivolt (calibrated to a main system reference). System calibration may also require a reference slightly different from 10.00 volts. In either case, the optional trim circuit shown in Figure 2 can offset the output by up to ± 30 millivolts (with the 22Ω resistor), if needed, with minimal effect on other device characteristics.

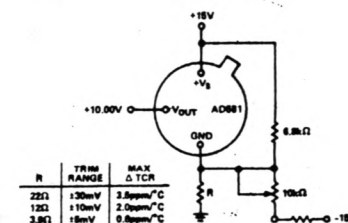


Figure 2. Optional Fine Trim Configuration

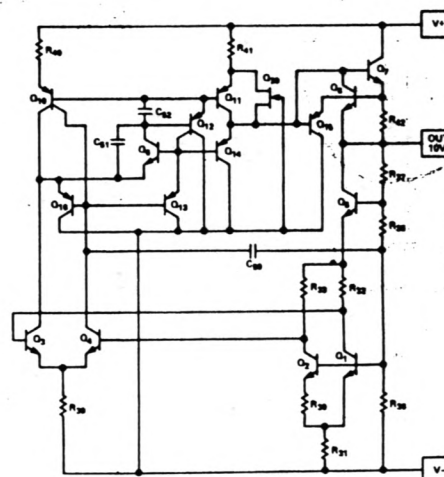


Figure 3. Simplified Schematic

PRECISION HIGH CURRENT SUPPLY

The AD581 can be easily connected with power pnp or power darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 9 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1 μ F capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

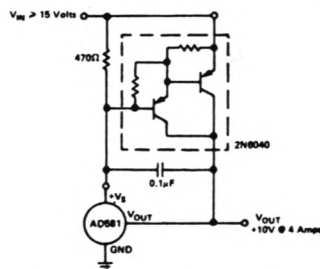


Figure 9. High Current Precision Supply

CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V \pm 5% as shown in Figure 10. The 560 Ω resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that the other bandgap references, without current sink capability, may be damaged by use in this circuit configuration.

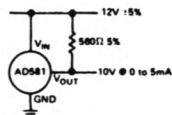


Figure 10. 12-Volt Supply Connection

THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

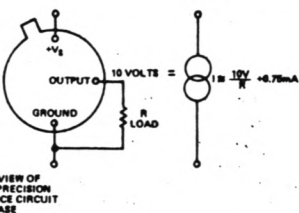


Figure 11. A Two-Component Precision Current Limiter

NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "Zener" mode to provide a precision -10.00 volt reference. As shown in Figure 13, the V_IN and V_OUT terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V_OUT. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.25 Ω typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD581 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V_IN and V_OUT are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA.

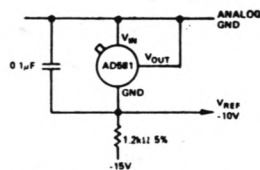


Figure 12. Two-Terminal -10 Volt Reference

TYPES SN55452B, SN75452B DUAL PERIPHERAL POSITIVE-NAND DRIVERS

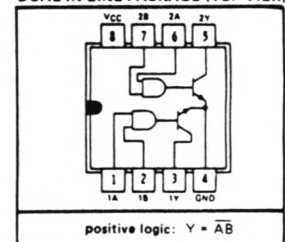
logic

FUNCTION TABLE
(EACH DRIVER)

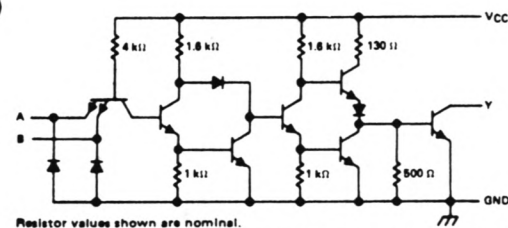
A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level, L = low level

SN55452B ... JG
SN75452B ... JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN55452B			SN75452B			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -12 mA		-1.2 -1.5	V _{CC} = MIN, I _I = -12 mA		-1.2 -1.5	V
I _{OH}	High-level output current	V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 30 V		300	V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 30 V		100	μA
V _{OL}	Low-level output voltage	V _{CC} = MIN, I _{OL} = 100 mA, V _{IH} = 2 V		0.25 0.5	V _{CC} = MIN, I _{OL} = 100 mA, V _{IH} = 2 V		0.25 0.4	V
		V _{CC} = MIN, I _{OL} = 300 mA, V _{IH} = 2 V		0.5 0.8	V _{CC} = MIN, I _{OL} = 300 mA, V _{IH} = 2 V		0.5 0.7	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1	V _{CC} = MAX, V _I = 5.5 V		1	mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.4 V		40	V _{CC} = MAX, V _I = 2.4 V		40	μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V		-1.1 -1.6	V _{CC} = MAX, V _I = 0.4 V		-1.1 -1.6	mA
I _{CC}	Supply current, outputs high	V _{CC} = MAX, V _I = 0 V		11 14	V _{CC} = MAX, V _I = 0 V		11 14	mA
I _{CC}	Supply current, outputs low	V _{CC} = MAX, V _I = 5 V		56 71	V _{CC} = MAX, V _I = 5 V		56 71	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output		26	35	ns
t _{PHL}	Propagation delay time, high-to-low-level output		24	35	ns
t _{TLH}	Transition time, low-to-high-level output		5	8	ns
t _{THL}	Transition time, high-to-low-level output		7	12	ns
V _{OH}	High-level output voltage after switching	V _S = 20 V, I _O = 300 mA, See Figure 4		V _S - 6.5	mV



Voltage Comparators

LM139/ 239/ 339, LM139A/239A/339A, LM2901, LM3302 Low Power Low Offset Voltage Quad Comparators General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic—where the low power drain of the LM339 is a distinct advantage over standard comparators.

Advantages

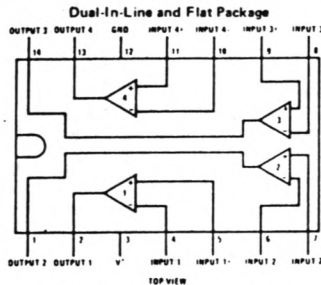
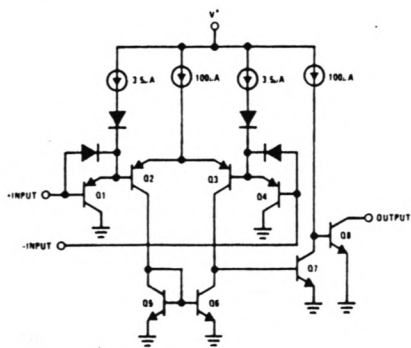
- High precision comparators
- Reduced V_{OS} drift over temperature

- Eliminates need for dual supplies
- Allows sensing near gnd
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Wide single supply voltage range or dual supplies
LM139 series, 2 VDC to 36 VDC or
LM139A series, LM2901 ± 1 VDC to ± 18 VDC
LM3302 2 VDC to 28 VDC
or ± 1 VDC to ± 14 VDC
- Very low supply current drain (0.8 mA) — independent of supply voltage (2 mW/comparator at ± 5 VDC)
- Low input biasing current 25 nA
- Low input offset current ± 5 nA
- Low input offset voltage ± 3 mV
- Input common-mode voltage range includes gnd
- Differential input voltage range equal to the power supply voltage
- Low output 250 mV at 4 mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

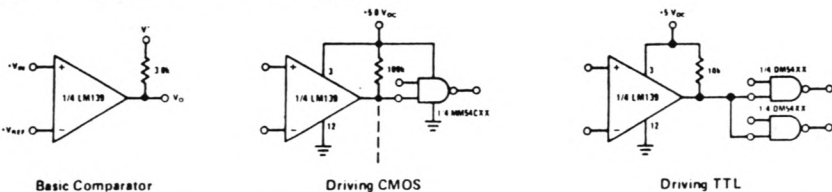
Schematic and Connection Diagrams



Order Number LM139J, LM139AJ,
LM239J, LM239AJ, LM339J,
LM339AJ, LM2901J or LM3302J
See NS Package J14A

Order Number LM339N, LM339AN,
LM2901N or LM3302N
See NS Package N14A

Typical Applications ($V^+ = 5.0$ VDC)



Absolute Maximum Ratings

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 VDC or ± 18 VDC	28 VDC or ± 14 VDC
Differential Input Voltage	36 VDC	28 VDC
Input Voltage	-0.3 VDC to +36 VDC	-0.3 VDC to +28 VDC
Power Dissipation (Note 1)	570 mW	570 mW
Modded DIP	900 mW	Continuous
Carrier DIP	800 mW	50 mA
Flat Pack	50 mA	Continuous
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3$ VDC), (Note 3)	50 mA	50 mA
Operating Temperature Range	0°C to +70°C -25°C to +85°C -40°C to +125°C -55°C to +150°C -65°C to +150°C 300°C	-40°C to +85°C -55°C to +150°C 300°C
Storage Temperature Range		
Lead Temperature (Soldering, 10 seconds)		

Electrical Characteristics ($V^+ = 5$ VDC, Note 4)

PARAMETER	CONDITIONS	LM139A	LM239A, LM339A	LM139	LM239, LM339	LM2901	LM3302	UNITS
Input Offset Voltage	$T_A = 25^\circ\text{C}$, (Note 5)	MIN 1.0	MIN 1.0	MIN 1.0	MIN 1.0	MIN 1.0	MIN 1.0	mVDC
Input Bias Current	$I_{IN(+)} \text{ or } I_{IN(-)}$ with Output in Linear Range, $T_A = 25^\circ\text{C}$, (Note 5)	TYP 25	TYP 25	TYP 25	TYP 25	TYP 25	TYP 25	nADC
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25^\circ\text{C}$	MAX 100	MAX 100	MAX 100	MAX 100	MAX 100	MAX 100	nADC
Input Common-Mode Voltage Range	$T_A = 25^\circ\text{C}$, (Note 6)	0	0	0	0	0	0	VDC
Supply Current	$R_L = \infty$ on all Comparators, $T_A = 25^\circ\text{C}$ $R_L = \infty$, $V^+ = 30$ V, $T_A = 25^\circ\text{C}$ $R_L \geq 15$ k Ω , $V^+ = 15$ VDC (T ₉₀) Support Load V_O Swing), $T_A = 25^\circ\text{C}$ $V_{IN} = \text{TTL Logic Swing}$, $V_{REF} = 1.4$ VDC, $V_{RL} = 5$ VDC, $R_L = 5.1$ k Ω , $T_A = 25^\circ\text{C}$	0.8	0.8	0.8	0.8	0.8	0.8	mA
Voltage Gain	$V_{RL} = 5$ VDC, $R_L = 5.1$ k Ω , $T_A = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$, (Note 7)	200	200	200	200	200	200	mV/mV
Large Signal Response Time	$V_{IN} = 1$ VDC, $V_{RL} = 5$ VDC, $R_L = 5.1$ k Ω , $T_A = 25^\circ\text{C}$	300	300	300	300	300	300	ns
Response Time	$V_{IN} = 1$ VDC, $V_{RL} = 5$ VDC, $R_L = 5.1$ k Ω , $T_A = 25^\circ\text{C}$	1.3	1.3	1.3	1.3	1.3	1.3	μ s
Output Sink Current	$V_{IN} = 1$ VDC, $V_{RL} = 5$ VDC, $R_L = 5.1$ k Ω , $T_A = 25^\circ\text{C}$	60	60	60	60	60	60	mA
Saturation Voltage	$V_{IN} = 1$ VDC, $V_{RL} = 5$ VDC, $R_L = 5.1$ k Ω , $T_A = 25^\circ\text{C}$	250	250	250	250	250	250	mVDC
Output Leakage Current	$V_O = 5$ VDC, $T_A = 25^\circ\text{C}$	0.1	0.1	0.1	0.1	0.1	0.1	nADC

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM139A				LM239A, LM339A				LM139				LM239, LM339				LM2901				LM3302				UNITS
		MIN	TYP	MAX		MIN	TYP	MAX		MIN	TYP	MAX		MIN	TYP	MAX		MIN	TYP	MAX		MIN	TYP	MAX		
Input Offset Voltage	(Note 8)		4.0				4.0				9.0				9.0				9	15			40			mVDC
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$		± 100				± 150				± 100				± 150				50	200			300			nADC
Input Bias Current	$I_{IN(+)} \text{ or } I_{IN(-)}$ with Output in Linear Range		300				400				300				400				200	500			1000			nADC
Input Common-Mode Voltage Range			$V^+ - 2.0$	0		$V^+ - 2.0$	0				$V^+ - 2.0$	0		$V^+ - 2.0$	0			$V^+ - 2.0$	0			$V^+ - 2.0$	0			VDC
Saturation Voltage	$V_{IN(+)} \geq 1 \text{ VDC}$; $V_{IN(-)} = 0$; $I_{SINK} \leq 4 \text{ mA}$		700				700				700				700				400	700			700			mVDC
Input Leakage Current	$V_{IN(+)} \geq 1 \text{ VDC}$; $V_{IN(-)} = 0$; $V_O = -30 \text{ VDC}$		1.0				1.0				1.0				1.0				1.0				1.0			μADC
Differential Input Voltage	Keep all V_{IN} 's $\geq 0 \text{ VDC}$ for V^- , if used. (Note 8)		36				36				36				36				0				36			VDC

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the output keeps the chip dissipation very small ($P_D \leq 100 \text{ mW}$), provided the output transitions are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+ .

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 VDC (at 25°C).

Note 4: These specifications apply for $V^+ = 5 \text{ VDC}$ and $-65^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise stated. With the LM239/LM239A, all temperature specifications are limited to $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, the LM339/LM339A temperature specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$, and the LM2901, LM3302 temperature range is $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

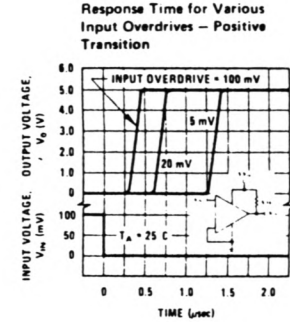
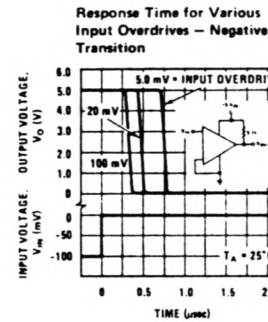
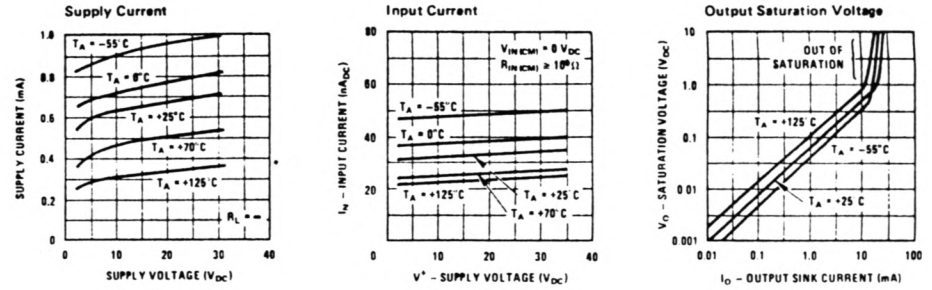
Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5\text{V}$, but either or both inputs can go to $+30 \text{ VDC}$ without damage (25V for LM3302).

Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 n can be obtained, see typical performance characteristics section.

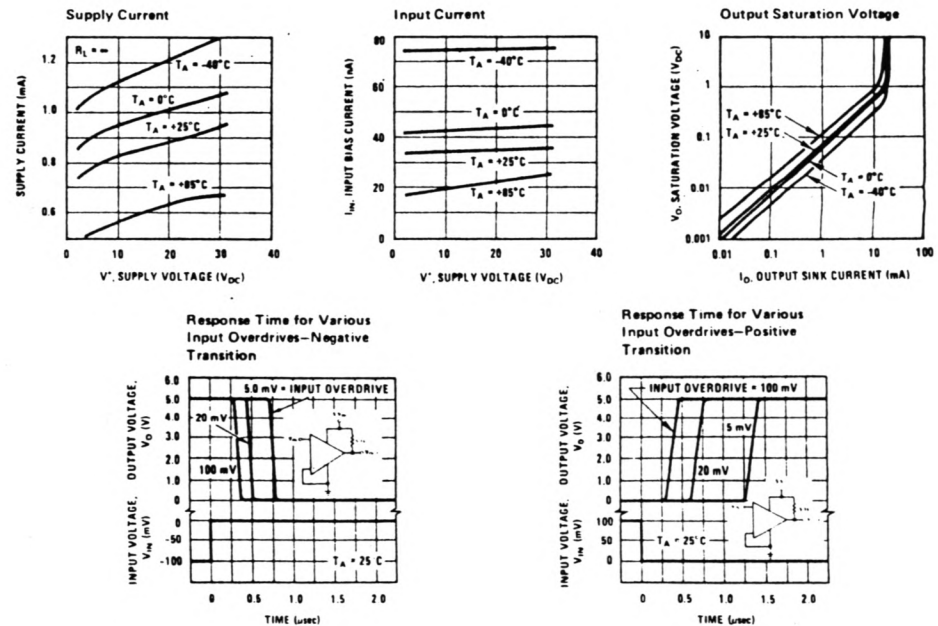
Note 8: Positive excursion of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 VDC (or 0.3 VDC below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, $V_O \approx 1.4 \text{ VDC}$; $R_S = 0\Omega$ with V^+ from 5 VDC and over the full input common-mode range (0 VDC to $V^+ - 1.5 \text{ VDC}$).

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302



Typical Performance Characteristics LM2901



TELEDYNE SOLID STATE

SERENDIP® AC SOLID STATE RELAY

OPTICALLY ISOLATED
1.0 A rms

FEATURES/BENEFITS

- Optical isolation – Isolates control elements from load transients.
- Floating output – Eliminates ground loops and signal ground noise.
- Zero voltage turn on, Zero current turn off – Minimum switching transient noise and extremely low EMI.
- Low off state leakage current – For high off state impedance.
- Switches high and low voltages and currents – Switches voltages from 20 to 250 Vrms Switches currents from 10 to 1000 mArms
- High noise immunity – Control circuit cannot be triggered by output switching noise.
- High dielectric strength – For safety and for protection of control and signal level circuits.
- Meets design requirements of UL, CSA, and VDE 8884 – Highest quality for commercial/industrial part. Approval pending.
- Switches resistive or reactive loads to 0.2 P.F. – Broad Load Switching Capability.

DESCRIPTION

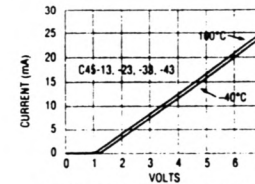
The C45 Series employs back-to-back photo SCRs and a patented zero crossing circuit. The tight zero switch window ensures reliable transient free switching of AC loads and very low EMI and noise generation. Optical isolation of control from output prevents switching noise from coupling into signal, power and ground distribution systems for noise free power switching. This series of solid state relays will switch from 10 ma to 1.0 amp rms at 280 Vrms. The C45 is packaged in a low profile 16 pin Dual In-Line package for PC mounting with minimum space utilization.

PART NUMBER	RELAY DESCRIPTION
C45	Solid State Relay with Terminals For Through Hole Mount
SC45	Solid State Relay with Terminals For Surface Mount

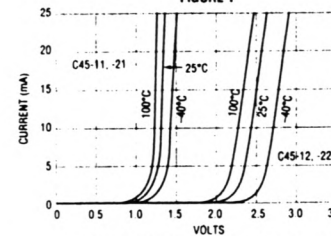
ELECTRICAL SPECIFICATIONS (25°C UNLESS OTHERWISE SPECIFIED)				
INPUT SPECIFICATIONS (See Figures 1 & 2)				
	MIN.	MAX.	UNITS	
Input Current (See Note 4)	C45-11, -21	5.0	50.0	ma
	C45-12, -22	10.0	50.0	ma
	C45-13, -23	N/A		
	C45-11, -21	N/A		
Input Voltage (See Note 4)	C45-12, -22	N/A		
	C45-13, -23	3.5	7.0	volts
	C45-11, -21			
	C45-12, -22			
Turn Off Current	C45-11, -21		10.0	µA
	C45-12, -22			
Turn On Current	C45-11, -21	5.0	50.0	ma
	C45-12, -22	10.0	50.0	ma
Turn Off Voltage	C45-13, -23		0.5	volts
	C45-13, -23	3.5		volts
Reverse Voltage Protection				
OUTPUT SPECIFICATIONS (See Notes 2 & 3)				
Load Current (See Figure 4)		0.01	1.0	Arms
Load Voltage Rating			280	Vrms
Frequency Range			47	650 Hz
On State Voltage Drop at Rated Current			1.5	Vrms
Zero Voltage Turn On			10	Vpeak
Surge Current Rating (non-repetitive 20 ms maximum) (See Figure 3 & Note 1)			8	A
Off State Leakage at Maximum Operating Voltage			1.0	mArms
Turn-On Time			1/2	cycle
Turn-Off Time			1/2	cycle
Over Voltage Rating	C45-11, -12, -13		400	Vpeak
	C45-21, -22, -23		500	Vpeak
Dielectric Strength (Input to Output)			4000	Vrms
Isolation (Input to Output)			10 ⁹	Ohms
Capacitance (Input to Output)			10	pF
Off State dv/dt			100	V/µsec
Fusing I ² T (1 ms)			5.0	A ² S
Output SCR's Dissipation Factor			1.0	Watt/A
Output SCR Temperature (T _J Maximum)			125	°C
Thermal Resistance	θ _{JA}		60	°C/W
	θ _{GC}		35	°C/W

SERIES C45

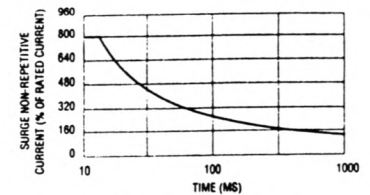
CHARACTERISTIC CURVES



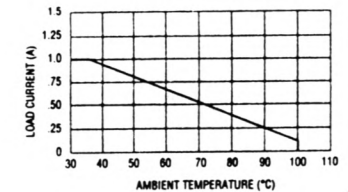
TYPICAL CONTROL CURRENT VS. VOLTAGE
FIGURE 1



TYPICAL CONTROL CURRENT VS. VOLTAGE
FIGURE 2

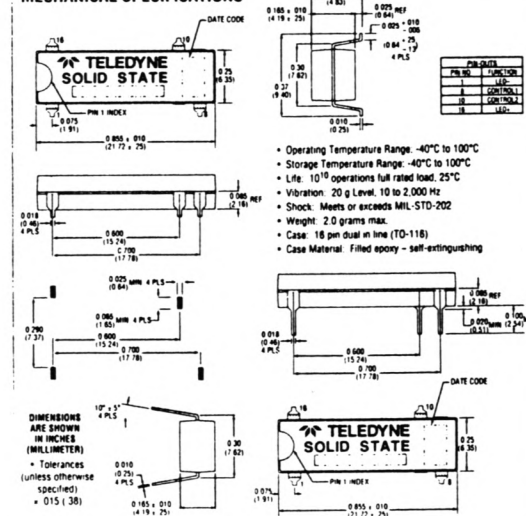


SURGE CURRENT VS. DURATION
FIGURE 3



LOAD CURRENT VS. TEMPERATURE
FIGURE 4

MECHANICAL SPECIFICATIONS



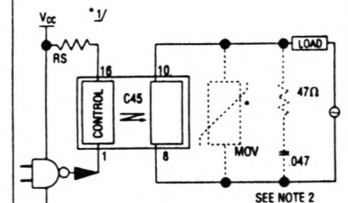
NOTES:

1. SCR may lose blocking capability during and after surge until T_J falls below 100°C maximum.
2. RC snubber is recommended but is not required.
3. Minimum Load Power Factor = 0.2 (Capacitive or Inductive). Lower power factors will damage relay.
4. Operation at load frequencies above 70 Hz requires increased input signal. Minimum input voltage is 5 Vdc for C45-13, -23. Minimum input current is 7.5 ma for C45-11, -21 and minimum input current is 15 ma for C45-12, -22.

6/93

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

TYPICAL INTERFACE TO 5V LOGIC (with suggested transient voltage and dv/dt suppression, if required)



*1/ Series resistor required

*USE THE TABLE BELOW FOR SELECTION OF PROPER METAL OXIDE VARISTOR (MOV)

MAXIMUM CONTINUOUS LINE VOLTAGE RATING	TRANSIENT (PEAK) RATING OF RELAY	TELEDYNE MOV P/N
140 Vac	400	970-1
250 Vac	600	970-2

(SEE 970 SERIES DATA SHEET FOR FURTHER INFORMATION ON MOV'S)

FIGURE 5

© 1993
TELEDYNE SOLID STATE
12525 Dopline Avenue
Houston, California 90230
(213) 777-0077

LM193/LM293/LM393, LM193A/LM293A/LM393A, LM2903

Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Advantages

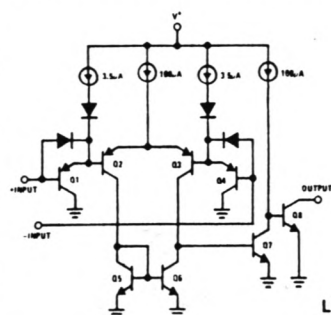
- High precision comparators
- Reduced V_{OS} drift over temperature

- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

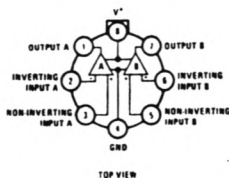
Features

- Wide single supply Voltage range or dual supplies 2.0 V_{DC} to 36 V_{DC}
 $\pm 1.0\text{ V}_{\text{DC}}$ to $\pm 18\text{ V}_{\text{DC}}$
- Very low supply current drain (0.8 mA)—independent of supply voltage (1.0 mW/comparator at 5.0 V_{DC})
- Low input biasing current 25 nA
- Low input offset current $\pm 5\text{ nA}$
and maximum offset voltage $\pm 3\text{ mV}$
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

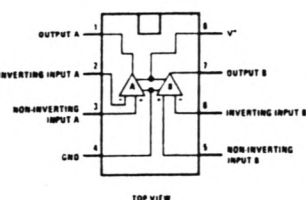
Schematic and Connection Diagrams



Metal Can Package



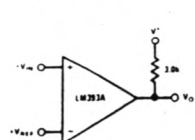
Dual-In-Line Package



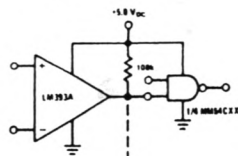
Order Number LM193H, LM193AH,
LM293H, LM293AH, LM393H or LM393AH
See NS Package H08C

Order Number LM393N,
LM393AN, or LM2903N
See NS Package N08B

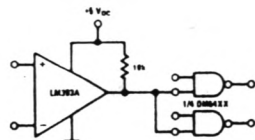
Typical Applications ($V^+ = 5.0\text{ V}_{DC}$)



Basic Comparator



Driving CMOS



Driving_TTL

PARAMETER	CONDITIONS	LM193A		LM293A, LM393A		LM193		LM293, LM393		LM2903		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Input Offset Voltage	$T_A = 25^\circ\text{C}$, (Note 9)	± 1.0	± 2.0	± 1.0	± 2.0	± 1.0	± 5.0	± 1.0	± 5.0	± 2.0	± 7.0	mVDC
Input Bias Current	I_{IN+} or I_{IN-} with Output in Linear Range, $T_A = 25^\circ\text{C}$, (Note 5)	25	100	25	250	25	100	25	250	25	250	nADC
Input Offset Current	$I_{IN+} - I_{IN-}$, $T_A = 25^\circ\text{C}$	± 3.0	± 25	± 5.0	± 50	± 3.0	± 25	± 5.0	± 50	± 5.0	± 50	nADC
Input Common Mode Voltage Range	$T_A = 25^\circ\text{C}$, (Note 6)	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	VDC
Supply Current	$R_L = \infty$ on All Comparators, $T_A = 25^\circ\text{C}$ $R_L = \infty$ on All Amps, $V^+ = 30\text{ VDC}$ $R_L \geq 15\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, $V^+ = 15\text{ VDC}$ (To Support Large VO Swing)	0.4 1 2.5	1 2.5	0.4 1 2.5	1 2.5	0.4 1 2.5	1 2.5	0.4 1 2.5	1 2.5	0.4 1 2.5	1.0 2.5	mADC mADC mADC
Voltage Gain		50	200	50	200	50	200	50	200	25	100	V/mV
Large Signal Response Time	$V_{IN} = \text{TTL Logic Swing}$, $V_{REF} = 1.4\text{ VDC}$ $V_{RL} = 5\text{ VDC}$, $R_L = 5.1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ $V_{RL} = 5\text{ VDC}$, $R_L = 5.1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ (Note 7)	300		300		300		300		300		ns
Response Time		1.3		1.3		1.3		1.3		1.5		μs
Output Sink Current	$V_{IN} \geq 1\text{ VDC}$, $V_{IN+} = 0$, $V_O \leq 1.5\text{ VDC}$ $T_A = 25^\circ\text{C}$	6.0	16	6.0	16	6.0	16	6.0	16	6	16	mAOC
Saturation Voltage	$V_{IN} \geq 1\text{ VDC}$, $V_{IN+} = 0$, $I_{SINK} \leq 4\text{ mA}$, $T_A = 25^\circ\text{C}$	250	400	250	400	250	400	250	400			mVDC
Output Leakage Current	$V_{IN} = 0$, $V_{IN+} \geq 1\text{ VDC}$, $V_O = 5\text{ VDC}$, $T_A = 25^\circ\text{C}$	0.1		0.1		0.1		0.1		0.1		nADC

Electrical Characteristics ($V^+ = 5\text{ V}_{\text{DC}}$) (Note 4)

Supply Voltage, V*	36 VDC or ±18 VDC
Differential Input Voltage	36 VDC
Input Voltage	-0.3 VDC to +36 VDC
Power Dissipation (Note 1)	
Molded DIP	570 mW
Metal Can	630 mW
Output Short Circuit to Ground, (Note 2)	Continuous
Input Current (VIN < -0.3 VDC), (Note 3)	50 nA
Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	-25°C to +75°C
LM193/LM193A	-55°C to +125°C
LM2903	-40°C to +85°C
	-65°C to +150°C
Storage Temperature Range	300°C
Lead Temperature (Soldering, 10 seconds)	

Absolute Maximum Ratings

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM193A				LM293, LM393				UNITS
		MIN	TYP	MAX		MIN	TYP	MAX		
Input Offset Voltage	(Note 9)			4.0				9		mVDC
Input Offset Current	$I_{IN+} - I_{IN-}$			± 100				± 150		nADC
Input Bias Current	I_{IN+} or I_{IN-} with Output in Linear Range			300				400		nADC
Input Common-Mode Voltage Range				0				0		VDC
Saturation Voltage	$V_{IN} \geq 1$ VDC; $V_{IN+} = 0$; $I_{SINK} \leq 4$ mA;			700				700		mVDC
Output Leakage Current	$V_{IN-} = 0$; $V_{IN+} \geq 1$ VDC; $V_O = 30$ VDC;			1.0				1.0		μ ADC
Differential Input Voltage	Keep All V_{IN+} 's ≥ 0 VDC for V_{-} , if Used.			36				36		VDC
	(Note 8)									

Note 1: For operating at high temperatures, the LM193/LM393A and LM293 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM393A/LM293 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON/OFF" characteristic of the outputs keeps the chip dissipation very small (PD ≤ 100 mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+ .

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 VDC.

Note 4: These specifications apply for $V^+ = 5$ VDC and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise stated. With the LM293/LM393A all temperature specifications are limited to $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ and the LM393/LM393A temperature specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$. The LM2903 is limited to $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

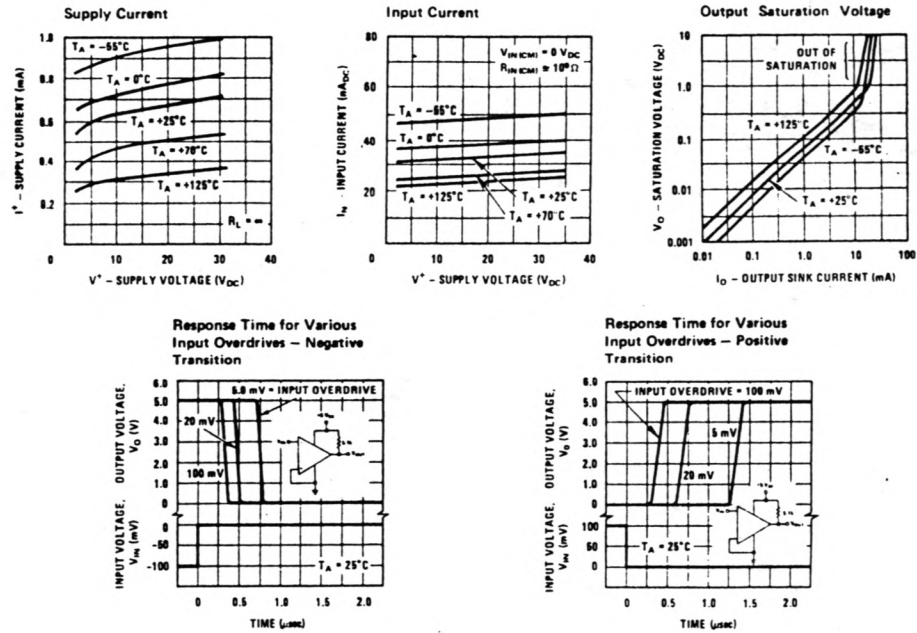
Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than $0.3V$. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to 30 VDC without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained; see typical performance characteristics section.

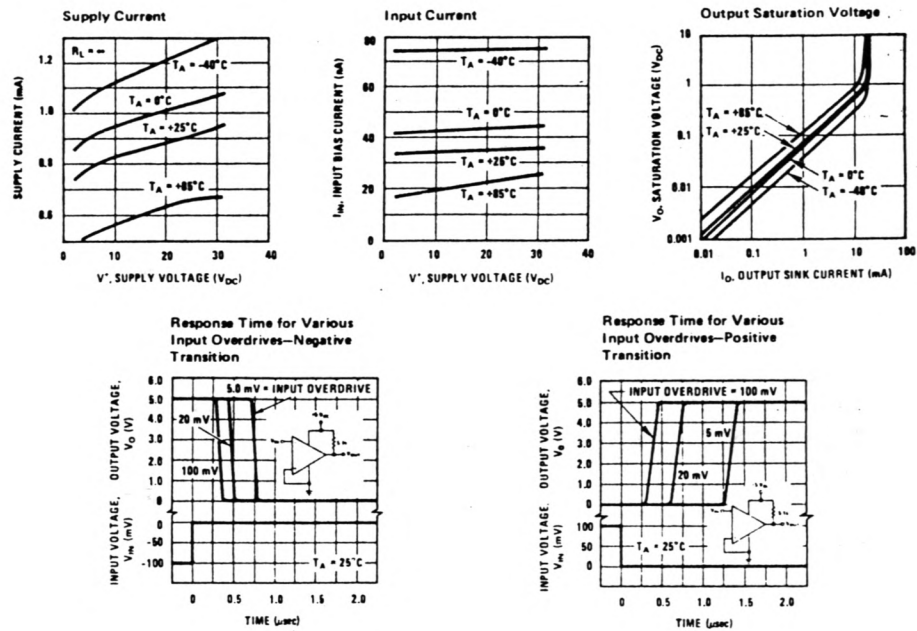
Note 8: Positive excursion of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 VDC for 0.3 VDC below the magnitude of the negative power supply, if used.

Note 9: At output switch point, $V_O \pm 1.4$ VDC, $R_S = 0\Omega$; with V^+ from 5 VDC to 30 VDC; and over the full input common-mode range (0 VDC to $V^+ - 1.5$ VDC).

Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A



Typical Performance Characteristics LM2903





DI CMOS Protected Analog Switches

AD7510DI/AD7511DI/AD7512DI

FEATURES

Latch-Proof
Overvoltage-Proof: $\pm 25V$
Low R_{ON} : 75Ω
Low Dissipation: $3mW$
TTL/CMOS Direct Interface
Monolithic Dielectrically Isolated CMOS
Standard 14/16-pin DIPs and 20-Terminal
Surface Mount Packages

GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch-proof dielectrically isolated CMOS switches featuring overvoltage protection up to $\pm 25V$ above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current ($500pA$), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in either a 16-pin DIP or a 20-terminal surface mount package. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged in either a 14-pin DIP or a 20-terminal surface mount package.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

ORDERING INFORMATION¹

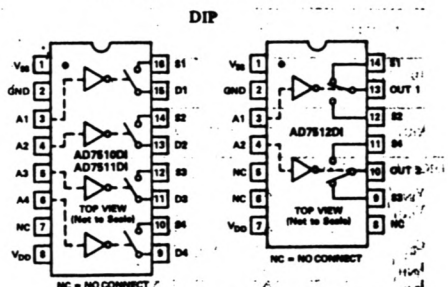
Temperature Range and Package		
0 to +70°C	-25°C to +85°C	-55°C to +125°C
Plastic DIP	Hermetic	Hermetic
AD7510DIJN	AD7510DIJQ	AD7510DISQ
AD7510DIKN	AD7510DIKQ	AD7510DITQ
AD7511DIJN	AD7511DIJQ	AD7511DITQ
AD7511DIKN	AD7511DIKQ	AD7512DISQ
AD7512DIJN	AD7512DIJQ	AD7512DITQ
AD7512DIKN	AD7512DIKQ	
PLCC ²		LCCC ³
AD7510DIJP		AD7510DISE
AD7510DIKP		AD7511DISE
AD7511DIJP		AD7511DITE
AD7511DIKP		AD7512DISE
AD7512DIJP		AD7512DITE
AD7512DIKP		

NOTES

¹To order MIL-STD-883, Class B processed parts, add/883B to part number. See Analog Devices' 1987 Military Product Databook military data sheet.

²PLCC: Plastic Leaded Chip Carrier.
³LCCC: Leadless Ceramic Chip Carrier.

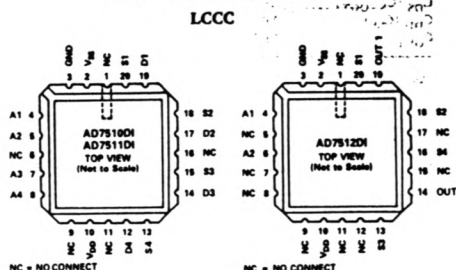
AD7510DI/AD7511DI/AD7512DI FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATIONS



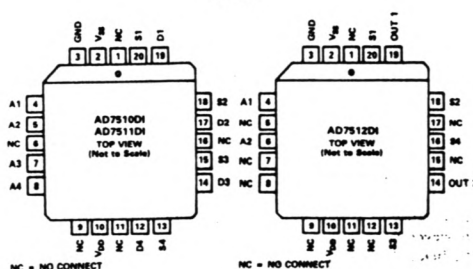
CONTROL LOGIC

AD7510DI: Switch "ON" for Address "HIGH"
AD7511DI: Switch "ON" for Address "LOW"
AD7512DI: Address "HIGH" makes S1 to Out 1 and S2 to Out 2

PIN CONFIGURATIONS



PLCC



SPECIFICATIONS ($V_{DD} = +15V$, $V_{SS} = -15V$ unless otherwise noted)

COMMERCIAL AND INDUSTRIAL VERSIONS (J, K)

PARAMETER	MODEL	VERSION	+25°C (N, P, Q, E)	0 to +70°C (N, P) -25°C to +85°C (Q)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON} ¹	All	J, K	75 Ω typ, 100 Ω max	175 Ω max	$-10V \leq V_D \leq +10V$ $I_{DS} = 1.0mA$
R_{ON} vs V_D (V_S)	All	J, K	20% typ		
R_{ON} Drift	All	J, K	+0.5%/°C typ		$V_D = 0$, $I_{DS} = 1.0mA$
R_{ON} Match	All	J, K	1% typ		
R_{ON} Drift Match	All	J, K	0.01%/°C typ		
I_D (I_S) OFF ¹	All	J, K	0.5nA typ, 5nA max	500nA max	$V_D = -10V$, $V_S = +10V$ and $V_D = +10V$, $V_S = -10V$
I_D (I_S) ON ¹	All	J, K	10nA max		$V_S = V_D = +10V$ $V_S = V_D = -10V$
I_{OUT} ¹	AD7512DI	J, K	15nA max	1500nA max	$V_{S1} = V_{OUT} = \pm 10V$, $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$, $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL} ¹	All	J, K		0.8V max	
V_{INH} ¹	All	J		3.0V min	
V_{INL} ¹	All	K		2.4V min	
C_{IN}	All	J, K	7pF typ		
I_{INH} ¹	All	J, K	10nA max		$V_{IN} = V_{DD}$ $V_{IN} = 0$
I_{INL} ¹	All	J, K	10nA max		
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	J, K	180ns typ		$V_{IN} = 0$ to $+3.0V$
	AD7511DI	J, K	350ns typ		
t_{OFF}	AD7510DI	J, K	350ns typ		
	AD7511DI	J, K	180ns typ		
$t_{TRANSITION}$	AD7512DI	J, K	300ns typ		
C_S (C_D) OFF	All	J, K	8pF typ		V_D (V_S) = 0V
C_S (C_D) ON	All	J, K	17pF typ		
C_{DS} (C_S -OUT)	All	J, K	1pF typ		
C_{DD} (C_{SS})	All	J, K	0.5pF typ		
C_{OUT}	AD7512DI	J, K	17pF typ		
Q_{INJ}	All	J, K	30pC typ		Measured at S or D terminal, $V_{IN} = 0$ to $3V$, $C_L = 1000pF$, $V_{DD} = 0$ to $3V$, V_D (V_S) = $+10V$ to $-10V$
POWER SUPPLY					
I_{DQ} ¹	All	J, K	800 μA max	800 μA max	All digital inputs = V_{INH}
I_{SS} ¹	All	J, K	800 μA max	800 μA max	
I_{DQ} ¹	All	J, K	500 μA max	500 μA max	All digital inputs = V_{INL}
I_{SS} ¹	All	J, K	500 μA max	500 μA max	
PACKAGE OPTIONS²					
Plastic (N-14)	AD7512DIJN/KN				
Plastic (N-16)	AD7510DIJN/KN				
	AD7511DIJN/KN				
Cerdip (Q-14)	AD7512DIJQ/KQ				
Cerdip (Q-16)	AD7510DIJQ/KQ				
	AD7511DIJQ/KQ				
PLCC (P-20A)	AD7510DIJP/KP				
	AD7511DIJP/KP				
	AD7512DIJP/KP				

NOTES

¹100% tested.

²See Section 13 for package outline information.

Specifications subject to change without notice.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

WARNING!



EXTENDED VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}^1	All	S, T	100Ω max	175Ω max	-10V < V_D < +10V $I_{DS} = 1mA$
$I_D (I_S)_{OFF}^1$	All	S, T	3nA max	200nA max	$V_D = -10V, V_S = +10V$ and $V_D = +10V, V_S = -10V$
$I_D (I_S)_{ON}^1$	All	S, T	10		$V_S = V_D = +10V$ and $V_S = V_D = -10V$
I_{OUT}^1	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = +10V$ $V_{S2} = V_{OUT} = -10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL}^1	All	S, T		0.8V max	
$V_{INH}^{1,2}$	AD7510DI	S		2.4V min	
	AD7511DI	T		2.4V min	
	AD7512DI	T		2.4V min	
	AD7511DI	S		3.0V min	
	AD7512DI	S		3.0V min	
I_{INH}^1	All	S, T	10nA max		$V_{IN} = V_{DD}$
I_{INL}^1	All	S, T	10nA max		$V_{IN} = 0$
DYNAMIC CHARACTERISTICS					
t_{ON}^3	AD7510DI	S	1.0μs max		$V_{IN} = 0$ to +3V
	AD7511DI	S, T	1.0μs max		
t_{OFF}^3	AD7510DI	S, T	1.0μs max		
	AD7511DI	S, T	1.0μs max		
$t_{TRANSITION}^3$	AD7512DI	S, T	1.0μs max		
POWER SUPPLY					
I_{DD}^1	All	S, T		800μA max	All digital inputs = V_{INH}
I_{SS}^1	All	S, T		800μA max	
I_{DD}^1	All	S, T		500μA max	All digital inputs = V_{INL}
I_{SS}^1	All	S, T		500μA max	
PACKAGE OPTIONS⁴					
Cerdip (Q-14)	AD7510DISQ				
Cerdip (Q-16)	AD7511DISQ/TQ				
	AD7512DISQ/TQ				
LCCC (E-20A)	AD7510DISE				
	AD7511DISE/TE				
	AD7512DISE/TE				

NOTES

- 100% tested.
- A pullup resistor, typically 1-2kΩ is required to make AD7511DISQ and AD7512DISQ TTL compatible.
- Guaranteed, not production tested.
- See Section 13 for package outline information.

Specifications subject to change without notice.

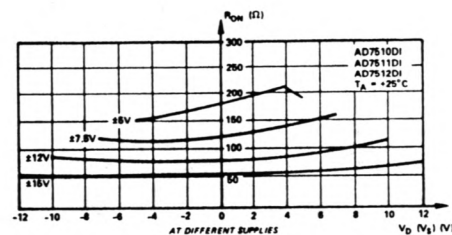
ABSOLUTE MAXIMUM RATINGS⁵

V_{DD} to GND	+17V
V_{SS} to GND	-17V
Overvoltage at $V_D (V_S)$	
(1 second surge)	$V_{DD} + 25V$ or $V_{SS} - 25V$
(Continuous)	$V_{DD} + 20V$ or $V_{SS} - 20V$
Switch Current (I_{DS} , Continuous)	50mA
Switch Current (I_{DS} , Surge)	
1ms Duration, 10% Duty Cycle	150mA
Digital Input Voltage Range	0V to $V_{DD} + 0.3V$
Power Dissipation (Any Package)	

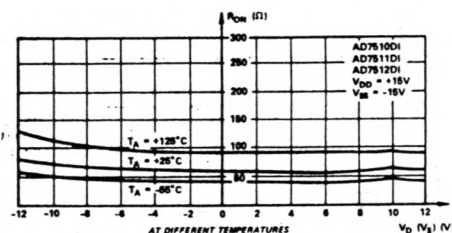
Up to +75°C	450mW
Derates above +75°C by	6mW/°C
Lead Temperature (Soldering, 10sec)	+300°C
Storage Temperature	-65°C to +150°C
Operating Temperature	
Commercial (JN, KN, JP, KP Versions)	0 to +70°C
Industrial (JQ, KQ Versions)	-25°C to +85°C
Extended (SQ, TQ, SE, TE Versions)	-55°C to +125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

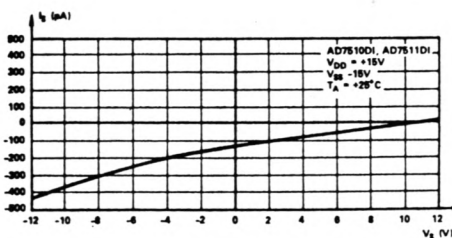
Typical Performance Characteristics



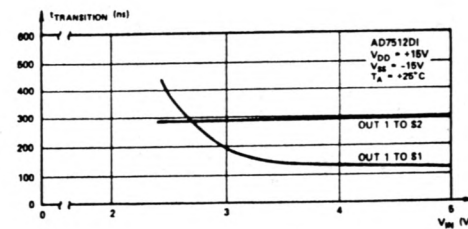
R_{ON} as a Function of $V_D (V_S)$



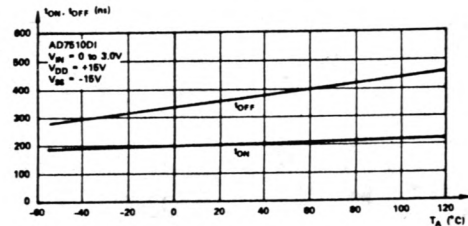
R_{ON} as a Function of $V_D (V_S)$



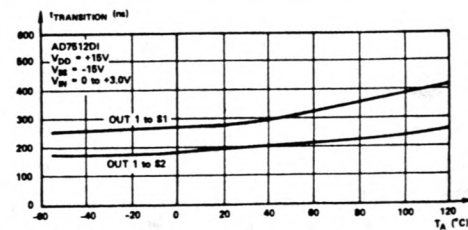
$I_S (I_{DS})_{OFF}$ vs V_S



$t_{TRANSITION}$ as a Function of Digital Input Voltage



t_{ON}, t_{OFF} as a Function of Temperature



$t_{TRANSITION}$ as a Function of Temperature

LM135/LM235/LM335, LM135A/LM235A/LM335A Precision Temperature Sensors

General Description

The LM135 series are precision, easily-calibrated, integrated circuit temperature sensors. Operating as a 2-terminal zener, the LM135 has a breakdown voltage directly proportional to absolute temperature at +10 mV/°K. With less than 1Ω dynamic impedance the device operates over a current range of 400 μA to 5 mA with virtually no change in performance. When calibrated at 25°C the LM135 has typically less than 1°C error over a 100°C temperature range. Unlike other sensors the LM135 has a linear output.

Applications for the LM135 include almost any type of temperature sensing over a -55°C to +150°C temperature range. The low impedance and linear output make interfacing to readout or control circuitry especially easy.

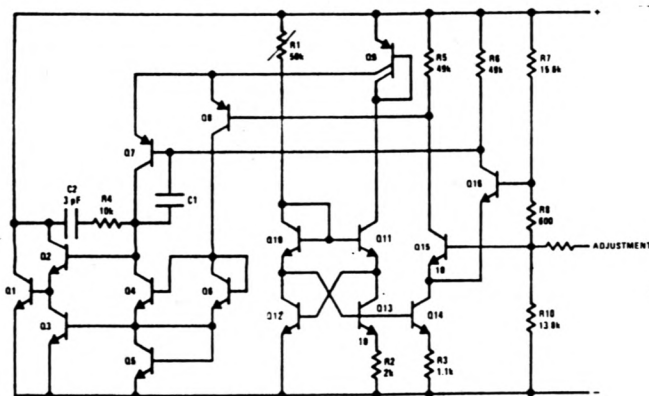
The LM135 operates over a -55°C to +150°C temperature range while the LM235 operates over a -40°C

to +125°C temperature range. The LM335 operates from -40°C to +100°C. The LM135/LM235/LM335 are available packaged in hermetic TO-46 transistor packages while the LM335 is also available in plastic TO-92 packages.

Features

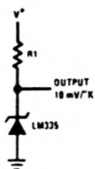
- Directly calibrated in °Kelvin
- 1°C initial accuracy available
- Operates from 400 μA to 5 mA
- Less than 1Ω dynamic impedance
- Easily calibrated
- Wide operating temperature range
- 200°C overrange
- Low cost

Schematic Diagram

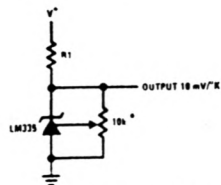


Typical Applications

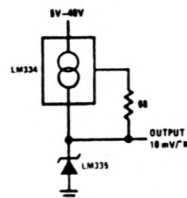
Basic Temperature Sensor



Calibrated Sensor



Wide Operating Supply



* Calibrate for 2.982V at 25°C

Absolute Maximum Ratings

Reverse Current	15 mA
Forward Current	10 mA
Storage Temperature	
TO-46 Package	-60°C to +180°C
TO-92 Package	-60°C to +150°C

Specified Operating Temperature Range

	Continuous	Intermittent (Note 2)
LM135, LM135A	-55°C to +150°C	150°C to 200°C
LM235, LM235A	-40°C to +125°C	125°C to 150°C
LM335, LM335A	-40°C to +100°C	100°C to 125°C
Lead Temperature (Soldering, 10 seconds)		300°C

Temperature Accuracy LM135/LM235, LM135A/LM235A (Note 1)

PARAMETER	CONDITIONS	LM135A/LM235A			LM135/LM235			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage	$T_C = 25^\circ\text{C}$, $I_R = 1\text{ mA}$	2.97	2.98	2.99	2.95	2.98	3.01	V
Uncalibrated Temperature Error	$T_C = 25^\circ\text{C}$, $I_R = 1\text{ mA}$		0.5	1		1	3	°C
Uncalibrated Temperature Error	$T_{\text{MIN}} < T_C < T_{\text{MAX}}$, $I_R = 1\text{ mA}$		1.3	2.7		2	5	°C
Temperature Error with 25°C Calibration	$T_{\text{MIN}} < T_C < T_{\text{MAX}}$, $I_R = 1\text{ mA}$		0.3	1		0.5	1.5	°C
Calibrated Error at Extended Temperatures	$T_C = T_{\text{MAX}}$ (Intermittent)		2			2		°C
Non-Linearity	$I_R = 1\text{ mA}$		0.3	0.5		0.3	1	°C

Temperature Accuracy LM335, LM335A (Note 1)

PARAMETER	CONDITIONS	LM335A			LM335			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage	$T_C = 25^\circ\text{C}$, $I_R = 1\text{ mA}$	2.95	2.98	3.01	2.92	2.98	3.04	V
Uncalibrated Temperature Error	$T_C = 25^\circ\text{C}$, $I_R = 1\text{ mA}$		1	3		2	6	°C
Uncalibrated Temperature Error	$T_{\text{MIN}} < T_C < T_{\text{MAX}}$, $I_R = 1\text{ mA}$		2	5		4	9	°C
Temperature Error with 25°C Calibration	$T_{\text{MIN}} < T_C < T_{\text{MAX}}$, $I_R = 1\text{ mA}$		0.5	1		1	2	°C
Calibrated Error at Extended Temperatures	$T_C = T_{\text{MAX}}$ (Intermittent)		2			2		°C
Non-Linearity	$I_R = 1\text{ mA}$		0.3	1.5		0.3	1.5	°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM135/LM235 LM135A/LM235A			LM335 LM335A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage	$400\text{ }\mu\text{A} < I_R < 5\text{ mA}$		2.5	10		3	14	mV
Change with Current	At Constant Temperature							
Dynamic Impedance	$I_R = 1\text{ mA}$		0.5			0.6		Ω
Output Voltage Temperature Drift			+10			+10		mV/°C
Time Constant	Still Air		80			80		sec
	100 ft/Min Air		10			10		sec
	Stirred Oil		1			1		sec
Time Stability	$T_C = 125^\circ\text{C}$		0.2			0.2		°C/khr

Note 1: Accuracy measurements are made in a well-stirred oil bath. For other conditions, self heating must be considered.

Note 2: Continuous operation at these temperatures for 10,000 hours for H package and 5,000 hours for Z package may decrease life expectancy of the device.



Precision Monolithics Inc.

OP-10

DUAL MATCHED INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- Extremely Tight Matching
- Excellent Individual Amplifier Parameters
- Offset Voltage Match 0.18mV Max
- Offset Voltage Match vs Temp. 0.8μV/°C Max
- Common-Mode Rejection Match 114dB Min
- Power Supply Rejection Match 100dB Min
- Bias Current Match 3.0nA Max
- Low Noise 0.6μV_{p-p} Max
- Low Bias Current 3.0nA Max
- High Common-Mode Input Impedance 200GΩ Typ
- Excellent Channel Separation 126dB Min

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
0.5	OP10AY*	MIL
0.5	OP10EY	COM
0.5	OP10Y*	MIL
0.5	OP10CY	COM

- For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
- Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

GENERAL DESCRIPTION

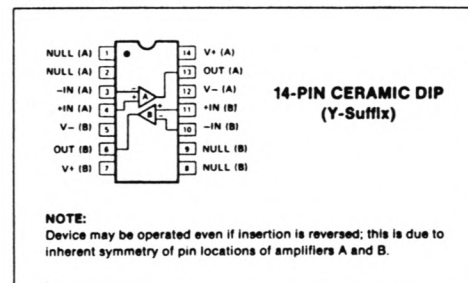
The OP-10 series of dual-matched instrumentation operational amplifiers consists of two independent monolithic high-performance operational amplifiers in a single 14-pin dual-in-line package. Tight matching of critical parameters

is provided between channels of the dual operational amplifier.

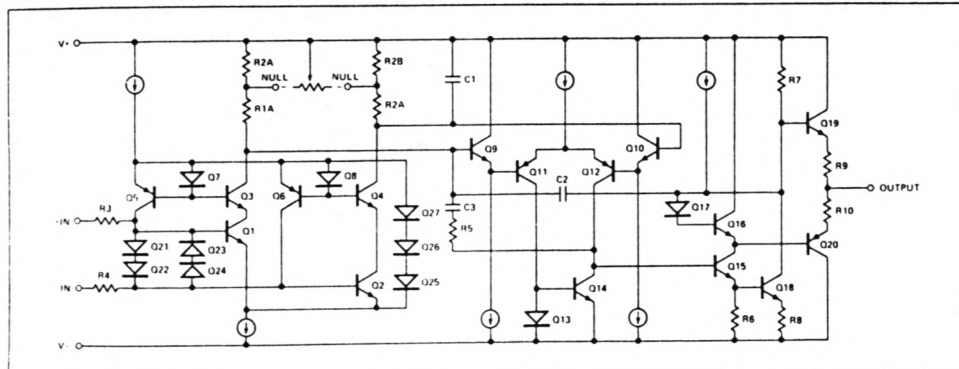
The excellent specifications of the individual amplifiers and tight matching over temperature enable construction of high-performance instrumentation amplifiers. The designer can achieve the guaranteed specifications because the common package eliminates temperature differentials which occur in designs using separately housed amplifiers.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode and power-supply rejection ratios. The individual amplifiers feature extremely low offset voltage, offset voltage drift, low noise voltage, low bias current, internal compensation and input/output protection.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/2 OP-10)



3.0 RELEVANT NRAO DRAWINGS

Title:	Number:	Notes:
43 GHz FE Block Diagram	C53213K002	
System Block Diagram	C53213K001	Page 2*
Front-End Assembly	D53213A001-1	Page 10*
Front-End BOM	A53213B001	Page 44*
Card Cage Assembly	D53206A005	
Card Cage BOM	A53213B007	Appendix page II-10*
Card Cage Wire List	A53213W001	Appendix page II-20*
RF Plate Assembly	No drawing	
RF Card BOM	A53213B005	Appendix page II-8*
Sensor Card Schematic	D53200S002	
Sensor Card Assembly	D53200A003	
Sensor Card BOM		No BOM, parts are on the assembly drawing.
Control Card Schematic	D53200S002	
Control Card Assembly	D53200A004	
Control Card BOM	A53200B004	
Monitor Card Schematic	C53200S005	
Monitor Card Assembly	D53200A006	
Monitor Card BOM	A53200B006	
FET Bias Card Schematic	D53200S001	
FET Bias Card Assembly	D53200S002	
FET Bias Card BOM	A53200B002	

* In TR 11.

4.0 COMPONENT DATA SHEETS

Data sheets for:

Lake Shore Cryotronics DT-500
Hastings DV-6R
Hastings DB-20
Texas Instruments TL084
Texmate PM-45XU
Analog Devices AD581JH
National Semiconductor LM339N
Texas Instruments 75452
Teledyne 643-1
Teledyne 645-2
National Semiconductor LM393AN
Analog Devices AD7512DIKN
National Semiconductor LM335Z
Precision Monolithics OP-10CY

5.0 APPENDIX

List of Relevant NRAO Technical Reports and Technical Memoranda.

VLBA Technical Report No. 1, Low-Noise, 8.4 GHz Cryogenic GASFET Front-End, S. Weinreb, H. Dill and R. Harris, August 29, 1984.

Electronics Division Internal Report No. 204, Temperature Readout Unit for Lake Shore Cryotronics Silicon Diode Sensors (DT-500 Series), Michael Balister, May 1980.

Calibration of the vacuum sensors on VLBA and JPL Front-Ends, Harry Dill, Jan 26, 1987. (This memorandum follows this list.)

VLA Technical Report No. 68, FRONT-END CONTROL MODULE, Module Type F14, David Weber, 5/15/92.

VLBA Technical Report No. 22, FRONT-END CONTROL MODULE, Module Type F117, Paul Lilie, Larry May, and David Weber, January 1993.

Post-It™ brand fax transmittal memo 7671		# of pages > 3
To: <i>Gerry Petencin</i>	From: <i>S. Grayson</i>	
Co:	Co:	
Dept:	Phone #	
Fax #	Fax #	

NATIONAL RADIO ASTRONOMY
Socorro, New Mexico

January 26, 1987

TO: VLBA Front End Maintenance Personnel

FROM: Harry Dill

SUBJECT: Calibration of the vacuum sensors on VLBA and JPL front ends.

TOOLS REQD: Small flat bladed screw driver.

The vacuum sensor circuits in the field have a tendency to drift upward over time. The cause of this is possibly contamination of the thermocouple. The extent of this problem needs to be determined, and can be done by keeping accurate field repair records.

Two circuits exist for sensing vacuum. Vd-dewar vacuum and Vp-pump vacuum. These circuits are on the sensor card, which is the second from the top in the card cage. Each circuit has two potentiometers for setting a zero point and an atmosphere point. These two set points are coupled together so that changing one, will alter the other slightly.

Outlined here is a procedure for calibration of the vacuum sensors in the field. If these do not work, then the unit should be returned to maintenance. When ever this field calibration is performed a proper maintenance report form should be filed. This is the only way that data on this problem can be accumulated.

PROCEDURE.

- 1) The Vp and Vd thermocouple gauges on the front end will be used as the reference points for ATM and ZERO. For this to work the front end must be cold, $T_{15} < 25K$.
- 2) Note the readings of Vd, Vp, T15, T50, T300 from the readout panel and record them on the maintenance sheet.
- 3) To ensure that the solenoid or the refrigerator will not be disturbed during the calibration process, the AC power plug, connected to J-1, should be connected directly to the refrigerator power receptacle. This removes power to the solenoid, and bypasses the control card for powering the refrigerator.

- 4) Disconnect the vacuum hose from the front end and seal it off at the pump end such that other front ends can use the pump if required. (During the calibration the pump will turn on an off depending the Vd reading.)
- 5) Remove the cover to the card cage (two thumb screws located on either side of the readout panel) and locate the sensor card (second from the top). Then locate four trimpots labeled D ZERO, D ATM, P ZERO and P ATM. Do not turn any other trimpots as they may effect the calibration of the receiver.
- 6) With the Vx, Vx is either Vd or Vp depending upon which circuit is being calibrated, plug connected to the Vp thermocouple the reading for Vx should be 10.0. Turning the multiturn trimpot X ATM; again, X is either P or D, should bring the readout to 10.0 if required. Note that the readout takes several seconds to stabilize after turning the trimpot, so turn it slowly.
- 7) Connect the Vx plug to the Vd thermocouple. The reading for Vx should be 0.0. Adjust X ZERO to bring this reading to 0.0 +/- .005.
- 8) Recheck the ATM reading and ZERO reading by repeating steps 6 and 7.
- 9) Reconnect the vacuum line. reconnect plugs Vp and Vd properly. Replace the card cage cover and reconnect the AC power to J-1 and the refrigerator AC power to itself.

NOTES

a) A reading of Vd >.420 will activate a pump request. This will be activated at all times unless the front end is commanded to the OFF mode. If the front end is issuing a pump request and is cold and running properly then this indicates that the vacuum sensor has drifted upward.

