VLBA Technical Report No. 44
THE VLBA CORRELATOR
FFT CONTROL CARD (FCC)
AND
FFT CARD MANUAL
VOLUME 2 of 2

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FFT CONTROL CARD (FCC)
AND
FFT CARD MANUAL
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Ray Escoffier

July 21, 1998

fftmanv2.doc Microsoft Word not under SCCS control

Master file stored in /corrdwgs/manuals/fftman/SCCS
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(VOLUME II)

The Orcad plot files can all be plotted using the script:
/corrdwgs/manuals/fftman/plotfft which is under SCCS control.

This file can be printed without the place holders by telling the print section to print pages 1,2,3,4,29,57,67,70 .

2 FCC Schematics, Layouts, PAL Schematic Representations

FCC Block Diagram /corrdwgs/fcc/sch/k046d01.sch

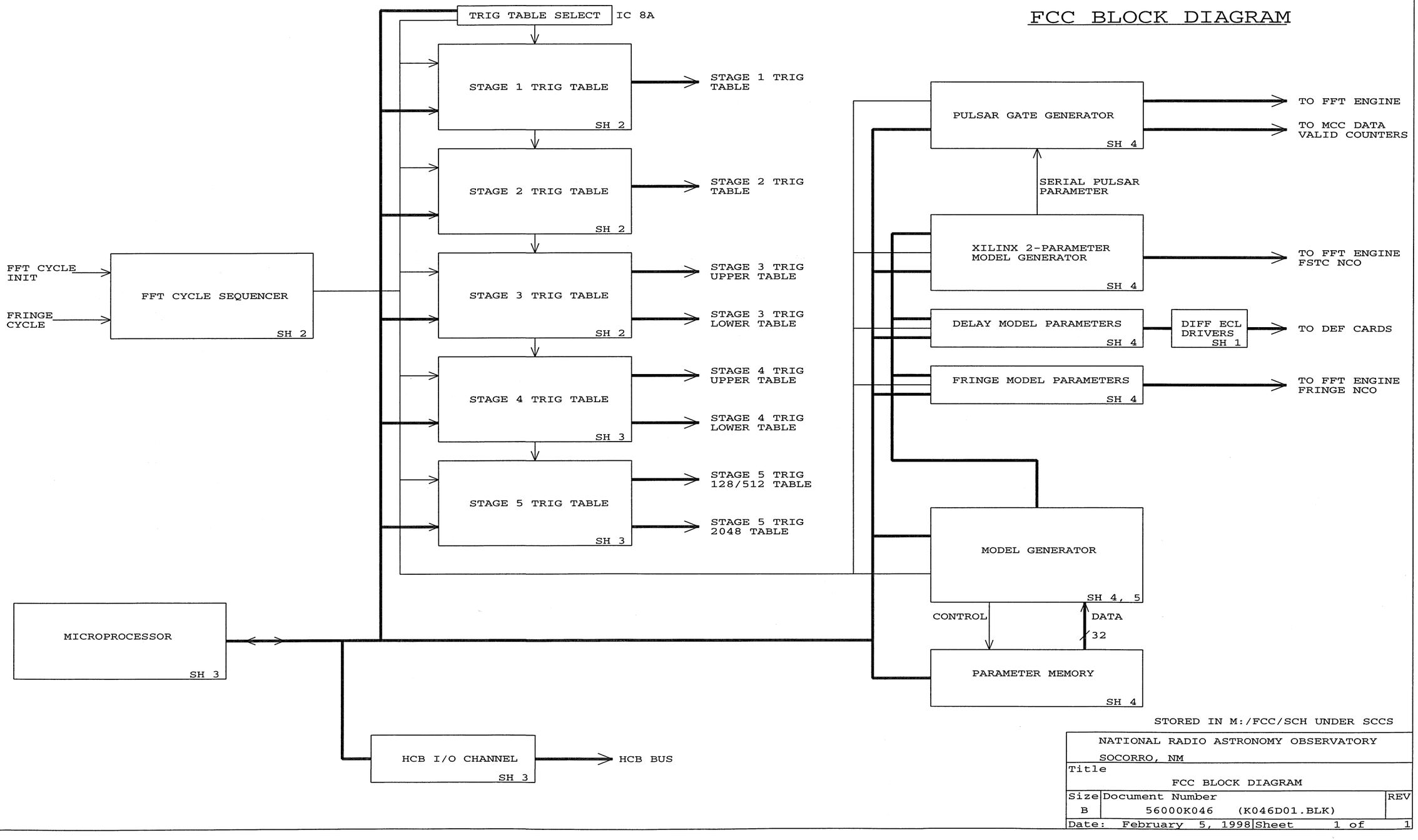
FCC Schematics /corrdwgs/fcc/sch/l013d01.sch through 05

FCC Layout z006d01.lay

FCC PAL Schematic Representations. FCC PALS Sheet 1 through 15

FCC FSTC XILINX DESIGN K027D02.BLK, 03

FCC BLOCK DIAGRAM



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NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NM		
Title: FCC BLOCK DIAGRAM		
Size: B	Document Number: 56000K046 (K046D01.BLK)	REV:
Date: February 5, 1998	Sheet 1 of 1	

LAYOUT

Z006D01.LAY
4 SHEETS ALL SIZE C

FSTC XILINX

K027D01.BLK
13 SHEETS ALL SIZE B

FCC PALS

FCCTOP.PAL
15 SHEETS

FCC BLOCK DIAGRAM

K046D01.BLK
1 SHEET B SIZE

L013D05.SCH, THE FLOATING POINT CHIP, IS WITHIN SHEET 4.

L0013D02.SCH

L013D03.SCH

L013D04.SCH

L013D02.SCH

L013D03.SCH

L013D04.SCH

P1A

P1B

P1C

P2A

P2B

P2C

P3A

P3B

P3C

J1

J2

3M50

RSC9X471J

* SPARE

REVISION	DATE	DESCRIPTION
REV A	2/20/90	CHANGE ADDR TEXT ON SH. 3 CHANGE S20 FUNCTION TABLE ON SH. 4 ADD S5 TABLE AND FIFO CHART ON SH. 4 CHANGE 34H TO 16R4 AND 6C TO 16L8. ADD T0 TO T7 TABLE TO SH. 1, CHG 8A TO 22V10 ADD SEL15 TO 26P ON SH. 3 CHANGE TRIG TABLE LABLES, ADD PIN NUMBERS
REV B	4/29/91	CHANGE 7F AND 7E TO 16V8A ON SH. 4 PUT FF70 INTO 7F AND 7E ON SH. 4 CORRECT MINOR ERRORS ON SH. 4 ADD SCOPE SYNC LABEL ON SH. 3 CHANGE FFT CARD CONTROL WORD SHIFT OUT CHANGE 1B TO 22V10 ON SH. 4 CHANGE S29 TO S12 ON SH. 4 PUT RAM PART NO. IN ADD NEW IC 7A, DEL SIX PINS FROM VEE
REV C	7/06/92	ADD INTEG_CYC
REV D	2/24/93	ADD NET - uP RESET\ FROM P3A TO 21E ADD RESISTOR R17 SHEETS AFFECTED SH1, SH2, & SH3 ADD NET - STG4ADRENA ADD NET - STG5ADRENA MOVED R1, ADDED R17 & R18

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VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

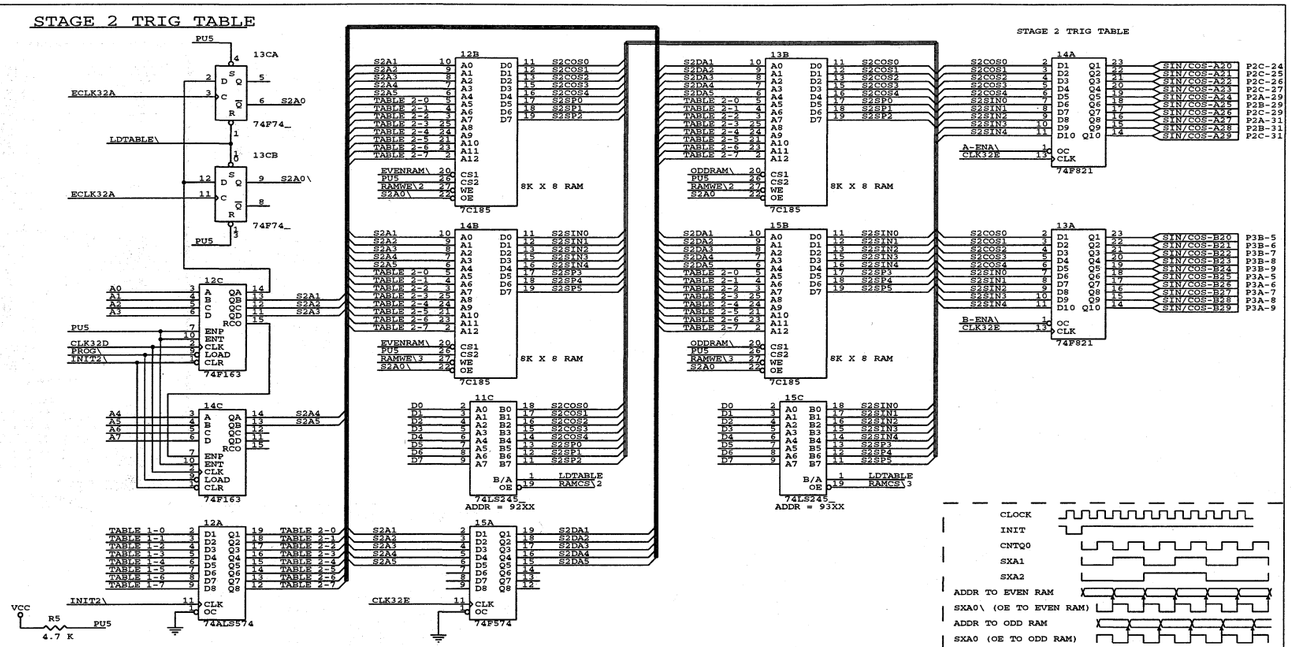
Title

FFT CONTROL CARD

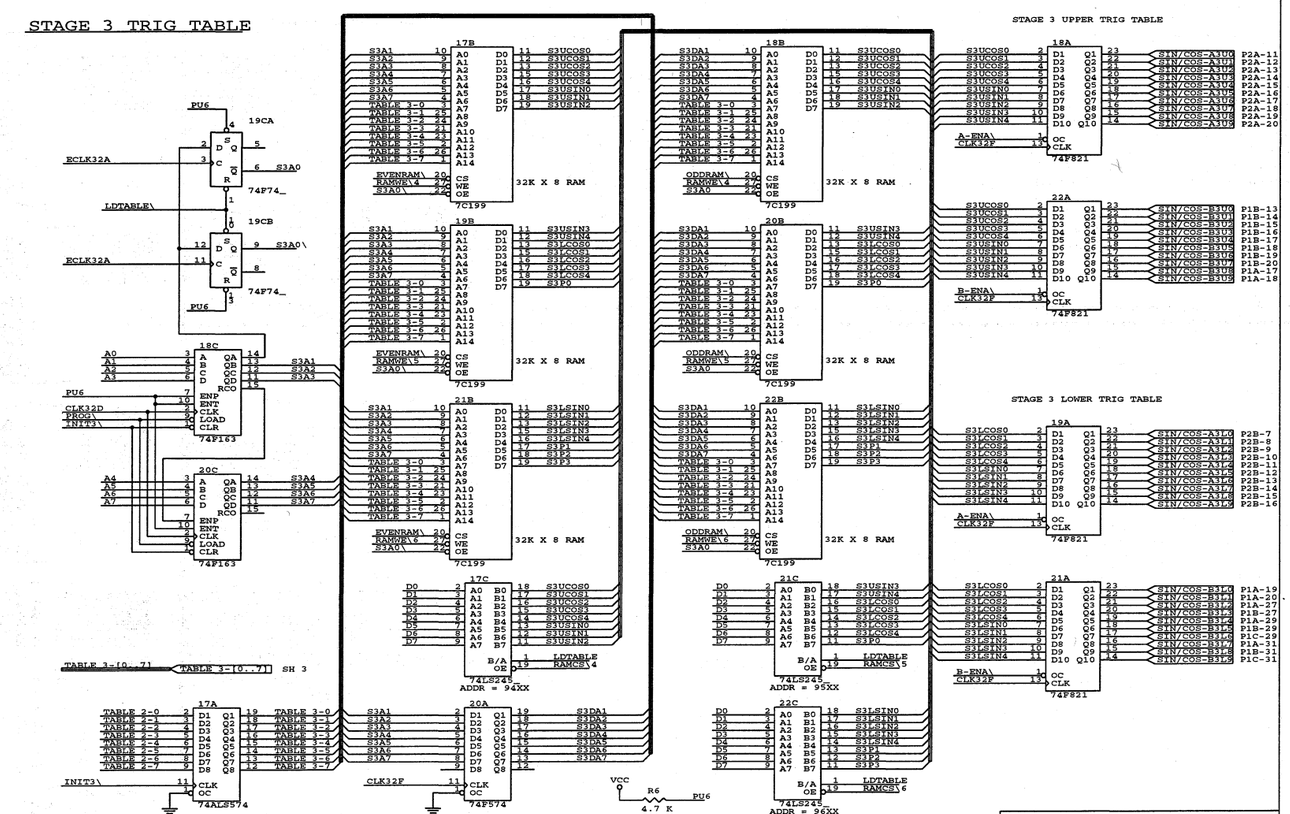
Size	Document Number	REV
D	56000L013 (L013D01.SCH)	D

Date: February 5, 1998 Sheet 1 of 5

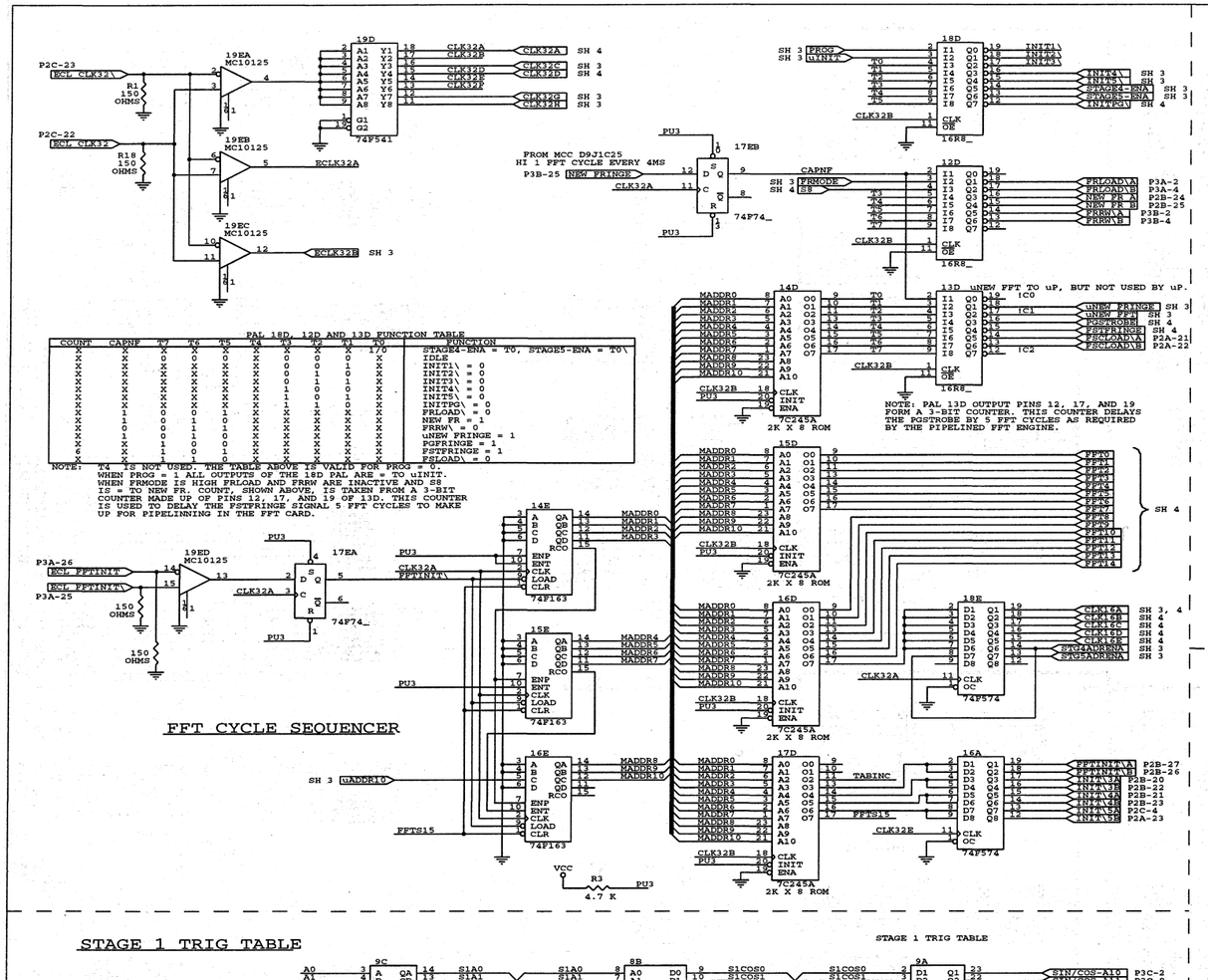
STAGE 2 TRIG TABLE



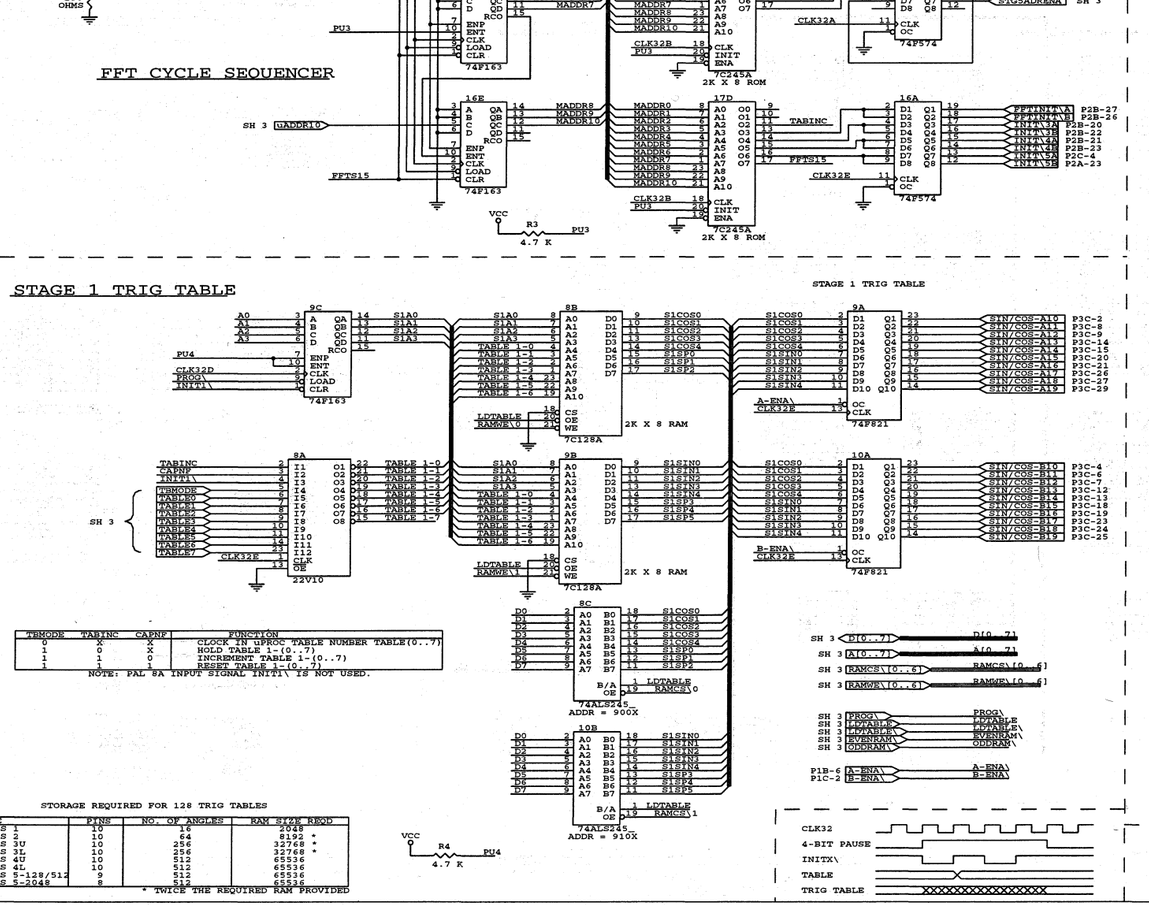
STAGE 3 TRIG TABLE



FFT CYCLE SEQUENCER



STAGE 1 TRIG TABLE



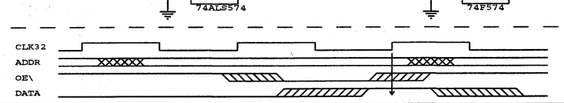
TBMODE	TABINC	CAPNF	FUNCTION
0	X	X	CLOCK IN UPROC TABLE NUMBER TABLE(0..7)
1	0	X	HOLD TABLE 1-(0..7)
1	1	0	INCREMENT TABLE 1-(0..7)
1	1	1	RESET TABLE 1-(0..7)

NOTE: PAL 8A INPUT SIGNAL INIT1\ IS NOT USED.

STORAGE REQUIRED FOR 128 TRIG TABLES

STAGE	PINS	NO. OF ANGLES	RAM SIZE REQD
SIN/COS 1	10	16	2048 *
SIN/COS 2	10	64	8192 *
SIN/COS 3U	10	256	32768 *
SIN/COS 3L	10	256	32768 *
SIN/COS 4U	10	512	65536
SIN/COS 4L	10	512	65536
SIN/COS 5-128/512	9	512	65536
SIN/COS 5-2048	8	512	65536

* TWICE THE REQUIRED RAM PROVIDED



	MIN	MAX
74F74	3.8 nsec	7.8 nsec
74F541	2.5 nsec	6.5 nsec
74F163	3.5 nsec	11.0 nsec
74F574	4.0 nsec	10.0 nsec
RAM OE	10.0 nsec	20.0 nsec

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CHARLOTTESVILLE, VA

Title: FFT CONTROL CARD

Size: D | Document Number: 5600L013 (L013D02.SCH) | REV: D

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STAGE 4 TRIG TABLE

STAGE 4 UPPER TRIG TABLE

STAGE 4 LOWER TRIG TABLE

STAGE 5 TRIG TABLE

128/512 PT TRIG TABLE

STAGE	PINS	NO. OF ANGLES
SIN/COS 1	10	16
SIN/COS 2	10	64
SIN/COS 3U	10	256
SIN/COS 3L	10	256
SIN/COS 4U	10	512
SIN/COS 4L	10	512
SIN/COS 5-128/512	9	512
SIN/COS 5-2048	8	512

2048 PT TRIG TABLE

MICROPROCESSOR

MICRO ADDR	SELECT	FUNCTION
8Y00	SEL0	WRITE TO MISCL PORTS
9YXX	SEL1	R/W TRIG TABLE
A00X	SEL2	R/W MODEL PARAMETER RAM
B000	SEL3	READ HARDWARE CONTROL BUS

ADDR	SELECT	FUNCTION
8000	WR0\	WRITE TRIG TABLE
8100	WR1\	TABLE CONTROL
8200	WR2\	ASIC CONTROL WORD
8300	WR3\	PARAMETER RAM
8400	WR4\	LD RAM CONTROL
8500	WR5\	LD RAM CONTROL
8600	WR6\	
8700	WR7\	HCB COMM
8800	WR8\	WR PARAMETER ADDR
8900	WR9\	MODEL GEN OP CODE
8A00	WR10\	MODEL SELECT
8B00	WR11\	PULSAR GATE ADDR

HCB DATA BUS

HCB0	J1-2
HCB\0	J1-1
HCB1	J1-4
HCB\1	J1-3
HCB2	J1-6
HCB\2	J1-5
HCB3	J1-8
HCB\3	J1-7
HCB4	J1-10
HCB\4	J1-9
HCB5	J1-12
HCB\5	J1-11
HCB6	J1-14
HCB\6	J1-13
HCB7	J1-16
HCB\7	J1-15

SELECT	STROBE	MODE1	MODE0	FUNCTION	ACK	RCVENA\	BUSENA	OEA\	ACKA\	WR\	RESET	IRQ\
0	X	0	0	ALLOW SLAVE TO ASSERT ATT'N	SDATARDY\	1	0	1	1	1	0	1
0	X	0	1	IDLE	1	1	0	1	1	1	0	1
0	X	1	0	IDLE	1	1	0	1	1	1	0	1
0	⊓	0	0	MASTER SENDS IRQ TO SLAVE	1	1	0	1	STROBE\	1	0	STROBE\
0	⊓	1	0	MASTER WRITES TO SLAVE	BUSY\	0	STROBE	STROBE\	STROBE\	1	0	1
1	⊓	0	0	MASTER READS FROM SLAVE	SDATARDY\	1	STROBE	STROBE\	STROBE\	1	0	1
1	⊓	1	1	MASTER RESETS SLAVE	1	1	0	1	STROBE\	1	STROBE	1

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
FFT CONTROL CARD

Size	Document Number	REV
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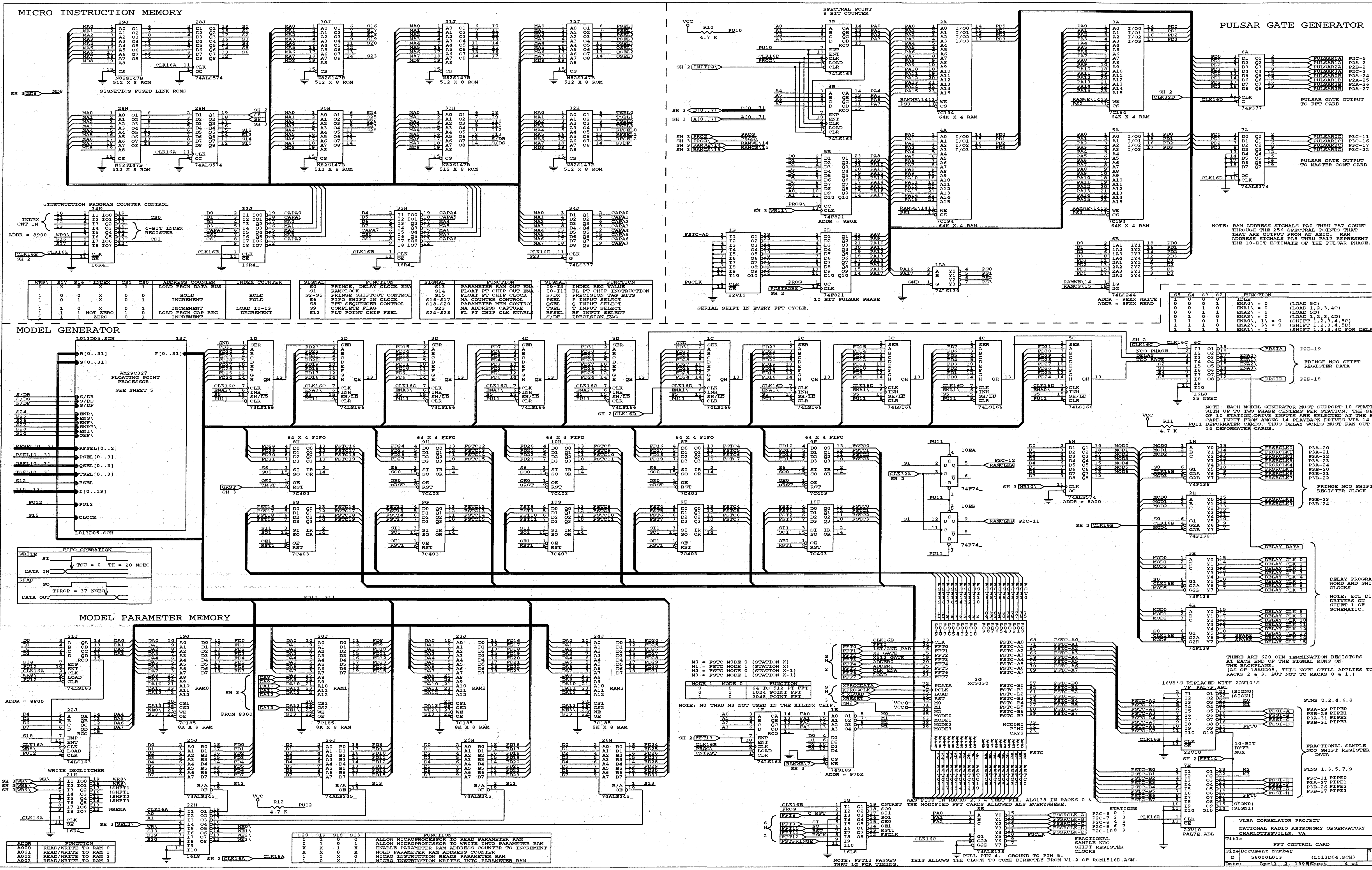
MICRO INSTRUCTION MEMORY
SIGNETICS FUSED LINK ROMS
N82S147B
512 X 8 ROM
74ALS574
µINSTRUCTION PROGRAM COUNTER CONTROL
INDEX CNT IN
4-BIT INDEX REGISTER
ADDR = 8900
16R4_
74LS377
PULSAR GATE GENERATOR
SPECTRAL POINT 8 BIT COUNTER
74LS163
7C194
64K X 4 RAM
74F821
ADDR = 8B0X
22V10
SERIAL SHIFT IN EVERY FFT CYCLE.
10 BIT PULSAR PHASE
74LS139
74LS244
ADDR = 9EXX WRITE
ADDR = 9FXX READ
PULSAR GATE OUTPUT TO FFT CARD
PULSAR GATE OUTPUT TO MASTER CONT CARD
74F377
74ALS374
NOTE: RAM ADDRESS SIGNALS PA0 THRU PA7 COUNT THROUGH THE 256 SPECTRAL POINTS THAT THAT ARE OUTPUT FROM AN ASIC. RAM ADDRESS SIGNALS PA8 THRU PA17 REPRESENT THE 10-BIT ESTIMATE OF THE PULSAR PHASE.
MODEL GENERATOR
L013D05.SCH
AM29C327 FLOATING POINT PROCESSOR
SEE SHEET 5
74LS166
64 X 4 FIFO
7C403
FIFO OPERATION
TSU = 0 TH = 20 NSEC
TPROP = 37 NSEC
FRINGE NCO SHIFT REGISTER DATA
NOTE: EACH MODEL GENERATOR MUST SUPPORT 10 STATIONS WITH UP TO TWO PHASE CENTERS PER STATION. THE SET OF 10 STATION DRIVE INPUTS ARE SELECTED AT THE FFT CARD INPUT FROM AMONG 14 PLAYBACK DRIVES VIA 14 DEFORMATER CARDS. THUS DELAY WORDS MUST FAN OUT TO 14 DEFORMATER CARDS.
74F74_
74ALS574
ADDR = 8A00
FRINGE NCO SHIFT REGISTER CLOCK
74F138
DELAY PROGRAM WORD AND SHIFT CLOCKS
NOTE: ECL DIFF DRIVERS ON SHEET 1 OF SCHEMATIC.
THERE ARE 620 OHM TERMINATION RESISTORS AT EACH END OF THE SIGNAL RUNS ON THE BACKPLANE. (AS OF 18AUG95, THIS NOTE STILL APPLIES TO RACKS 2 & 3, BUT NOT TO RACKS 0 & 1.)
16V8'S REPLACED WITH 22V10'S
3G XC3030
STNS 0,2,4,6,8
FRACTIONAL SAMPLE NCO SHIFT REGISTER DATA
STNS 1,3,5,7,9
10-BIT BYTE MUX
22V10 PAL7E.ABL
MODEL PARAMETER MEMORY
7C185
8K X 8 RAM
FROM 8300
ADDR = 8800
74ALS245_
WRITE DEGLITCHER
16L8
74S189
ADDR = 970X
WAS F138 IN RACKS 2,3 & TEST FIX, ALS138 IN RACKS 0 & 1. THE MODIFIED FFT CARDS ALLOWED ALS EVERYWHERE.
74ALS138
FRACTIONAL SAMPLE NCO SHIFT REGISTER CLOCKS
NOTE: FFT12 PASSES THRU 1G FOR TIMING.
PULL PIN 4. GROUND TO PIN 5. THIS ALLOWS THE CLOCK TO COME DIRECTLY FROM V1.2 OF ROM1516D.ASM.
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NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title FFT CONTROL CARD
Size D Document Number 56000L013 (L013D04.SCH) REV D
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WR9\	S17	S16	INDEX	CS1	CS0	ADDRESS COUNTER	INDEX COUNTER
0	X	X	X	1	1	LOAD FROM DATA BUS	
1	0	0	X	0	0	HOLD	HOLD
1	0	1	X	0	1	INCREMENT	HOLD
1	1	0	X	0	1	INCREMENT	LOAD I0-I3
1	1	1	NOT ZERO	1	0	LOAD FROM CAP REG	DECREMENT
1	1	1	ZERO	0	1	INCREMENT	

SIGNAL	FUNCTION
S0	FRINGE, DELAY CLOCK ENA
S1	RAMCLOCK
S2-S5	FRINGE SHIFTOUT CONTROL
S6	FIFO SHIFT IN CLOCK
S8	FFT SEQUENCER CONTROL
S9	COMPLETE FLAG
S12	FLT POINT CHIP FSEL

SIGNAL	FUNCTION
S13	PARAMETER RAM OUT ENA
S14	FLOAT PT CHIP OUT ENA
S15	FLOAT PT CHIP CLOCK
S16-S17	MA COUNTER CONTROL
S18-S20	PARAMETER MEM CONTROL
S23	MA ADDRESS CAPTURE
S24-S28	FL PT CHIP CLK ENABLS

SIGNAL	FUNCTION
I0-I3	INDEX REG VALUE
I0-I13	FL PT CHIP INSTRUCTION
S/DX	PRECISION TAG BITS
PSEL	P INPUT SELECT
QSEL	Q INPUT SELECT
TSEL	T INPUT SELECT
RFSEL	RF INPUT SELECT
S/DF	PRECISION TAG

S5	S4	S3	S2	FUNCTION	
1	0	0	0	IDLE	
0	0	0	1	ENA0\ = 0	(LOAD 5C)
0	0	1	0	ENA1\ = 0	(LOAD 1,2,3,4C)
0	0	1	1	ENA2\ = 0	(LOAD 5D)
0	1	0	0	ENA3\ = 0	(LOAD 1,2,3,4D)
1	1	0	1	ENA0\, 1\ = 0	(SHIFT 1,2,3,4,5C)
1	1	1	0	ENA2\, 3\ = 0	(SHIFT 1,2,3,4,5D)
1	1	1	1	ENA1\ = 0	(SHIFT 1,2,3,4C FOR DELAY)

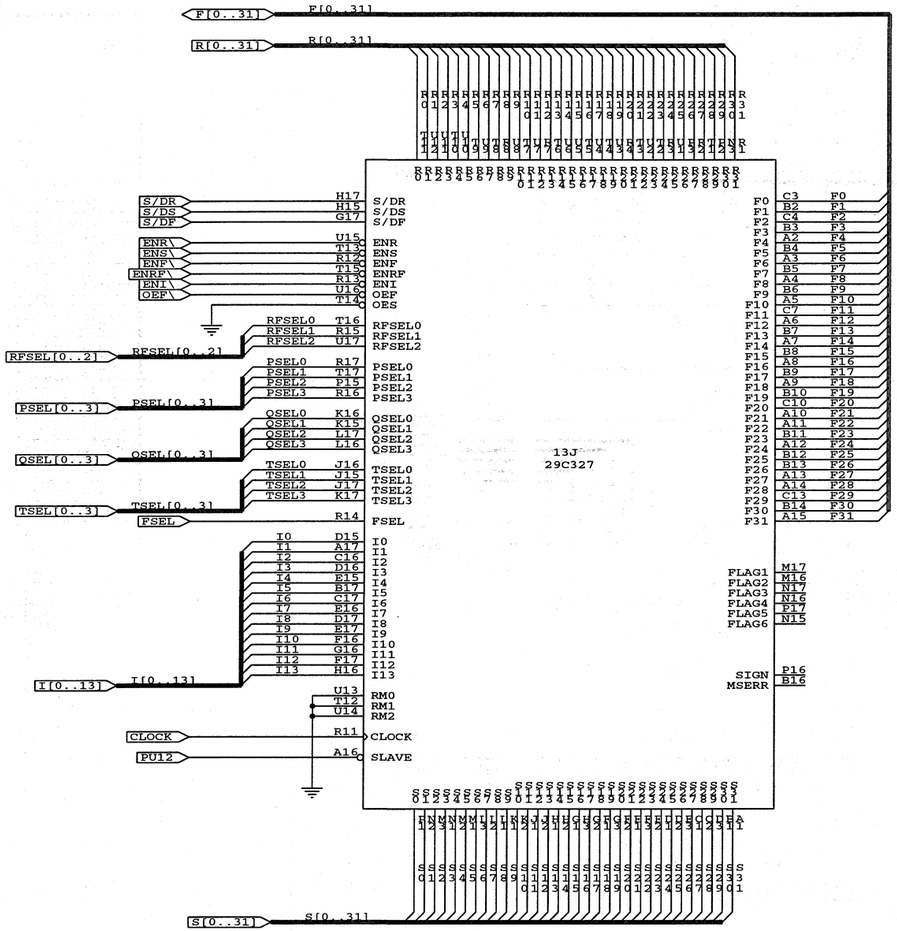
M0 = FSTC MODE 0 (STATION X)
M1 = FSTC MODE 1 (STATION X)
M2 = FSTC MODE 0 (STATION X+1)
M3 = FSTC MODE 1 (STATION X+1)

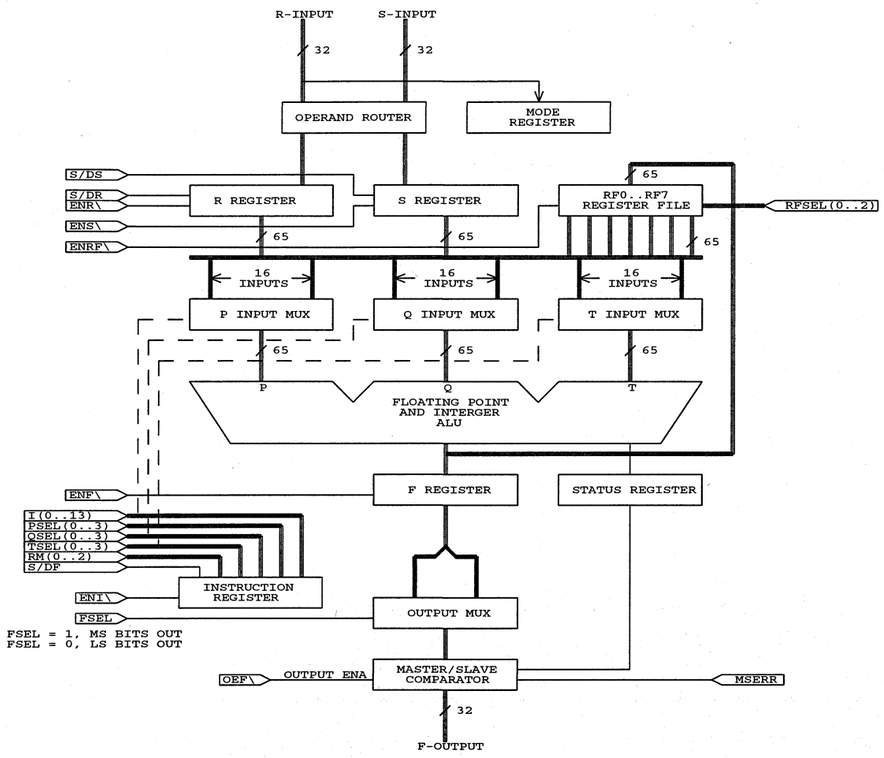
MODE 1	MODE 0	FUNCTION
0	0	64 TO 512 PT FFT
0	1	1024 POINT FFT
1	0	2048 POINT FFT

NOTE: M0 THRU M3 NOT USED IN THE XILINX CHIP.

ADDR	FUNCTION
A000	READ/WRITE TO RAM 0
A001	READ/WRITE TO RAM 1
A002	READ/WRITE TO RAM 2
A003	READ/WRITE TO RAM 3

S20	S19	S18	S13	FUNCTION
0	1	0	0	ALLOW MICROPROCESSOR TO READ PARAMETER RAM
0	1	0	1	ALLOW MICROPROECSSOR TO WRITE INTO PARAMETER RAM
X	X	1	X	ENABLE PARAMETER RAM ADDRESS COUNTER TO INCREMENT
X	X	0	X	HOLD PARAMETER RAM ADDRESS COUNTER
1	1	X	0	MICRO INSTRUCTION READS PARAMETER RAM
1	0	X	1	MICRO INSTRUCTION WRITES INTO PARAMETER RAM





SIX PARAMETER MODEL EQUATION:

CLOCK	INPUT	OP CODE	OPERATION	FUNCTION	STORAGE
0	A5 LS				
1	A5 MS				
0	A4 LS	02			
1	A4 MS	02	P	A5 INTO REGISTER	RF1
0	A3 LS	08			
1	A3 MS	08	(P * Q) + T	(RF1 X T) + A4	RF1
0	A2 LS	08			
1	A2 MS	08	(P * Q) + T	(RF1 X T) + A3	RF1
0	A1 LS	08			
1	A1 MS	08	(P * Q) + T	(RF1 X T) + A2	RF1
0	A0 LS	08			
1	A0 MS	08	(P * Q) + T	(RF1 X T) + A1	RF1
0		08			
1		08	(P * Q) + T	(RF1 X T) + A0	F REG

T (TIME IS STORED IN THE RF0 REGISTER.
REGISTER RF1 IS USED AS THE ACCUMULATOR.
THE INPUT PARAMETERS PING PONG BETWEEN REGISTER R AND S.

I5	I4	I3	I2	I1	I0	HEX	OPERATION (FLOATING POINT)
0	0	0	0	0	0	00	P
0	0	0	0	0	1	01	P + T
0	0	0	0	1	0	02	P * Q
0	0	0	0	1	1	03	COMPARE P AND T
0	0	0	1	0	0	04	MAX P, T
0	0	0	1	0	1	05	MIN P, T
0	0	0	1	1	0	06	CONVERT T TO INTEGER
0	0	0	1	1	1	07	SCALE T TO INTEGER BY Q
0	0	1	0	0	0	08	(P * Q) + T
0	0	1	0	0	1	09	ROUND T TO INTEGRAL VALUE
0	0	1	0	1	0	0A	RECIPROCAL SEED OF P
0	0	1	0	1	1	0B	CONVERT T TO ALTERNATE F, P FORMAT
0	0	1	1	0	0	0C	CONVERT T FROM ALTERNATE F, P FORMAT
0	0	1	1	0	1	0D	
0	0	1	1	1	0	0E	
0	0	1	1	1	1	OF	
I5	I4	I3	I2	I1	I0		OPERATION (INTEGER)
1	0	0	0	0	0	20	P
1	0	0	0	0	1	21	P + T
1	0	0	0	1	0	22	P * Q
1	0	0	0	1	1	23	COMPARE P AND T
1	0	0	1	0	0	24	MAX P, T
1	0	0	1	0	1	25	MIN P, T
1	0	0	1	1	0	26	CONVERT T TO INTEGER
1	0	0	1	1	1	27	SCALE T TO INTEGER BY Q
1	0	1	0	0	0	28	
1	0	1	0	0	1	29	
1	0	1	0	1	0	2A	
1	0	1	0	1	1	2B	
1	1	0	0	0	0	30	P OR T
1	1	0	0	0	1	31	P AND T
1	1	0	0	1	0	32	P EXOR T
1	1	0	0	1	1	33	LOGICAL SHIFT P Q PLACES
1	1	0	1	0	0	34	ARITHMETIC SHIFT P Q PLACES
1	1	0	1	0	1	35	FUNNEL SHIFT P-T Q PLACES
1	1	0	1	1	0	36	
1	1	0	1	1	1	37	
X	1	1	0	0	0	18	MOVE P
X	1	1	1	1	1	1F	LOAD MODE REGISTER

PSEL(0..3), QSEL(0..3), TSEL(0..3) SELECTION CHART

SEL3	SEL2	SEL1	SEL0	HEX	P, Q, T INPUT SELECTED
0	0	0	0	00	R REGISTER
0	0	0	1	01	S REGISTER
0	0	1	0	02	ZERO (0000 0000 0000 0000)
0	0	1	1	03	0.5 * (3FE0 0000 0000 0000)
0	1	0	0	04	1 (3FF0 0000 0000 0000)
0	1	0	1	05	2 (4000 0000 0000 0000)
0	1	1	0	06	3 (4080 0000 0000 0000)
0	1	1	1	07	PI ** (4009 21FB 5444 2D18)
1	0	0	0	08	REGISTER FILE 0
1	0	0	1	09	REGISTER FILE 1
1	0	1	0	0A	REGISTER FILE 2
1	0	1	1	0B	REGISTER FILE 3
1	1	0	0	0C	REGISTER FILE 4
1	1	0	1	0D	REGISTER FILE 5
1	1	1	0	0E	REGISTER FILE 6
1	1	1	1	OF	REGISTER FILE 7

* 0.5 (FLOATING POINT) OR -1 (INTEGER)
** PI (FLOATING POINT) OR MAX NEG (INTEG)

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: FFT CONTROL CARD

Size	Document Number	REV
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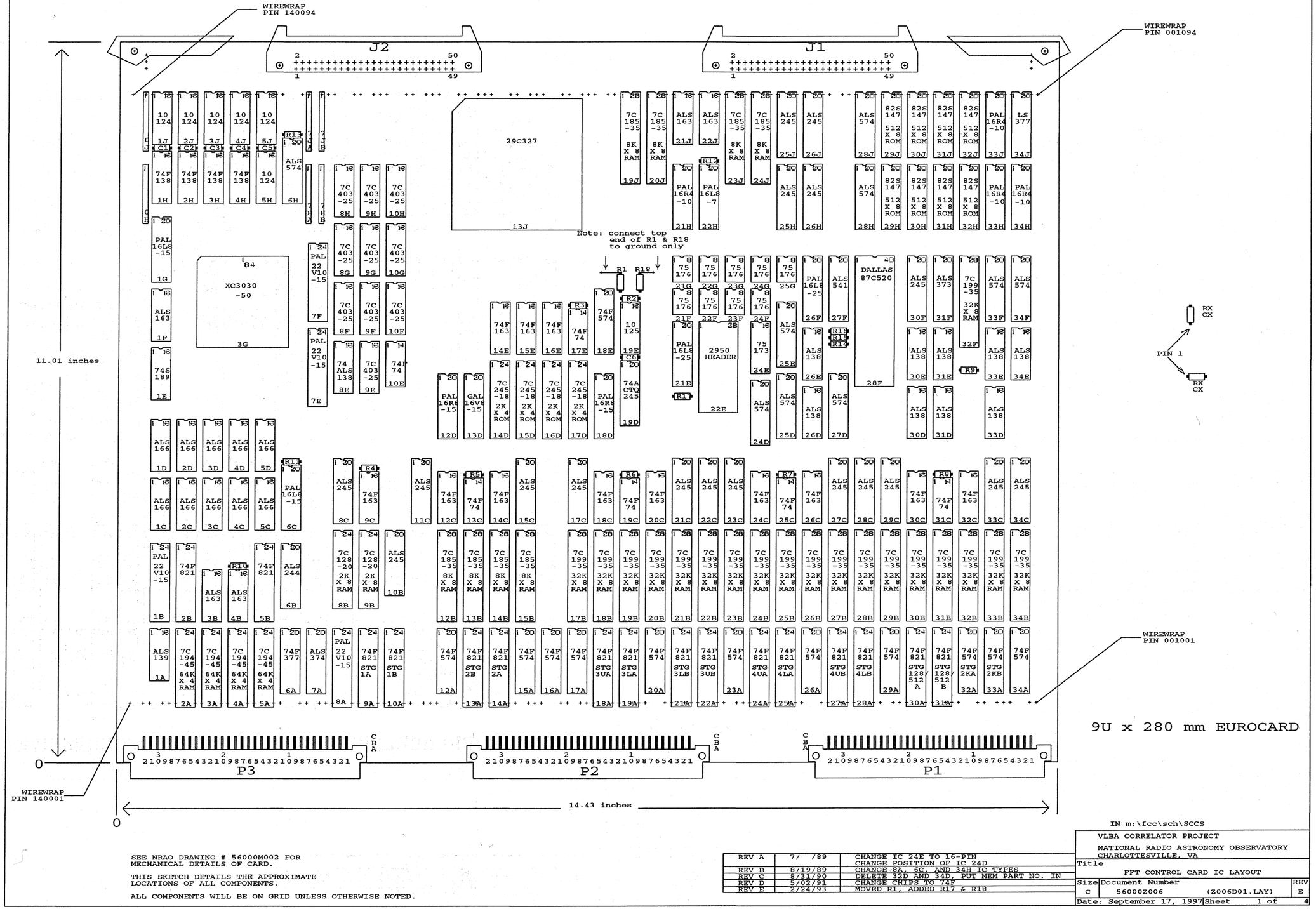
32 MHZ CLK RUNS
Z006D02.LAY

16 MHZ CLK RUNS
Z006D03.LAY

MISC RUNS
Z006D04.RAT



SEE NRAO DRAWING # 56000M002 FOR MECHANICAL DETAILS OF CARD.

THIS SKETCH DETAILS THE APPROXIMATE LOCATIONS OF ALL COMPONENTS.

ALL COMPONENTS WILL BE ON GRID UNLESS OTHERWISE NOTED.

REV A	7/ /89	CHANGE IC 24E TO 16-PIN CHANGE POSITION OF IC 24D
REV B	8/19/89	CHANGE 8A, 6C, AND 34H IC TYPES
REV C	8/31/90	DELETE 32D AND 34D, PUT MEM PART NO. IN
REV D	5/02/91	CHANGE CHIPS TO 74F
REV E	2/24/93	MOVED R1, ADDED R17 & R18

IN m:\fcc\sch\SCCS

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
FFT CONTROL CARD IC LAYOUT

Size	Document Number	REV
C	56000Z006 (Z006D01.LAY)	E

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DRAWINGS ARE B SIZE UNLESS OTHERWISE INDICATED

PULSAR GATE MODEL SHIFT REGISTER

SHEET 2

PAL1B.SCH

FSTC 2 PARAM MODEL GEN CONTROL PAL

SHEET 3

PAL1G.SCH

FRINGE NCO SERIAL INPUT CONTROL PAL

SHEET 4

PAL6C.SCH

FSTC SERIAL WORD MUX 7F & 7E

SHEET 5

C SIZE

PAL7F.SCH

TRIG TABLE SELECTION PAL

SHEET 6

PAL8A.SCH

FFT SEQUENCER DECODE PAL

SHEET 7

PAL12D.SCH

FFT SEQUENCER DECODE PAL

SHEET 8

PAL13D.SCH

FFT SEQUENCER DECODE PAL

SHEET 9

PAL18D.SCH

HCB CONTROLLER PAL

SHEET 10

PAL21E.SCH

WRITE DEGLITCHER

SHEET 11

PAL21H.SCH

MODEL PARAMETER RAM SELECT PAL

SHEET 12

PAL22H.SCH

MISC uP LOGIC PAL

SHEET 13

PAL26F.SCH

MOD GEN MICRO-SEQ ADR GEN 33J & 33H

SHEET 14

PAL33J.SCH

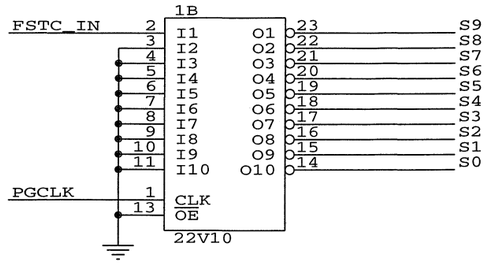
MOD GEN MICRO-SEQ CONTROL PAL

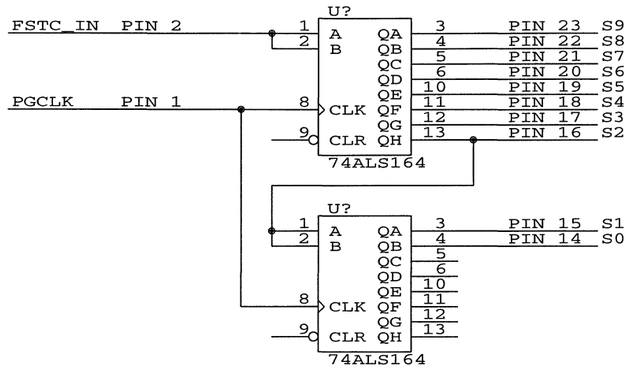
SHEET 15

PAL34H.SCH

Title: FCC PALS		
Size: B	Document Number: FCCTOP.PAL	REV
Date: October 15, 1997	Sheet 1 of 15	

LOCATED L013D04.SCH, CENTER





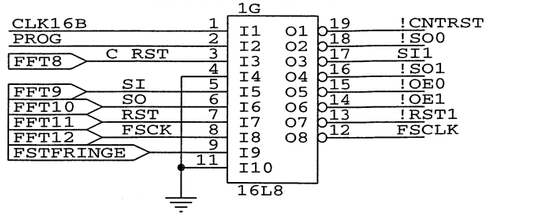
PAL 1B
PULSAR GATE MODEL SHIFT REGISTER

THIS PAL IS A 10-BIT SHIFT REGISTER AND RECEIVES A PULSAR MODEL FROM THE MODEL GENERATOR EVERY 4 mSEC.

```
module PAL_1B
title 'PULSAR GATE SHIFT REGISTER
Ray Escoffier   14 Feb 1991'
                U1B       device          'P22V10' ;

"inputs......................................................................"
                FSTC_IN         PIN 2   ;

"outputs.....................................................................  "
                S9              PIN 23 ;
                S8              PIN 22 ;
                S7              PIN 21 ;
                S6              PIN 20 ;
                S5              PIN 19 ;
                S4              PIN 18 ;
                S3              PIN 17 ;
                S2              PIN 16 ;
                S1              PIN 15 ;
                S0              PIN 14 ;

"definitions................................................................."

"equations..................................................................."
equations


        S0      :=      FSTC_IN         ;
        S1      :=      S0              ;
        S2      :=      S1              ;
        S3      :=      S2              ;
        S4      :=      S3              ;
        S5      :=      S4              ;
        S6      :=      S5              ;
        S7      :=      S6              ;
        S8      :=      S7              ;
        S9      :=      S8              ;

    end PAL_1B
```

Title: PULSAR GATE MODEL SHIFT REGISTER		
Size: B	Document Number: PAL1B.SCH	REV
Date: October 20, 1997	Sheet 2 of 15	

LOCATED L013D04.SCH, LOWER RIGHT



PAL 1G

FSTC 2 PARAMETER MODEL GENERATOR CONTROL PAL

THIS PAL DECODES VARIOUS FFT CYCLE AND FRINGE CYCLE TIMING SIGNALS TO PROVIDE VARIOUS CONTROL SIGNAL REQUIRED BY THE FSTC TWO PARAMETER MODEL GENERATOR.

!CNTRST
PIN 19. THIS PAL OUTPUT PIN SUPPLIES A RESET SIGNAL FOR THE 74LS163. THIS COUNTER RESETS AT THE START OF AN FFT CYCLE AND COUNTS THRU STATION PAIRS DURING AN FFT CYCLE. THIS OUTPUT IS JUST FFT8 EXCEPT WHEN INHIBITED BY THE SIGNAL PROG.

!SO0
PIN 18. THIS PAL OUTPUT CLOCKS FSTC PARAMETERS OUT OF THE UPPER FIFO INTO THE XILINX CHIP.

SI1
PIN 17. THIS PAL OUTPUT CLOCKS FSTC PARAMETERS OUT OF THE XILINX CHIP AND INTO THE LOWER FIFO,

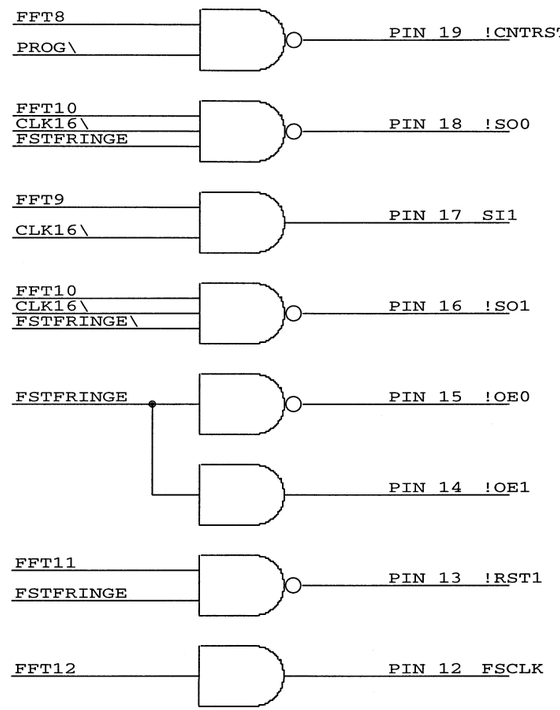
!SO1
PIN 16. THIS PAL OUTPUT CLOCKS FSTC PARAMETERS OUT OF THE LOWER FIFO INTO THE XILINX CHIP.

!OE0
PIN 15. THIS PAL OUTPUT ENABLES THE OUTPUT OF THE UPPER FIFO SO IT CAN DRIVE THE XILINX CHIP.

!OE1
PIN 14. THIS PAL OUTPUT ENABLES THE OUTPUT OF THE LOWER FIFO SO IT CAN DRIVE THE XILINX CHIP.

!RST1
PIN 13. THIS PAL OUTPUT RESETS THE LOWER FSTC PARAMETER FIFO.

FSCLK
PIN 12. THIS PAL OUTPUT IS THE ENABLE FOR FOR THE FSSRCLK CLOCK. BECAUSE CLK16 HAS THE SAME TIMING AS THIS SIGNAL IT MUST BE DELAYED BY PASSING THRU THIS PAL TO AVOID A RACE AT THE 8E 74LE138.




```
module PAL_1G
title 'FSTC MODEL GENERATOR PAL
Ray Escoffier   19 August, 1989'
                U1G      device          'P16L8' ;
"inputs......................................................"
                CLK16           PIN 1 ;
                PROG            PIN 2 ;
                FFT8            PIN 3 ;  "COUNTER 1F RESET"
                FFT9            PIN 5 ;  "FIFO SHIFT IN CLOCK"
                FFT10           PIN 6 ;  "FIFO SHIFT OUT CLOCK"
                FFT11           PIN 7 ;  "FIFO RESET"
                FFT12           PIN 8 ;  "FSCLK"
                FSTFRINGE       PIN 9 ;
"outputs....................................................."
                !CNTRST         PIN 19 ;
                !SO0            PIN 18 ;
                 SI1            PIN 17 ;
                !SO1            PIN 16 ;
                !OE0            PIN 15 ;
                !OE1            PIN 14 ;
                !RST1           PIN 13 ;
                 FSCLK          PIN 12 ;
"definitions................................................."

"equations..................................................."
equations
      CNTRST    =    FFT8   & !PROG                    ;
      SO0       =    FFT10  &  FSTFRINGE               ;
      SI1       =    FFT9                             ;
      SO1       =    FFT10  & !FSTFRINGE               ;
      OE0       =    FSTFRINGE                         ;
      OE1       =   !FSTFRINGE                         ;
      RST1      =    FFT11  &  FSTFRINGE               ;
      FSCLK     =    FFT12                             ;
      end PAL_1G
```

Title: FSTC: 2 PARAM MODEL GENERATOR: CONTROL PAL		
Size: B	Document Number: PAL1G.SCH	REV:
Date: February 6, 1998	Sheet 3 of 15	

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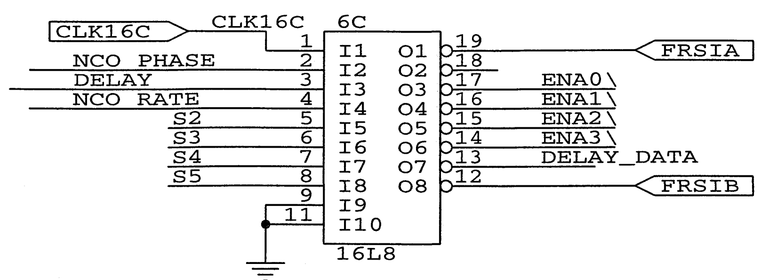

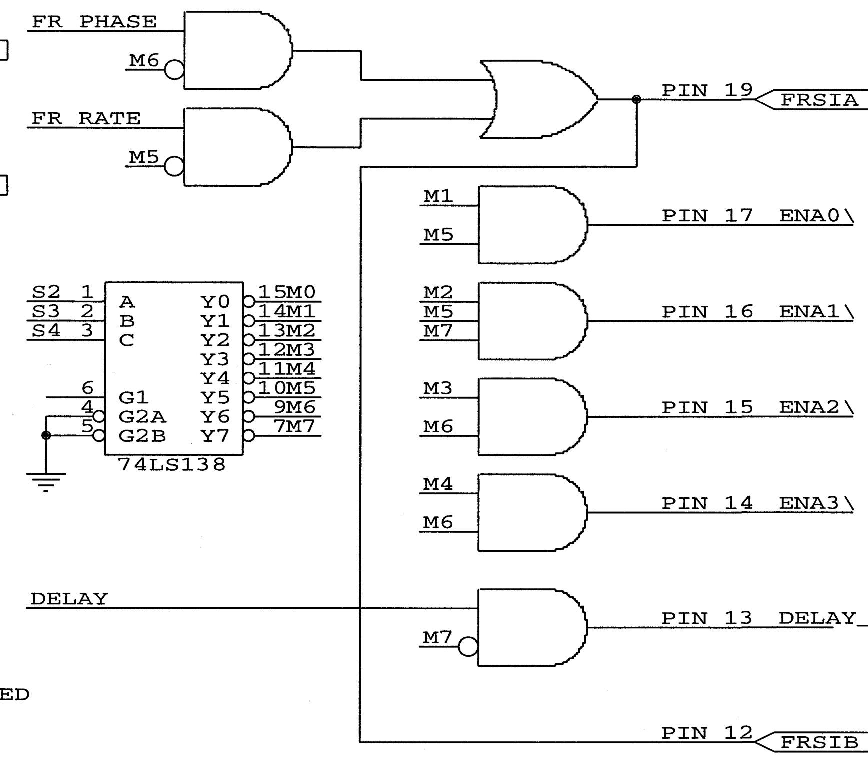

PAL 6C

FRINGE NCO SERIAL INPUT CONTROL PAL

THIS PAL CONTROLS THE CLOCK ENABLES FOR THE 74LS166 SHIFT REGISTERS THAT SHIFT SERIAL MODEL PARAMETERS INTO THE SYSTEM AND THE NCO AND DELAY DATA OUTPUT SIGNALS.

FRSIA
PIN 19. THIS PAL OUTPUT SUPPLIES THE FRINGE PARAMETER DATA OUTPUT. THERE ARE TWO IDENTICAL VERSIONS OF THIS SIGNAL FOR FANOUT REASONS.

PIN 18. THIS PAL OUTPUT IS NOT USED.

ENA0\
PIN 17. THIS PAL OUTPUT SUPPLIES THE CLOCK ENABLE SIGNAL FOR THE 8-BIT SHIFT REGISTER 5C.

ENA1\
PIN 16. THIS PAL OUTPUT SUPPLIES THE CLOCK ENABLE SIGNAL FOR THE 32-BIT SHIFT REGISTER FORMED BY 1C, 2C, 3C, AND 4C.

ENA2\
PINS 15. THIS PAL OUTPUT SUPPLIES THE CLOCK ENABLE SIGNAL FOR THE 8-BIT SHIFT REGISTER 5D.

ENA3\
PIN 14. THIS PAL OUTPUT SUPPLIES THE CLOCK ENABLE SIGNAL FOR THE 32-BIT SHIFT REGISTER FORMED BY 1D, 2D, 3D, AND 4D.

DELAY_DATA
PIN 13. THIS PAL OUTPUT SUPPLIES THE DELAY VALUE OUTPUT.

FRSIB
PIN 12. THIS PAL OUTPUT SUPPLIES THE SECOND FRINGE PARAMETER DATA OUTPUT.

```
module PAL_6C

title 'FRINGE NCO SERIAL INPUT CONTROL PAL

Ray Escoffier    9 August, 1989'
              U6C        device           'P16L8' ;
"inputs..............................................................   "
              FR_PHASE          PIN 2 ;
              DELAY_IN          PIN 3 ;
              FR_RATE           PIN 4 ;
              S2                PIN 5 ;
              S3                PIN 6 ;
              S4                PIN 7 ;
              S5                PIN 8 ;      "NOT USED"
"  S5  S4  S3  S2       FUNCTION                                         "
"---------------------------------------------------------------------   "
"  1   0   0   0     IDLE                                                "
"  0   0   0   1     ENA0\ = 0 OTHER ENABLES INACTIVE     (LOAD 5C)      "
"  0   0   1   0     ENA1\ = 0 OTHER ENABLES INACTIVE     (LOAD 1,2,3,4C) "
"  0   0   1   1     ENA2\ = 0 OTHER ENABLES INACTIVE     (LOAD 5D)      "
"  0   1   0   0     ENA3\ = 0 OTHER ENABLES INACTIVE     (LOAD 1,2,3,4D) "
"  1   1   0   1     ENA0\ AND ENA1\ = 0 OTHERS INACTIVE  (SHIFT 1,2,3,4,5C) "
"  1   1   1   0     ENA2\ AND ENA3\ = 0 OTHERS INACTIVE  (SHIFT 1,2,3,4,5D) "
"  1   1   1   1     ENA1\ = 0 OTHERS INACTIVE  (SHIFT 1,2,3,4C FOR DELAY)  "
"outputs.............................................................   "
               FRSIA          PIN 19                 ;
              !ENA0           PIN 17                 ;
              !ENA1           PIN 16                 ;
              !ENA2           PIN 15                 ;
              !ENA3           PIN 14                 ;
               DELAY          PIN 13                 ;
               FRSIB          PIN 12                 ;
"definitions.........................................................   "
               MODE   =    [S4,S3,S2]                ;
               ENA    =    [ENA3,ENA2,ENA1,ENA0]     ;
"equations...........................................................   "
equations
        FRSIA          =    FR_PHASE & (MODE == [1,1,0])
                          # FR_RATE  & (MODE == [1,0,1])      ;

        ENA            =     [0,0,0,1] & (MODE == [0,0,1])
                          #  [0,0,1,0] & (MODE == [0,1,0])
                          #  [0,1,0,0] & (MODE == [0,1,1])
                          #  [1,0,0,0] & (MODE == [1,0,0])
                          #  [0,0,1,1] & (MODE == [1,0,1])
                          #  [1,1,0,0] & (MODE == [1,1,0])
                          #  [0,0,1,0] & (MODE == [1,1,1])    ;

        DELAY          = DELAY_IN & (MODE == [1,1,1])         ;

        FRSIB          =    FR_PHASE & (MODE == [1,1,0])
                          # FR_RATE  & (MODE == [1,0,1])      ;
     end PAL_6C
```

S5	S4	S3	S2	FUNCTION		MODEL
0	X	X	X	ENABLE ALL SHIFT REGISTERS TO LOAD		
1	X	X	X	ENABLE ALL SHIFT REGISTERS TO SHIFT		
1	0	0	0	IDLE		
0	0	0	1	ENA0\ = 0 OTHER ENABLES INACTIVE	(LOAD 5C)	FRINGE RATE
0	0	1	0	ENA1\ = 0 OTHER ENABLES INACTIVE	(LOAD 1,2,3,4C)	FRINGE RATE OR DELAY
0	0	1	1	ENA2\ = 0 OTHER ENABLES INACTIVE	(LOAD 5D)	FRINGE PHASE
0	1	0	0	ENA3\ = 0 OTHER ENABLES INACTIVE	(LOAD 1,2,3,4D)	FRINGE PHASE
1	1	0	1	ENA0\ AND ENA1\ = 0 OTHERS INACTIVE	(SHIFT 1,2,3,4,5C)	FRINGE RATE
1	1	1	0	ENA2\ AND ENA3\ = 0 OTHERS INACTIVE	(SHIFT 1,2,3,4,5D)	FRINGE PHASE
1	1	1	1	ENA1\ = 0 OTHERS INACTIVE	(SHIFT 1,2,3,4C)	DELAY

NOTE THAT CLK16C IS NOT USED.

FRINGE NCO SERIAL INPUT CONTROL PAL		
Size: B	Document Number: PAL6C.SCH	REV
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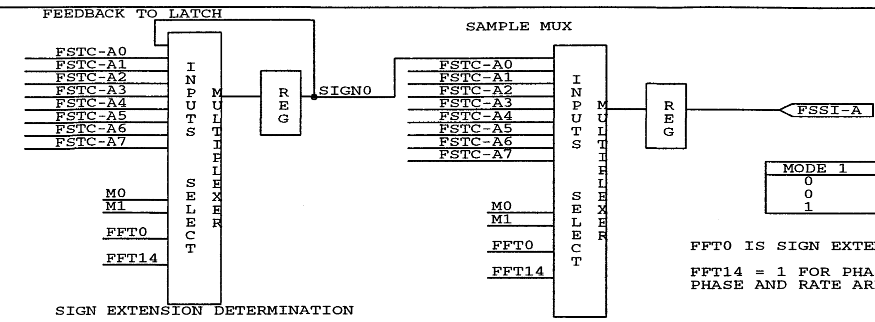


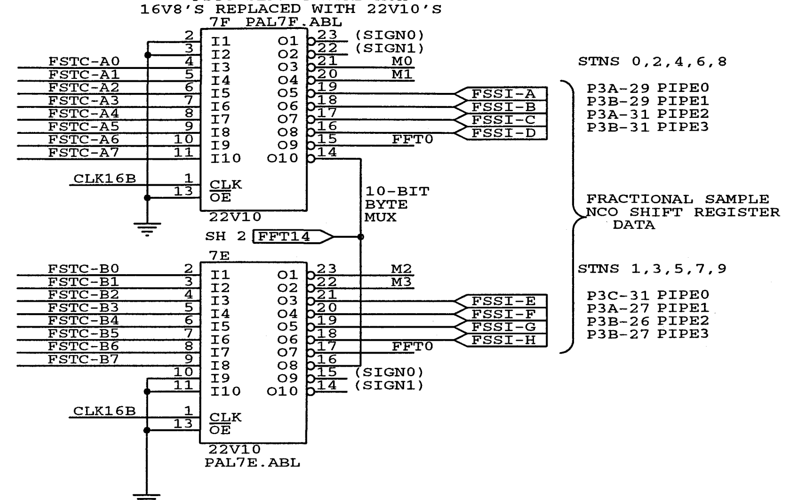
MODE 1	MODE 0	FUNCTION
0	0	64 TO 512 PT FFT
0	1	1024 POINT FFT
1	0	2048 POINT FFT

FFT0 IS SIGN EXTENSION POSITION.

FFT14 = 1 FOR PHASE, 0 FOR RATE
PHASE AND RATE ARE ALTERNATELY SHIFTED OUT.

THESE PALS MUX THE FSTC XILINX OUTPUTS TOGETHER TO GET THE
PROPER FSTC PHASE AND RATE PARAMETERS FOR THE MODE PROGRAMMED.

LOCATED L013D04.SCH, LOWER RIGHT
PAL 7F (ALSO 7E)
FSTC SERIAL WORD MUX
16V8'S REPLACED WITH 22V10'S



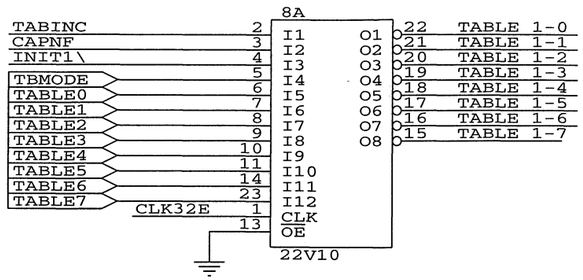

```
module PAL_7E

title 'FSTC DATA MUX PAL

Ray Escoffier   19 August, 1989'

                 U7E      device          'P22V10' ;

" THIS PAL REPLACES THE 16V8 ORIGINAL DESIGN "
" This pal is very similar to pal7f.abl.  See pal7f.abl for detailed "
" comments. "

"inputs..........................................................."

                 FSTC0            PIN 2  ;
                 FSTC1            PIN 3  ;
                 FSTC2            PIN 4  ;
                 FSTC3            PIN 5  ;
                 FSTC4            PIN 6  ;
                 FSTC5            PIN 7  ;
                 FSTC6            PIN 8  ;
                 FSTC7            PIN 9  ;
                 M2               PIN 23 ;
                 M3               PIN 22 ;
                 FFT0             PIN 17 ;
                 FFT14            PIN 16 ;

"internal storage, not used externally............................"

  SIGN0  PIN 15 ;
  SIGN1  PIN 14 ;

"    M3    M2      MODE                                       "
"  ---------------------------------------------              "
"    0     0     64, 128, 256, OR 512 POINT FFT               "
"    0     1     1024 POINT FFT                               "
"    1     0     2048 POINT FFT                               "
"                                                                  "
"     FFT0  = 1 PRODUCES SIGN EXTENSION                            "
"     FFT14 = 0 DURING 10-BIT SHIFTOUT OF THE FSTC NCO PHASE       "
"     FFT14 = 1 DURING 10-BIT SHIFTOUT OF THE FSTC NCO RATE        "

"outputs.........................................................."

                !FSSIE           PIN 21 ;
                !FSSIF           PIN 20 ;
                !FSSIG           PIN 19 ;
                !FSSIH           PIN 18 ;

"definitions......................................................"

                MODE = [M3,M2]                                ;

"
"equations........................................................"

equations

      SIGN0   :=          0  &  (MODE == [0,0])  & !FFT14 & !FFT0    "PHASE"
    #  FSTC2  &  (MODE == [0,0])  &  FFT14 & !FFT0    "RATE"

                   #  FSTC0  &  (MODE == [0,1])  & !FFT14 & !FFT0    "PHASE"
    #  FSTC4  &  (MODE == [0,1])  &  FFT14 & !FFT0    "RATE"

                   #      0  &  (MODE == [1,0])  & !FFT14 & !FFT0    "PHASE"
    #  FSTC4  &  (MODE == [1,0])  &  FFT14 & !FFT0    "RATE"

    #  SIGN0  &                             FFT0    ;

      SIGN1   :=          0  &  (MODE == [0,0])  & !FFT14 & !FFT0    "PHASE"
    #  FSTC3  &  (MODE == [0,0])  &  FFT14 & !FFT0    "RATE"

                   #  FSTC1  &  (MODE == [0,1])  & !FFT14 & !FFT0    "PHASE"
    #  FSTC5  &  (MODE == [0,1])  &  FFT14 & !FFT0    "RATE"

                   #      0  &  (MODE == [1,0])  & !FFT14 & !FFT0    "PHASE"
    #  FSTC4  &  (MODE == [1,0])  &  FFT14 & !FFT0    "RATE"

    #  SIGN1  &                             FFT0    ;
  "PIPE 0"
  "for FSSIE, sign extension, using the sign of the rate, is only applied to"
  "the rates for all fft sizes"
  "since the phase is all zeros, we do not want the sign of the rate applied"
  "to the phase for any of the three FFT sizes for FSSIE (pipe 0)          "

      FSSIE    :=        0   &  (MODE == [0,0])  & !FFT14  & !FFT0  "PHASE"
                  #  FSTC2   &  (MODE == [0,0])  &  FFT14  & !FFT0  "RATE "

                  #      0   &  (MODE == [0,1])  & !FFT14  & !FFT0  "PHASE"
                  #  FSTC4   &  (MODE == [0,1])  &  FFT14  & !FFT0  "RATE "

                  #      0   &  (MODE == [1,0])  & !FFT14  & !FFT0  "PHASE"
                  #  FSTC4   &  (MODE == [1,0])  &  FFT14  & !FFT0  "RATE "

                  #      0                       & !FFT14  &  FFT0  "PHASE"
     #  SIGN0                    &  FFT14  &  FFT0; "RATE "

 "PIPE 1"
 "sign extension, using the sign of the rate, is applied to both phase and "
 "rate except for the phase for fft sizes <= 512 and 2K, which are zero    "

 "The Xilinx FSTC7 term is faulty.  FSTC7 adds ncox1 plus ncox512 for"
 "2K pipe 3 initial phase.  FSTC7 needs sign extension on the ncox1"
 "term.  In the 2K phase equation, we are changing FSTC7 to FSTC6 so"
 "pipe 3 will have the same initial phase as pipe 2.  This is done as an"
 "alternative to fixing the Xilinx.  The error of the initial phase"
 "being slightly off is not considered significant.  For consistancy the"
 "initial phases are made identical for pipes 0 and 1 also."
 "This entailed changing the 2K Phase from FSTC0 to 0. "

      FSSIF    :=        0   &  (MODE == [0,0])  & !FFT14  & !FFT0  "PHASE"
                  #  FSTC2   &  (MODE == [0,0])  &  FFT14  & !FFT0  "RATE "

                  #  FSTC0   &  (MODE == [0,1])  & !FFT14  & !FFT0  "PHASE"
                  #  FSTC4   &  (MODE == [0,1])  &  FFT14  & !FFT0  "RATE "

                  #      0   &  (MODE == [1,0])  & !FFT14  & !FFT0  "PHASE"
                  #  FSTC4   &  (MODE == [1,0])  &  FFT14  & !FFT0  "RATE "

                  #      0   &  (MODE == [0,0])  & !FFT14  &  FFT0  "PHASE 512"
                  #  SIGN0   &  (MODE == [0,0])  &  FFT14  &  FFT0  "RATE  512"
     #  SIGN0  &  (MODE == [0,1])  &               FFT0  "P & R 1K "
                  #      0   &  (MODE == [1,0])  & !FFT14  &  FFT0  "PHASE 2K "
                  #  SIGN0   &  (MODE == [1,0])  &  FFT14  &  FFT0; "RATE 2K "


 " "
 "PIPE 2"
 "for FSSIG, we want the rate sign bit used for sign extension for rates in"
 "all three FFT cases; we want zeros for the upper five bits for 512 and 1K"
 "and we want to pass fstc6 thru during the upper 5 bits for 2K"
 "for 512 and 1K, sign1 is the storage element to use"
 "for 2K, sign0 is same as sign1 and we still use sign1 for the rate"

      FSSIG    :=        0   &  (MODE == [0,0])  & !FFT14  & !FFT0  "PHASE"
                  #  FSTC3   &  (MODE == [0,0])  &  FFT14  & !FFT0  "RATE "

                  #      0   &  (MODE == [0,1])  & !FFT14  & !FFT0  "PHASE"
                  #  FSTC5   &  (MODE == [0,1])  &  FFT14  & !FFT0  "RATE "

                  #  FSTC6   &  (MODE == [1,0])  & !FFT14           "PHASE"
                  #  FSTC4   &  (MODE == [1,0])  &  FFT14  & !FFT0  "RATE "

                  #      0   &  (M3 == 0      )  & !FFT14  &  FFT0  "P 512&1K"
     #  SIGN1  &                     FFT14  &  FFT0; "ALL RATES"

 "PIPE 3"
 "for FSSIH we want sign extension, using the sign of the rate, for all rates"
 "we need the same sign extension for phase in 1K"
 "we want zeros for <=512 phase"
 "The Xilinx FSTC7 term is faulty.  FSTC7 adds ncox1 plus ncox512 for"
 "2K pipe 3 initial phase.  FSTC7 needs sign extension on the ncox1"
 "term.  In the 2K phase equation, we are changing FSTC7 to FSTC6 so"
 "pipe 3 will have the same initial phase as pipe 2.  This is done as an"
 "alternative to fixing the Xilinx.  The error of the initial phase"
 "being slightly off is not considered significant.  For consistancy the"
 "initial phases are made identical for pipes 0 and 1 also."

      FSSIH    :=        0   &  (MODE == [0,0])  & !FFT14  & !FFT0  "PHASE"
                  #  FSTC3   &  (MODE == [0,0])  &  FFT14  & !FFT0  "RATE "

                  #  FSTC1   &  (MODE == [0,1])  & !FFT14  & !FFT0  "PHASE"
                  #  FSTC5   &  (MODE == [0,1])  &  FFT14  & !FFT0  "RATE "

                  #  FSTC6   &  (MODE == [1,0])  & !FFT14           "PHASE"
                  #  FSTC4   &  (MODE == [1,0])  &  FFT14  & !FFT0  "RATE "

                  #      0   &  (MODE == [0,0])  & !FFT14  &  FFT0  "PHASE 512"
                  #  SIGN1   &                      FFT14  &  FFT0  "ALL RATES"
                  #  SIGN1   &  (MODE == [0,1])  & !FFT14  &  FFT0; "PHASE 1K"


 "See pal7f.abl for additional notes"

      end PAL_7E
```

SEE EXTENSIVE COMMENTS IN pal7f.abl
SEE k027d02.blk
SEE fccasm/fcc.doc

IN m:/fcc/sch under SCCS

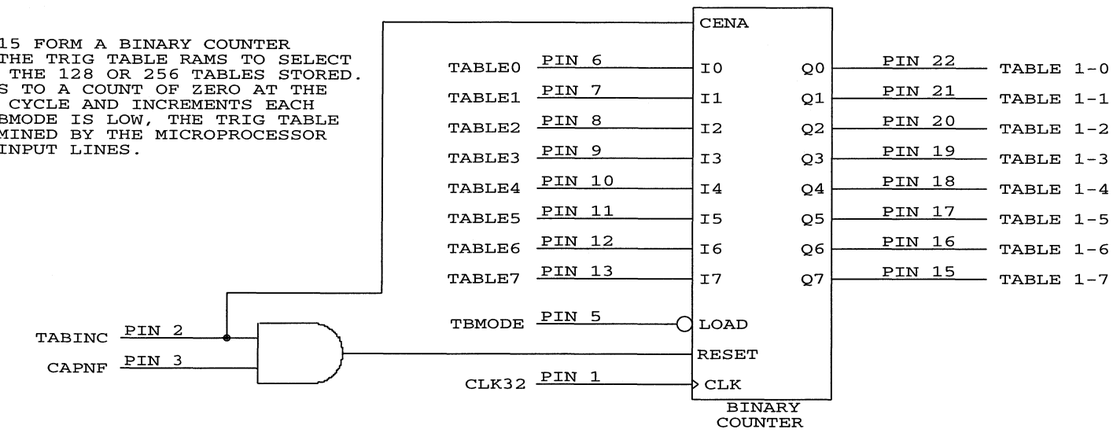
Title		
FSTC SERIAL WORD MUX 7F & 7E		
Size: C	Document Number: PAL7F.SCH	REV
Date: October 20, 1997	Sheet 5 of 15	

LOCATED LOWER LEFT OF L013D02.SCH



PAL 8A
TRIG TABLE SELECTION PAL

PAL PINS 22 THRU 15 FORM A BINARY COUNTER WHICH IS USED BY THE TRIG TABLE RAMS TO SELECT A TRIG TABLE FROM THE 128 OR 256 TABLES STORED. THE COUNTER RESETS TO A COUNT OF ZERO AT THE START OF A FRINGE CYCLE AND INCREMENTS EACH FFT CYCLE. WHEN TBMODE IS LOW, THE TRIG TABLE SELECTED IS DETERMINED BY THE MICROPROCESSOR VIA THE TABLE0-7 INPUT LINES.



LOAD OVERRIDES RESET AND CLEAR.

TBMODE	TABINC	CAPNF	FUNCTION
0	X	X	CLOCK IN uPROC TABLE NUMBER TABLE(0..7)
1	0	X	HOLD TABLE 1-(0..7)
1	1	0	INCREMENT TABLE 1-(0..7)
1	1	1	RESET TABLE 1-(0..7)

NOTE: INIT1\ INTO 8A IS A SPARE INPUT.

```
module PAL_8A
title 'TRIG TABLE CONTROL PAL
Ray Escoffier   28 July 1989'
                U8A         device          'P22V10' ;

"inputs..........................................................."

                TABINC          PIN 2  ;
                CAPNF           PIN 3  ;
               !INIT1           PIN 4  ;
                TBMODE          PIN 5  ;
                TAB0            PIN 6  ;
                TAB1            PIN 7  ;
                TAB2            PIN 8  ;
                TAB3            PIN 9  ;
                TAB4            PIN 10 ;
                TAB5            PIN 11 ;
                TAB6            PIN 14 ;
                TAB7            PIN 23 ;

"outputs.....................................................  "

                TABLE0          PIN 22 ;
                TABLE1          PIN 21 ;
                TABLE2          PIN 20 ;
                TABLE3          PIN 19 ;
                TABLE4          PIN 18 ;
                TABLE5          PIN 17 ;
                TABLE6          PIN 16 ;
                TABLE7          PIN 15 ;

"definitions....................................................."

      TABLE_IN = [TAB6,TAB5,TAB4,TAB3,TAB2,TAB1,TAB0]                ;
      TABLE    = [TABLE6,TABLE5,TABLE4,TABLE3,TABLE2,TABLE1,TABLE0]  ;

"equations......................................................."

equations


    TABLE          :=    (TABLE_IN )  & !TBMODE
                       #  (TABLE    )  &  TBMODE & !TABINC
                       #  (TABLE + 1)  &  TBMODE &  TABINC & !CAPNF
                       #     0         &  TBMODE &  TABINC &  CAPNF          ;


    TABLE7         :=    (TAB7     )  & !TBMODE
                       #     0         &  TBMODE                             ;


      end PAL_8A
```

Title	TRIG TABLE SELECTION PAL	
Size: B	Document Number: PAL8A.SCH	REV:
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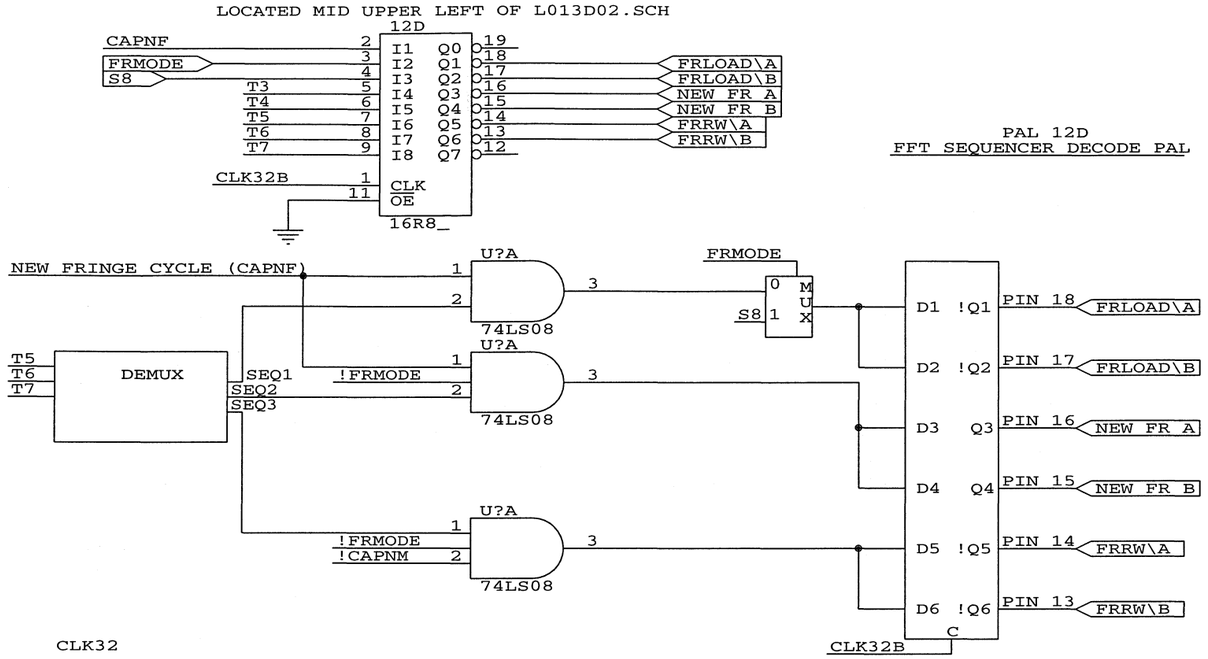
LOCATED MID UPPER LEFT OF L013D02.SCH



PAL 12D
FFT SEQUENCER DECODE PAL

THIS PAL WILL DECODE TIMING SIGNALS GENERATED BY THE FFT CYCLE SEQUENCER TO PROVIDE CONTROL SIGNALS TO THE FFT CARD.

PIN 19. THIS PAL OUTPUT IS NOT USED.

PINS 18 AND 17. THESE PAL OUTPUTS DECODE THE FFT CYCLE SEQUENCER TIMING OUTPUT SIGNALS TO PROVIDE THE FRINGE LOAD SIGNAL FOR THE FFT CARD. THIS SIGNAL COMES NEAR THE BEGINNING OF THE FIRST FFT CYCLE OF A NEW FRINGE CYCLE. TWO IDENTICAL OUTPUTS ARE PROVIDED FOR FANOUT.

PINS 16 AND 15. THESE PAL OUTPUTS DECODE THE FFT CYCLE SEQUENCER TIMING OUTPUT SIGNALS TO PROVIDE THE NEW FRINGE SIGNAL FOR THE FFT CARD. THIS SIGNAL IS CAPTURED BY THE FFT INIT SIGANL ON THE FFT CARD. IT THUS CAN BE A WIDE PULSE NEAR THE FIRST FFT CYCLE OF A NEW FRINGE CYCLE. TWO IDENTICAL OUTPUTS ARE PROVIDED FOR FANOUT.

PINS 14 AND 13. THESE PAL OUTPUTS DECODE THE FFT CYCLE SEQUENCER TIMING OUTPUT SIGNALS TO PROVIDE THE FRINGE REWIND SIGNAL FOR THE FFT CARD. THIS SIGNAL COMES NEAR THE BIGINNING OF EACH FFT CYCLE. TWO IDENTICAL OUTPUTS ARE PROVIDED FOR FANOUT.

PIN 12. THIS PAL OUTPUT IS NOT USED.

PAL 18D, 12D AND 13D FUNCTION TABLE

COUNT	CAPNF	T7	T6	T5	T4	T3	T2	T1	T0	FUNCTION
X	X	X	X	X	X	X	X	X	1/0	STAGE4-ENA = T0, STAGE5-ENA = T0\
X	X	0	0	0	X	0	0	0	X	IDLE
X	X	X	X	X	X	0	0	1	X	INIT1\ = 0
X	X	X	X	X	X	0	1	0	X	INIT2\ = 0
X	X	X	X	X	X	0	1	1	X	INIT3\ = 0
X	X	X	X	X	X	1	0	0	X	INIT4\ = 0
X	X	X	X	X	X	1	0	1	X	INIT5\ = 0
X	X	X	X	X	X	1	1	0	X	INITPG\ = 0
X	1	0	0	1	X	X	X	X	X	FRLOAD\ = 0
X	1	0	1	0	X	X	X	X	X	NEW FR = 1
X	0	0	1	1	X	X	X	X	X	FRRW\ = 0
X	1	0	1	0	X	X	X	X	X	uNEW FRINGE = 1
X	X	1	0	0	X	X	X	X	X	PGFRINGE = 1
6	X	1	0	1	X	X	X	X	X	FSTFRINGE = 1
X	X	1	1	0	X	X	X	X	X	FSLOAD\ = 0

NOTE: T4 IS NOT USED.
WHEN FRMODE IS HIGH FRLOAD AND FRRW ARE INACTIVE AND S8 IS = TO NEW FR.

```
module PAL_12D

title 'FFT SEQ FR DECODER

Ray Escoffier   16 Aug 1989'

                U12D      device          'P16R8' ;
"inputs..........................................................."

                CAPNF           PIN 2 ;
                FRMODE          PIN 3 ;
                S8              PIN 4 ;
                T3              PIN 5 ;
                T4              PIN 6 ;
                T5              PIN 7 ;
                T6              PIN 8 ;
                T7              PIN 9 ;

" FRMODE  S8  T7  T6  T5   CAPNF    CARD     FUNCTION                    "
"-------------------------------------------------------------------------"
"    0     X   0   0   0      X      -       IDLE                        "
"    0     X   0   0   1      1      FFT     FR LOAD ACTIVE              "
"    0     X   0   1   0      1      FFT     NEW FRINGE ACTIVE           "
"    0     X   0   1   1      X      FFT     FRINGE REWIND ACTIVE        "
"    1     0   X   X   X      X      FFT     IDLE                        "
"    1     1   X   X   X      X      FFT     FR LOAD ACTIVE              "
"
"outputs.........................................................."

                !FRLOADA        PIN 18 ;
                !FRLOADB        PIN 17 ;
                 NEWFRA         PIN 16 ;
                 NEWFRB         PIN 15 ;
                !FRRWA          PIN 14 ;
                !FRRWB          PIN 13 ;

"definitions....................................................."

                SEQ = [T7,T6,T5]                                ;

"equations......................................................."

equations

        FRLOADA         :=    (SEQ == [0,0,1]) &  CAPNF & !FRMODE
                            # S8  & FRMODE                      ;
        FRLOADB         :=    (SEQ == [0,0,1]) &  CAPNF & !FRMODE
                            # S8  & FRMODE                      ;
        NEWFRA          :=    (SEQ == [0,1,0]) &  CAPNF & !FRMODE  ;
        NEWFRB          :=    (SEQ == [0,1,0]) &  CAPNF & !FRMODE  ;
        FRRWA           :=    (SEQ == [0,1,1]) & !CAPNF & !FRMODE  ;
        FRRWB           :=    (SEQ == [0,1,1]) & !CAPNF & !FRMODE  ;

    end PAL_12D
```

FFT SEQUENCER DECODE PAL		
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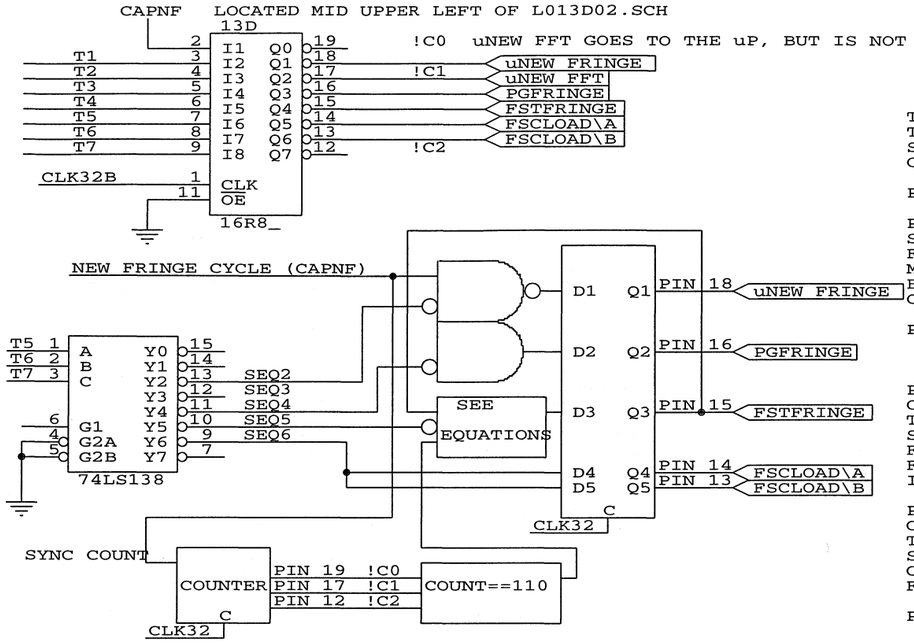

PAL 13D
FFT SEQUENCER DECODE PAL

THIS PAL WILL DECODE TIMING SIGNALS GENERATED BY THE FFT CYCLE SEQUENCER TO PROVIDE CONTROL SIGNALS TO THE FFT CONTROL CARD AND THE FFT CARD.

PIN 19. ONE BIT OF A 3-BIT COUNTER.

PIN 18. THIS PAL OUTPUT DECODES THE FFT CYCLE SEQUENCER TIMING OUTPUT SIGNALS TO PROVIDE A NEW FRINGE INTERRUPT SIGNAL FOR THE FFT CONTROL CARD MICROPROCESSOR. THIS SIGNAL COMES NEAR THE BEGINNING OF THE FRIST FFT CYCLE OF A NEW FRINGE CYCLE.

PIN 17. ONE BIT OF A 3-BIT COUNTER.

PINS 16 AND 15. THESE PAL OUTPUTS DECODE THE FFT CYCLE SEQUENCER TIMING OUTPUT SIGNALS TO PROVIDE THE NEW FRINGE SIGNAL FOR THE FFT CARD. THIS SIGNAL IS CAPTURED BY THE FFT INIT SIGNAL ON THE FFT CARD. IT THUS CAN BE A WIDE PULSE NEAR THE FIRST FFT CYCLE OF A NEW FRINGE CYCLE. TWO IDENTICAL OUTPUTS ARE PRIVIDED FOR FANOUT.

PINS 14 AND 13. THESE PAL OUTPUTS DECODE THE FFT CYCLE SEQUENCER TIMING OUTPUT SIGNALS TO PROVIDE THE FRINGE REWIND SIGNAL FOR THE FFT CARD. THIS SIGNAL COMES NEAR THE BIGINNING OF EACH FFT CYCLE. TWO IDENTICAL OUTPUTS ARE PRIVIDED FOR FANOUT.

PIN 12. ONE BIT OF A 3-BIT COUNTER.

PAL 18D, 12D AND 13D FUNCTION TABLE

COUNT	CAPNF	T7	T6	T5	T4	T3	T2	T1	T0	FUNCTION
X	X	X	X	X	X	X	X	X	1/0	STAGE4-ENA = T0, STAGE5-ENA = T0\
X	X	0	0	0	X	0	0	0	X	IDLE
X	X	X	X	X	X	0	0	1	X	INIT1\ = 0
X	X	X	X	X	X	0	1	0	X	INIT2\ = 0
X	X	X	X	X	X	0	1	1	X	INIT3\ = 0
X	X	X	X	X	X	1	0	0	X	INIT4\ = 0
X	X	X	X	X	X	1	0	1	X	INIT5\ = 0
X	X	X	X	X	X	1	1	0	X	INITPG\ = 0
X	1	0	0	1	X	X	X	X	X	FRLOAD\ = 0
X	1	0	1	0	X	X	X	X	X	NEW FR = 1
X	0	0	1	1	X	X	X	X	X	FRRW\ = 0
X	1	0	1	0	X	X	X	X	X	uNEW FRINGE = 1
X	X	1	0	0	X	X	X	X	X	PGFRINGE = 1
6	X	1	0	1	X	X	X	X	X	FSTFRINGE = 1
X	X	1	1	0	X	X	X	X	X	FSLOAD\ = 0

NOTE: T4 IS NOT USED. COUNT, SHOWN ABOVE, IS TAKEN FROM A 3-BIT COUNTER MADE UP OF PINS 12, 17, AND 19 OF 13D. THIS COUNTER IS USED TO DELAY THE FSTFRINGE SIGNAL 5 FFT CYCLES TO MAKE UP FOR PIPELINNING IN THE FFT CARD.

```
module PAL_13D

title 'FFT SEQ DECODER

Ray Escoffier    16 Aug 1989'

                 U13D       device          'P16R8' ;

"inputs..............................."

        CAPNF            PIN 2 ;
        T1               PIN 3 ;
        T2               PIN 4 ;
        T3               PIN 5 ;
        T4               PIN 6 ;
        T5               PIN 7 ;
        T6               PIN 8 ;
        T7               PIN 9 ;

"    T7  T6  T5    CAPNF    CARD      FUNCTION                                  "
"-------------------------------------------------------------------------------"
"    0   0   0       X       -        IDLE                                      "
"    0   1   0       1       CONT     NEW FRINGE INTRR TO uPROC ( = NEW FR)     "
"    0   1   0       X       CONT     NEW FFT SIGNAL TO uPROC (NOT USED)        "
"    1   0   0       1       CONT     NEW FRINGE SIGNAL TO PULSAR GATE LOGIC    "
"    1   0   1       1       CONT     NEW FRINGE SIGNAL TO FRACT SAMPLE LOGIC   "
"    1   1   0       X       FFT      LOAD FRACTIONAL SAMPLE TIME PARAMETERS    "

"outputs.............................................................."

                !uNEWFRINGE    PIN 18 ;
                 PGFRINGE      PIN 16 ;
                 FSTFRINGE     PIN 15 ;
                !FSCLOADA      PIN 14 ;
                !FSCLOADB      PIN 13 ;
                !C0            PIN 19 ;
                !C1            PIN 17 ;
                !C2            PIN 12 ;

"definitions.........................................................."

                SEQ = [T7,T6,T5]                                    ;
                CNT = [C2,C1,C0]                                    ;

"equations............................................................"

equations

        uNEWFRINGE    :=     (SEQ == [0,1,0]) & CAPNF                ;
        PGFRINGE      :=     (SEQ == [1,0,0])                        ;
        FSTFRINGE     :=     (SEQ == [1,0,1]) & (CNT == [1,1,0])
                          #  (SEQ != [1,0,1]) &  FSTFRINGE           ;
        FSCLOADA      :=     (SEQ == [1,1,0])                        ;
        FSCLOADB      :=     (SEQ == [1,1,0])                        ;

        CNT           :=     CNT          &  (SEQ != [0,1,1])
                          #  [0,0,1]      &  (SEQ == [0,1,1])  &  CAPNF
                          #  (CNT + 1)    &  (SEQ == [0,1,1])  &  (CNT != [0,0,0]) ;

      end PAL_13D
```

FFT SEQUENCER DECODE PAL		
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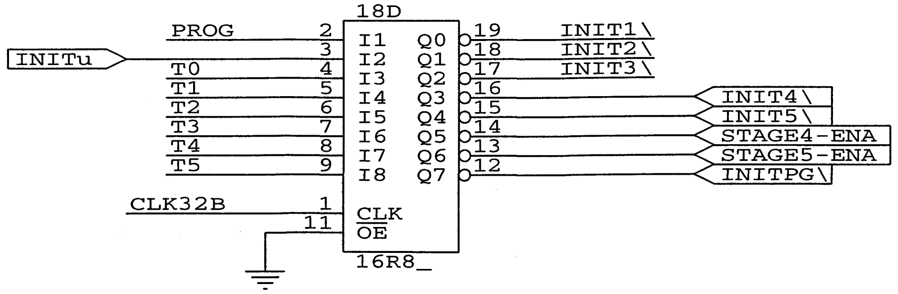
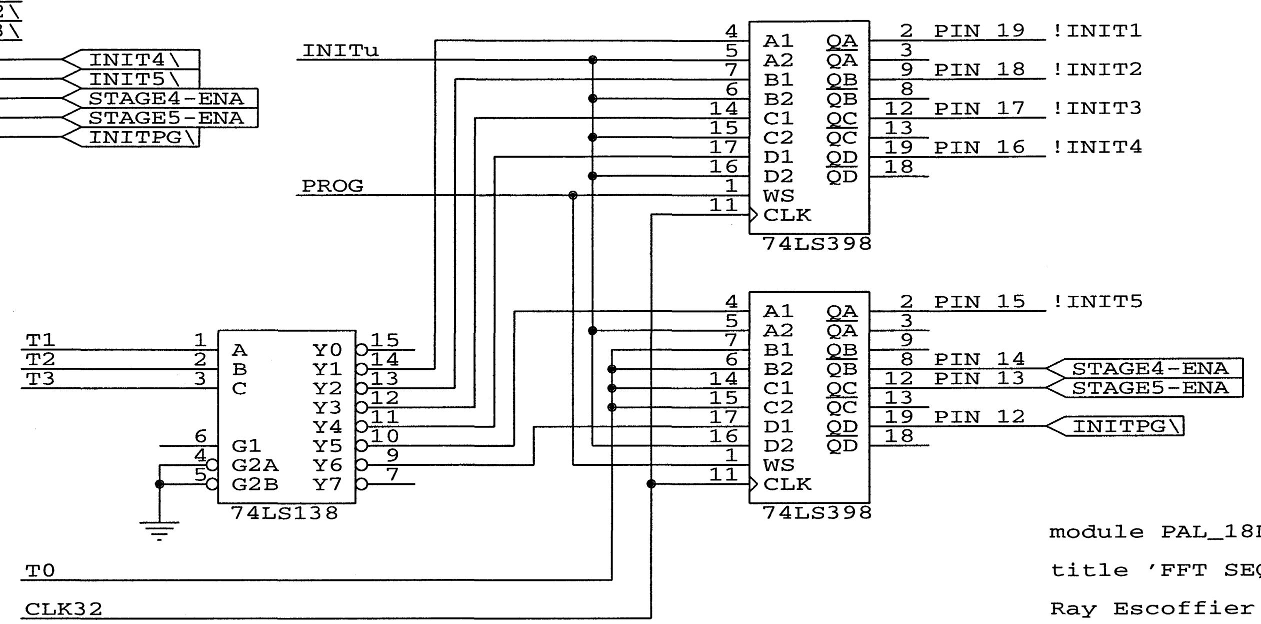
LOCATED MID UPPER LEFT OF L013D02.SCH



PAL 18D
FFT SEQUENCER DECODE PAL

PAL OUTPUT PINS 19, 18, 17, 16, 15, AND 12 DECODE STATES OF THE FFT CYCLE SEQUENCER AND PROVIDE FFT CYCLE INITIATE PULSES FOR THE 5 STAGES OF TRIG TABLES AND FOR THE PULSAR GATE GENERATOR. OUTPUT PINS 14 AND 13 PROVIDE ALTERNATE 1/0 WHICH BECOME THE LS ADDRESS OF STAGE 4 AND STAGE 5 TRIG TABLE. WHEN PROG IS HIGH THE MICROPROCESSOR SIGNAL uINIT REPLACES THE FFT CYCLE SEQUENCER TIMING SIGNAL SO THE MICROPROCESSOR CAN ADDRESS THE TRIG TABLES.



PAL 18D, 12D AND 13D FUNCTION TABLE

COUNT	CAPNF	T7	T6	T5	T4	T3	T2	T1	T0	FUNCTION
X	X	X	X	X	X	X	X	X	1/0	STAGE4-ENA = T0, STAGE5-ENA = T0\
X	X	0	0	0	X	0	0	0	X	IDLE
X	X	X	X	X	X	0	0	1	X	INIT1\ = 0
X	X	X	X	X	X	0	1	0	X	INIT2\ = 0
X	X	X	X	X	X	0	1	1	X	INIT3\ = 0
X	X	X	X	X	X	1	0	0	X	INIT4\ = 0
X	X	X	X	X	X	1	0	1	X	INIT5\ = 0
X	X	X	X	X	X	1	1	0	X	INITPG\ = 0
X	1	0	0	1	X	X	X	X	X	FRLOAD\ = 0
X	1	0	1	0	X	X	X	X	X	NEW FR = 1
X	0	0	1	1	X	X	X	X	X	FRRW\ = 0
X	1	0	1	0	X	X	X	X	X	uNEW FRINGE = 1
X	1	1	0	0	X	X	X	X	X	PGFRINGE = 1
6	1	1	0	1	X	X	X	X	X	FSTFRINGE = 1
X	X	1	1	0	X	X	X	X	X	FSLOAD\ = 0

NOTE: T4 IS NOT USED. THE TABLE ABOVE IS VALID FOR PROG = 0.
WHEN PROG = 1 ALL OUTPUTS OF THE 18D PAL ARE = TO uINIT.

```
module PAL_18D

title 'FFT SEQ INIT DECODER

Ray Escoffier   28 July 1989'

                U18D      device          'P16R8' ;
"inputs.............................................................."

                PROG            PIN 2 ;
                uINIT           PIN 3 ;
                T0              PIN 4 ;
                T1              PIN 5 ;
                T2              PIN 6 ;
                T3              PIN 7 ;
                T4              PIN 8 ;
                T5              PIN 9 ;

"    T5  T4  T3  T2  T1  T0          FUNCTION                          "
"----------------------------------------------------------------------
"    X   X   X   X   X   1/0         STAGE4 = T0 AND STAGE 5 = T0\     "
"    X   X   0   0   0   X           IDLE                              "
"    X   X   0   0   1   X           FFT STAGE 1 INIT ACTIVE           "
"    X   X   0   1   0   X           FFT STAGE 2 INIT ACTIVE           "
"    X   X   0   1   1   X           FFT STAGE 3 INIT ACTIVE           "
"    X   X   1   0   0   X           FFT STAGE 4 INIT ACTIVE           "
"    X   X   1   0   1   X           FFT STAGE 5 INIT ACTIVE           "
"    X   X   1   1   0   X           PULSAR GATE INIT ACTIVE           "
"outputs............................................................."

                !INIT1          PIN 19 ;
                !INIT2          PIN 18 ;
                !INIT3          PIN 17 ;
                !INIT4          PIN 16 ;
                !INIT5          PIN 15 ;
                !STAGE4         PIN 14 ;
                !STAGE5         PIN 13 ;
                !INITPG         PIN 12 ;
"definitions........................................................."
                SEQ = [T3,T2,T1]                                ;
"equations..........................................................."

equations

        INIT1       :=    (SEQ == [0,0,1]) & !PROG  #  !uINIT & PROG     ;
        INIT2       :=    (SEQ == [0,1,0]) & !PROG  #  !uINIT & PROG     ;
        INIT3       :=    (SEQ == [0,1,1]) & !PROG  #  !uINIT & PROG     ;
        INIT4       :=    (SEQ == [1,0,0]) & !PROG  #  !uINIT & PROG     ;
        INIT5       :=    (SEQ == [1,0,1]) & !PROG  #  !uINIT & PROG     ;
        STAGE4      :=    !T0                                            ;
        STAGE5      :=     T0                                            ;
        INITPG      :=    (SEQ == [1,1,0]) & !PROG  #  !uINIT & PROG     ;

      end PAL_18D
```

FFT SEQUENCER DECODE PAL		
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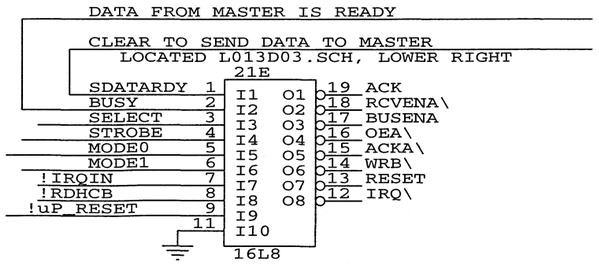


PAL 21E
HCB CONTROLLER PAL

ACK: FOR WRITES FROM MASTER TO 2950, ACK GOES LOW WHEN 2950 IS BUSY, GOES HIGH WHEN 2950 IS READY FOR MORE DATA.

FOR READS OF 2950 BY MASTER, ACK GOES LOW WHEN 2950 HAS NEW DATA, HIGH WHEN MASTER HAS READ THE DATA.

FOR ATTENTION REQUEST FROM SLAVE TO MASTER, ACK GOES LOW; CLEARS WHEN MASTER INTEROGATES SLAVE.

RCVENA\: ENABLE DATA FROM HCB BUS TO LOCAL BUS

BUSENA: ENABLE DATA FROM LOCAL BUS TO HCB BUS

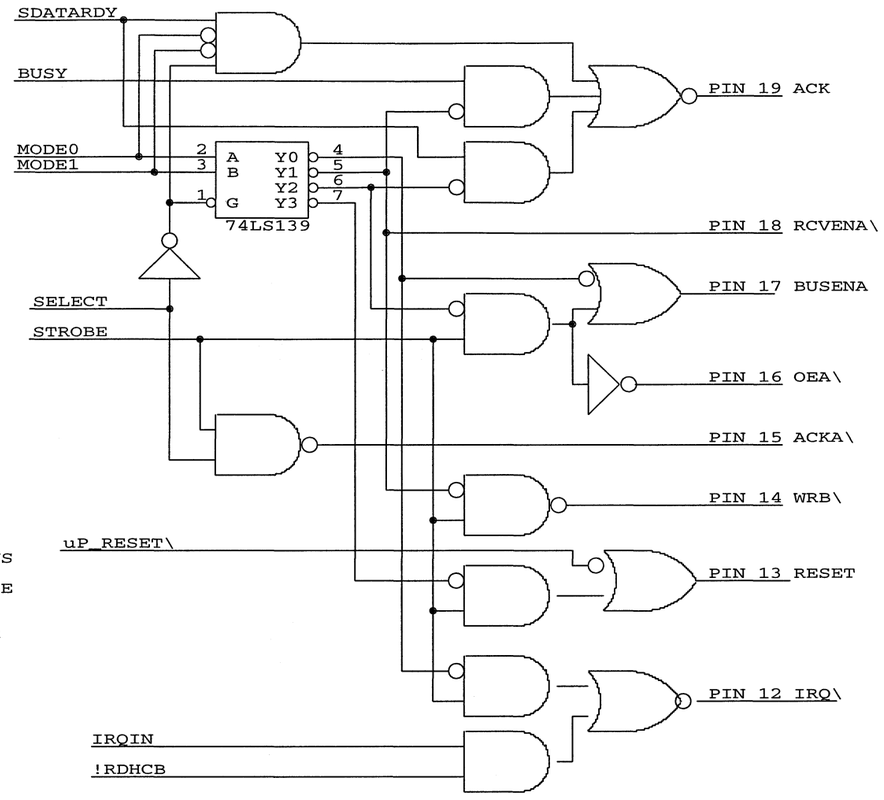
OEA\: ENABLE DATA FROM 2950 PORT A TO LOCAL BUS

ACKA\: ACK PULSE TO 2950 FOR BOTH READ AND WRITE (PULSES LOW, TRAILING EDGE IS ACTIVE)

WRB\: WRITE PULSE TO 2950 FOR WRITES BY MASTER (PULSES LOW, TRAILING EDGE IS ACTIVE)

RESET: HIGH TRUE RESET PULSE

IRQ\: LOW TRUE INTR RQST PULSE TO SLAVE INDICATES NEXT BYTE IS FIRST BYTE OF A TRANSFER FROM MASTER TO SLAVE.



SELECT	STROBE	MODE1	MODE0	FUNCTION	ACK	RCVENA\	BUSENA	OEA\	ACKA\	WRB\	RESET	IRQ\
0	X	0	0	ALLOW SLAVE TO ASSERT ATTN	SDATARDY\	1	0	1	1	1	0	1
0	X	0	1	IDLE	1	1	0	1	1	1	0	1
0	X	1	0	IDLE	1	1	0	1	1	1	0	1
0	X	1	1	IDLE	1	1	0	1	1	1	0	1
1	⎍	0	0	MASTER SENDS IRQ TO SLAVE	1	1	1	1	STROBE\	1	0	STROBE\
1	⎍	0	1	MASTER WRITES TO SLAVE	BUSY\	0	0	1	STROBE\	STROBE\	0	1
1	⎍	1	0	MASTER READS FROM SLAVE	SDATARDY\	1	STROBE	STROBE\	STROBE\	1	0	1
1	⎍	1	1	MASTER RESETS SLAVE	1	1	0	1	STROBE\	1	STROBE	1

```
module PAL_21E  flag '-r3'

title 'HCB CONTROLLER

Ray Escoffier   19 August, 1989'

                U21E      device          'P16L8' ;
" Adapted from firpal11.abl "

"inputs........................."

        SRDY    PIN 1;
        !BUSY   PIN 2;
        SEL     PIN 3;
        STB     PIN 4;
        MD0     PIN 5;
        MD1     PIN 6;
 !IRQIN PIN 7;
 !RDHCB PIN 8;
        !UPRESET PIN 9;
"outputs........................"

        ACK     PIN 19;
        !RENA   PIN 18;
        BENA    PIN 17;
        !OEA    PIN 16;
        !ACKA   PIN 15;
        !WRB    PIN 14;
        RST     PIN 13;
        !IRQ    PIN 12;


"constants......................."

        H,L,X,Z,C       = 1,0,.X.,.Z.,.C.;

        MODE = [SEL,MD1,MD0];

        ATN       = (MODE == [0,0,0]);
        FIRSTBYTE = (MODE == [1,0,0]);
        MOREBYTES = (MODE == [1,0,1]);
        READ      = (MODE == [1,1,0]);
        RESET     = (MODE == [1,1,1]);
        ACKHIGH   = (
                (MODE == [0,0,1]) # (MODE == [0,1,0])
              # (MODE == [0,1,1]) # (MODE == [1,1,1])
              # (MODE == [1,0,0])
            );

        OEAHIGH   = (
                (MODE == [0,0,0]) # (MODE == [0,0,1])
              # (MODE == [0,1,0]) # (MODE == [0,1,1])
              # (MODE == [1,0,0]) # (MODE == [1,0,1])
              # (MODE == [1,1,1])
        );

"equations......................."
equations
        ACK   =    ATN & !SRDY
                 # MOREBYTES & !BUSY
                 # READ & !SRDY
                 # ACKHIGH;

        RENA  =    FIRSTBYTE
                 # MOREBYTES;

        BENA  =    READ & STB;

        OEA   =    READ & STB;

        ACKA  =    (FIRSTBYTE # MOREBYTES # READ # RESET) & STB;

        WRB   =    (FIRSTBYTE # MOREBYTES) & STB;

        RST   =    (RESET & STB) # UPRESET;

 IRQ   =   (FIRSTBYTE & STB) # (IRQIN & !RDHCB);

      end PAL_21E
```

HCB CONTROLLER PAL		
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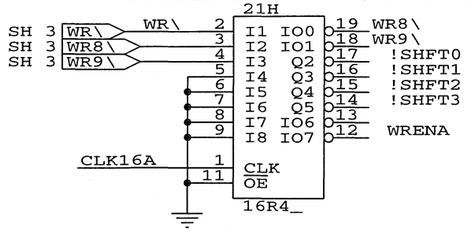

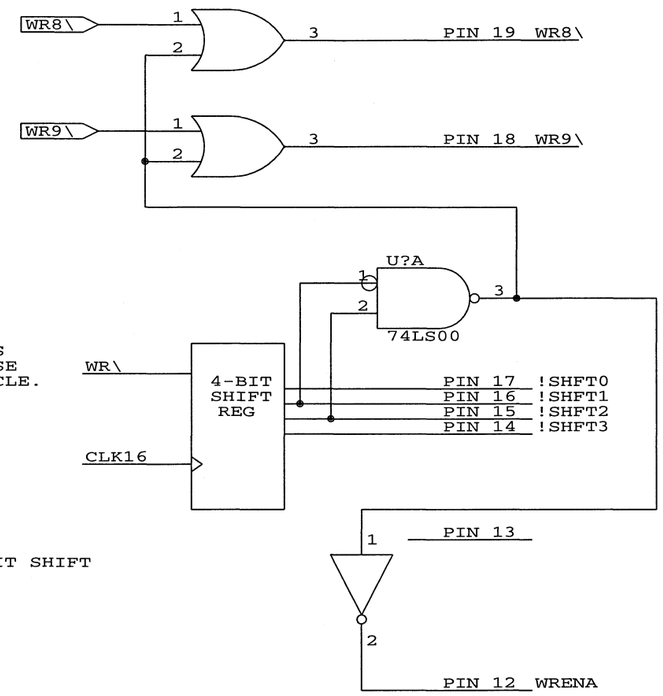

PAL 21H
WRITE DEGLITCHER PAL

THIS PAL WILL PRODUCE GLITCHLESS WRITE SIGNALS FROM THE 87C51 MICROPROCESSOR WR\ SIGNAL. THESE SIGNALS WILL BE ACTIVE FOR ONT CLK16 CLOCK CYCLE.

WR8\ PIN 19. THIS PIN PROVIDES A GLITCHLESS WR9 TERM.

WR9\ PIN 18. THIS PAL PROVIDES A GLITCHLESS WR8 TERM.

!SHFT0 PINS 17 THRU 14. THESE PAL OUTPUTS FORM A 4-BIT SHIFT
!SHFT1 REGISTER.
!SHFT2
!SHFT3

PIN 13. THIS PAL OUTPUT IS NOT USED.

WRENA PIN 12. THIS PAL OUTPUT PROVIDES A ONE CLOCK PULSE DURATION GLITCHLESS GATE THAT CAN BE USED TO DE GLITCH MICROPROCESSOR SELECT LINES IN ADDITION TO WR8 AND WR9..
NOTE THIS WRENA SIGNAL CURRENTLY HAS NO USE OUTSIDE THE PAL.

```
module PAL_21H
title 'MICROPROCESSOR WRITE PULSE DEGLITCHER
Ray Escoffier    27 JULY 1989'

                U21H      device          'P16R4' ;

"inputs......................................................................"

                !WR             PIN 2 ;
                !WR8i           PIN 3 ;
                !WR9i           PIN 4 ;

"outputs.....................................................................  "

                !WR8            PIN 19 ;
                !WR9            PIN 18 ;
                !SHFT0          PIN 17 ;
                !SHFT1          PIN 16 ;
                !SHFT2          PIN 15 ;
                !SHFT3          PIN 14 ;
                 WRENA          PIN 12 ;

"definitions................................................................."

"equations..................................................................."

equations

        WR8             =       SHFT1 & !SHFT2 & WR8i                   ;

        WR9             =       SHFT1 & !SHFT2 & WR9i                   ;

        SHFT0           :=      WR                                      ;
        SHFT1           :=      SHFT0 & WR                              ;
        SHFT2           :=      SHFT1 & WR                              ;
        SHFT3           :=      SHFT2 & WR                              ;

        WRENA            =      SHFT1 & !SHFT2                          ;

end PAL_21H
```

Title: WRITE DEGLITCHER PAL		
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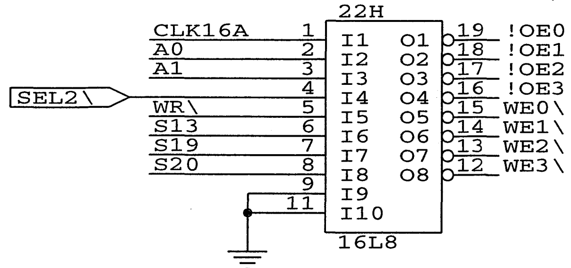
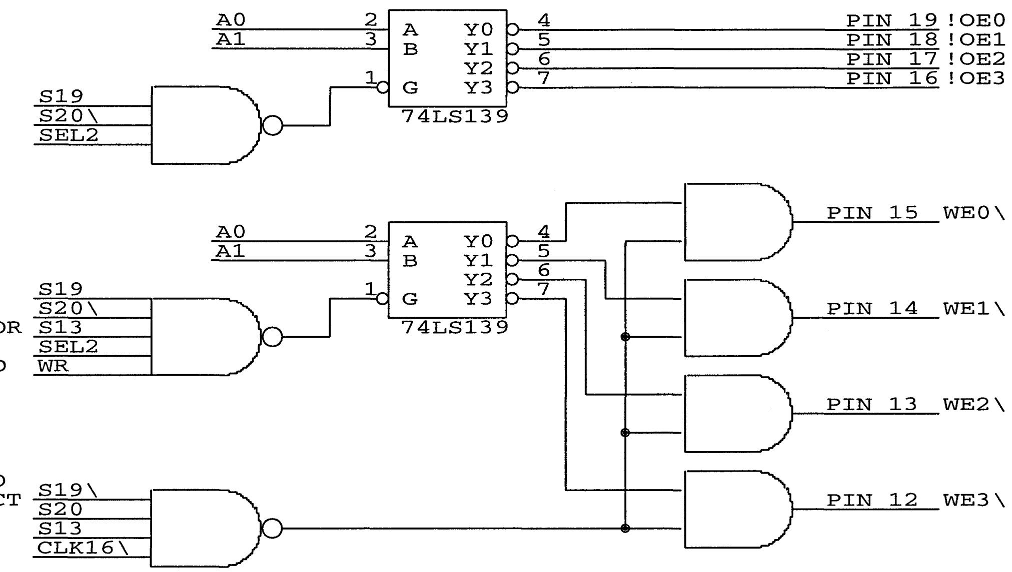
Date: October 20, 1997	Sheet 11 of 15	

LOCATED L013D04.SCH, LOWER LEFT





PAL 22H
MODEL PARAMETER RAM SELECT PAL

THIS PAL PROVIDES FOUR 74LS245 OUTPUT ENABLES FOR THE FOUR BUS TRANCEIVERS THAT ALLOW THE FFT CONTROL CARD MICROPROCESSOR TO WRITE TO AND READ THE MODEL GENERATOR MODEL PARAMETER RAMS. ALSO GENERATED IN THE PAL ARE THE FOUR WRITE SIGNALS FOR THESE FOUR RAMS.

PINS 19 THRU 16. THESE PINS PROVIDE THE OUTPUT ENABLES FOR 74LS245S 25J, 26J, 25H, AND 26H. TWO MICROPROCESSOR ADDRESS BITS ARE DECODED TO SELECT BETWEEN THE FOUR.

PINS 15 THRU 12. THESE PAL OUTPUTS PROVIDE THE FOUR RAM WRITE SIGNAL FOR THE PARAMETER RAM MEMORY. IF THE MICRO IS IN CONTROL OF THE MEMORY TWO ADDRESS BITS DECODE WHICH RAM IS BEING WRITTEN TO. IF THE MODEL GENERATOR MICRO-SEQUENCER IS IN CONTROL OF THE MEMORY ALL FOUR RAMS ARE WRITTEN TO IN PARALLEL.

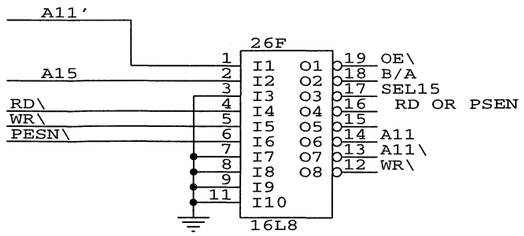
S20	S19	S18	S13	FUNCTION
0	1	1	0	ALLOW MICROPROCESSOR TO READ PARAMETER RAM
0	1	1	1	ALLOW MICROPROECSSOR TO WRITE INTO PARAMETER RAM
1	X	1	X	ENABLE PARAMETER RAM ADDRESS COUNTER TO INCREMENT
1	X	0	X	HOLD PARAMETER RAM ADDRESS COUNTER
1	1	X	0	MICRO INSTRUCTION READS PARAMETER RAM
1	0	X	1	MICRO INSTRUCTION WRITES INTO PARAMETER RAM

ADDR	FUNCTION
A000	READ/WRITE TO RAM 0
A001	READ/WRITE TO RAM 1
A002	READ/WRITE TO RAM 2
A003	READ/WRITE TO RAM 3

```
module PAL_22H

title 'PARAMETER RAM CONTROL PAL

Ray Escoffier     8 August, 1989'

            U22H       device           'P16L8' ;

"inputs.........................."

            CLK16              PIN 1 ;
            A0                 PIN 2 ;
            A1                 PIN 3 ;
           !SEL2               PIN 4 ;
           !WR                 PIN 5 ;
            S13                PIN 6 ;
            S19                PIN 7 ;
            S20                PIN 8 ;

"outputs.........................."

            !OE0             PIN 19 ;
            !OE1             PIN 18 ;
            !OE2             PIN 17 ;
            !OE3             PIN 16 ;
            !WR0             PIN 15 ;
            !WR1             PIN 14 ;
            !WR2             PIN 13 ;
            !WR3             PIN 12 ;
"definitions...................."

            ADDR = [A1,A0]                  ;
"equations......................"

equations

        OE0     =    !S20 &  S19 & (ADDR == [0,0]) & SEL2            ;
        OE1     =    !S20 &  S19 & (ADDR == [0,1]) & SEL2            ;
        OE2     =    !S20 &  S19 & (ADDR == [1,0]) & SEL2            ;
        OE3     =    !S20 &  S19 & (ADDR == [1,1]) & SEL2            ;

        WR0     =    !S20 &  S19 & S13 & (ADDR == [0,0]) & SEL2 & WR
                  #   S20 & !S19 & S13 & !CLK16                      ;

        WR1     =    !S20 &  S19 & S13 & (ADDR == [0,1]) & SEL2 & WR
                  #   S20 & !S19 & S13 & !CLK16                      ;

        WR2     =    !S20 &  S19 & S13 & (ADDR == [1,0]) & SEL2 & WR
                  #   S20 & !S19 & S13 & !CLK16                      ;

        WR3     =    !S20 &  S19 & S13 & (ADDR == [1,1]) & SEL2 & WR
                  #   S20 & !S19 & S13 & !CLK16                      ;

      end PAL_22H
```

MODEL PARAMETER RAM SELECT PAL		
Size: B	Document Number: PAL22H.SCH	REV
Date: October 20, 1997	Sheet 12 of 15	

LOCATED L013D03.SCH, LOWER LEFT TO THE RIGHT OF THE uP.



PAL 26F
MISCELLANEOUS MICROPROCESSOR LOGIC PAL

THIS PAL CONTAINS MISCELLANEOUS LOGIC IN THE MICROPROCESSOR PORTION OF THE FFT CONTROL CARD:

OE\ PIN 19. THIS PIN IS THE LS245 OUTPUT ENABLE. IT IS ACTIVE (LOW) ALL THE TIME EXCEPT FOR RAM 32F READ OPERATIONS.

B/A PIN 18. THIS PAL OUTPUT SUPPLIES THE DIRECTION SIGNAL FOR THE DATA BUS LS245.

SEL15 PIN 17. THIS PAL OUTPUT SUPPLIES A GLITCHLESS A15 SIGNAL FOR THE 74LS138 DECODERS.

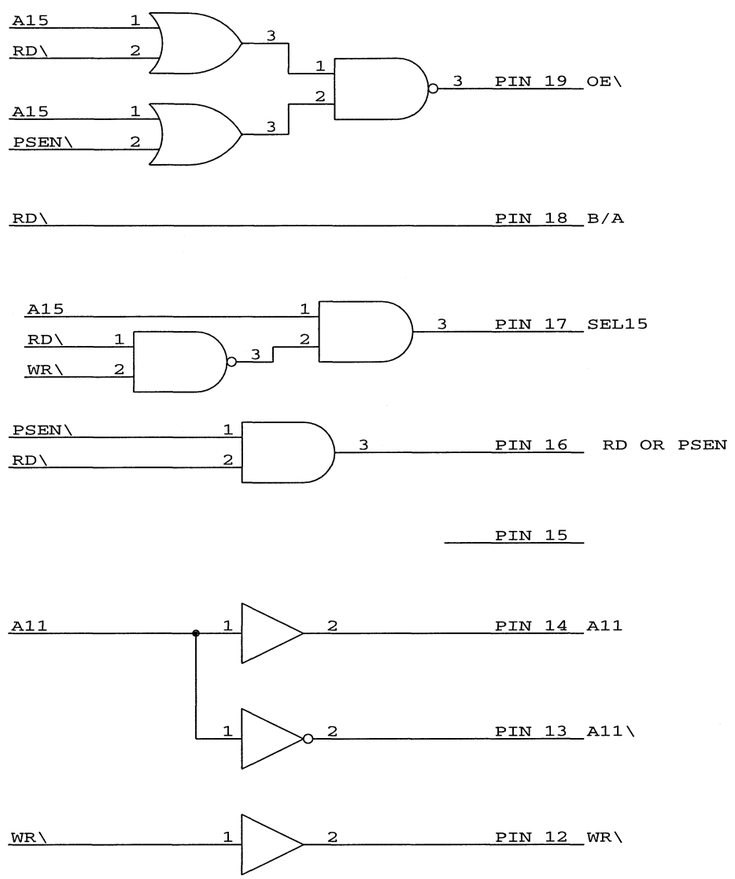
RD OR PSEN PIN 16. THIS PAL OUTPUT PROVIDES THE RAM MEMORY OUTPUT ENABLE SIGNAL FOR EITHER DATA MEMORY ACCESS (RD) OR FOR PROGRAM MEMORY ACCESS (PSEN).

PIN 15. NOT USED.

A11 PIN 14. THIS PAL OUTPUT BUFFERS THE A11 MICRO ADDRESS LINE FOR HIGH FANOUT.

A11\ PIN 13. THIS PAL OUTPUT INVERTS THE A11 MICRO ADDRESS LINE.

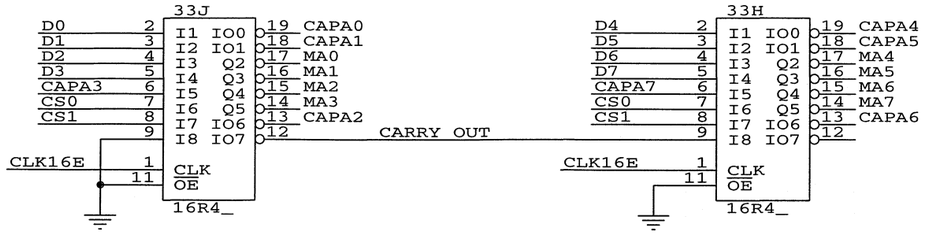
WR\ PIN 12. THIS PAL OUTPUT BUFFERS THE MICRO WR\ LINE FOR HIGH FANOUT.

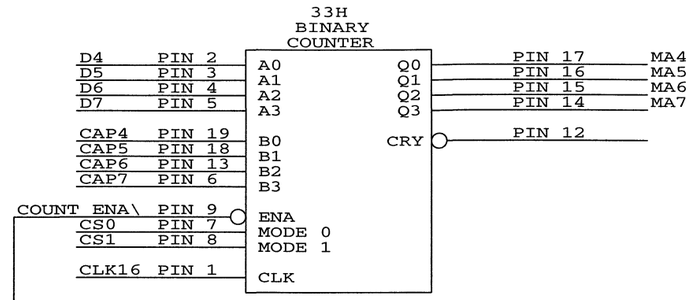



```
module PAL_26F
title 'MISCL MICROPROCESSOR LOGIC
Ray Escoffier   28 July 1989'
                U26F      device          'P16L8' ;
"inputs........................."
                A11i            PIN 1 ;
                A15i            PIN 2 ;
               !RD              PIN 4 ;
               !WRi             PIN 5 ;
               !PSEN            PIN 6 ;
"outputs........................."
                !OE245          PIN 19 ;
                 DIR245         PIN 18 ;
                 SEL15          PIN 17 ;
                !MEMOE          PIN 16 ;
                 A11A           PIN 14 ;
                !A11B           PIN 13 ;
                !WR             PIN 12 ;
"definitions....................."
"equations......................."
equations
   OE245        =   (A15i # !RD)  &  (A15i # !PSEN)     ;
   DIR245       =   !RD                                 ;
   SEL15        =    A15i & (WRi # RD)                  ;
   MEMOE        =    RD # PSEN                          ;
   A11A         =    A11i                               ;
  !A11B         =   !A11i                               ;
   WR           =    WRi                                ;
end PAL_26F
```

MISC uP LOGIC PAL		
Size B	Document Number PAL26F.SCH	REV
Date: October 20, 1997	Sheet 13 of 15	

LOCATED L013D04.SCH, UPPER LEFT
SAME JED FILE FOR 33J AND 33H



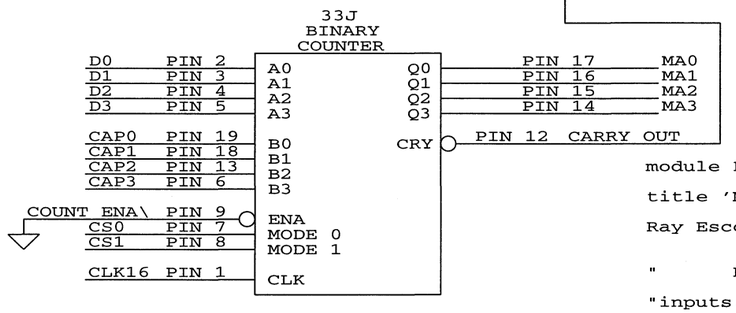


PALS 33J AND 33H
MODEL GENERATOR MICRO-SEQUENCER ADDRESS GENERATOR

THIS PAL IS THE MICRO INSTRUCTION ADDRESS COUNTER FOR THE FLOATING POINT MODEL GENERATOR. IT CAN HOLD A COUNT, INCREMENT, LOAD FROM THE MICROPROCESSOR DATA BUS OR LOAD FROM THE CAPTURE REGISTER. A LOAD FROM THE DATA BUS IS THE MICROPROCESSOR' WAY OF GETTING AN INSTRUCTION STARTED. LOADING FROM THE CAPTURE REGISTER ALLOWS MICRO STEP LOOPS TO BE IMPLEMENTED. THE CS0 AND CS1 ARE THE FUNCTION CODE INPUTS.

OUTPUT PINS 17, 16, 15, AND 14 ARE THE BINARY COUNT OUTPUT PINS.

OUTPUT PIN 12 IS THE COUNTER CARRY\ OUTPUT.



MODE 1	MODE 0	COUNT ENA\	FUNCTION
0	0	X	HOLD
0	1	1	HOLD
0	1	0	INCREMENT
1	0	X	LOAD FROM B
1	1	X	LOAD FROM A

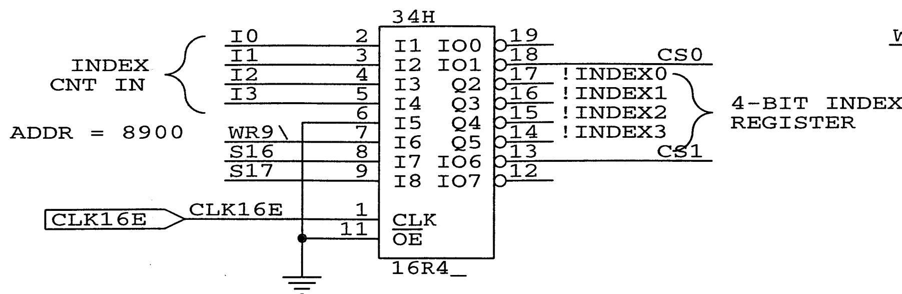
WR9\	S17	S16	INDEX	CS1	CS0	ADDRESS COUNTER	INDEX COUNTER
0	X	X	X	1	1	LOAD FROM DATA BUS	HOLD
1	0	0	X	0	0	HOLD	HOLD
1	0	1	X	0	1	INCREMENT	HOLD
1	1	0	X	0	1	INCREMENT	LOAD I0 - I3
1	1	1	NOT ZERO*	1	0	LOAD FROM CAP REG	DECREMENT
1	1	1	ZERO*	0	1	INCREMENT	HOLD

* POST DECREMENT

```
module PAL_33J

title 'MICRO-INSTRUCTION PROGRAM COUNTER PAL

Ray Escoffier    8 August, 1989'

                U33J      device          'P16R4' ;
"       FFT CONTROL CARD, IC POSITIONS 33J AND 33H                    "

"inputs.........................................................."

                D0              PIN 2 ;
                D1              PIN 3 ;
                D2              PIN 4 ;
                D3              PIN 5 ;
                CAPA3           PIN 6 ;
                CS0             PIN 7 ;
                CS1             PIN 8 ;
                !CARRY_IN       PIN 9 ;
                CAPA0           PIN 19;
                CAPA1           PIN 18;
                CAPA2           PIN 13;


"       CS1     CS0       FUNCTION          "
"-------------------------------------      "
"         0       0     HOLD MA COUNT       "
"         0       1     INCREMENT MA COUNT  "
"         1       0     LOAD FROM CAP REG   "
"         1       1     LOAD FROM DATA BUS  "
"outputs.....................................................  "
                MA0             PIN 17 ;
                MA1             PIN 16 ;
                MA2             PIN 15 ;
                MA3             PIN 14 ;
                !CARRY          PIN 12 ;
"definitions....................................................."
                ADDRESS     = [MA3,MA2,MA1,MA0]             ;
                MODE        = [CS1,CS0]                     ;
                DATA_BUS    = [D3,D2,D1,D0]                 ;
                CAP_REG     = [CAPA3,CAPA2,CAPA1,CAPA0]     ;
"equations......................................................."

equations

        ADDRESS  :=    (ADDRESS     ) & (MODE == [0,0])
                     # (ADDRESS     ) & (MODE == [0,1]) & (CARRY_IN == 0)
                     # (ADDRESS + 1) & (MODE == [0,1]) & (CARRY_IN == 1)
                     # (CAP_REG     ) & (MODE == [1,0])
                     # (DATA_BUS    ) & (MODE == [1,1])                ;

         CARRY    =    (ADDRESS == [1,1,1,1])                         ;

        end PAL_33J
```

MOD GEN MICRO-SEQ ADR GEN 33J & 33H		
Size B	Document Number PAL33J.SCH	REV
Date: October 20, 1997	Sheet 14 of 15	

LOCATED L013D04.SCH, UPPER LEFT



PAL 34H

MODEL GENERATOR MICRO-SEQUENCER CONTROL PAL

THIS PAL CONTROLS THE MODEL GENERATOR MICRO-SEQUENCER ADDRESS COUNTER ON THE FFT CONTROL CARD.

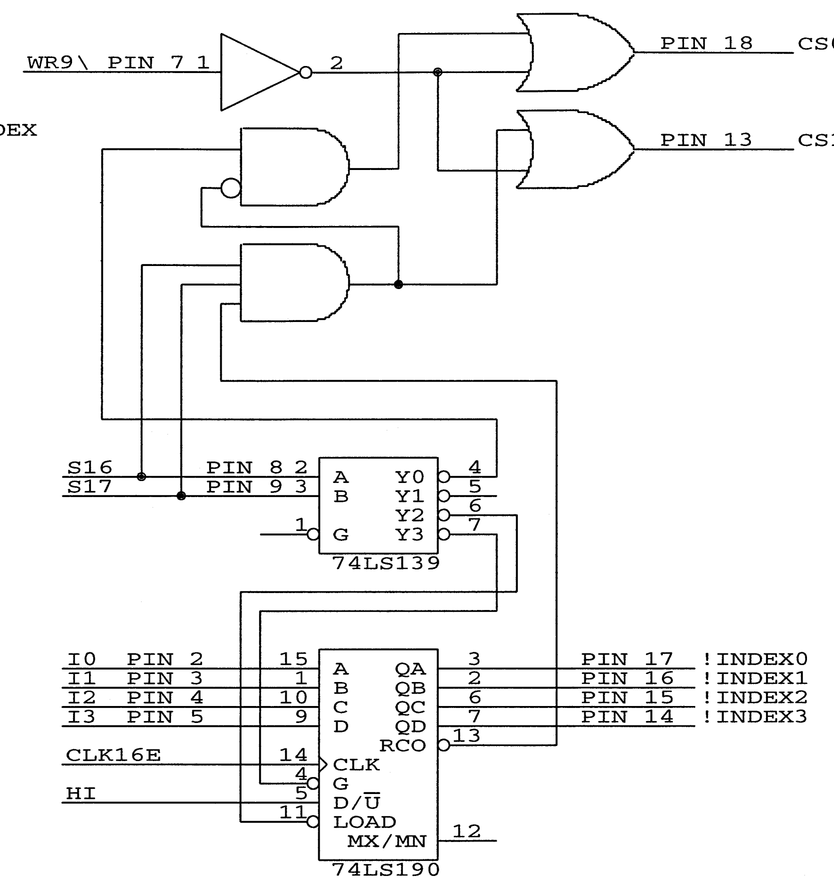
PIN 19. THIS PIN IS NOT USED.

CS0 PIN 18. THIS PAL OUTPUT SUPPLIES ONE OF TWO CONTROL SIGNALS FOR THE MICRO-SEQUENCER ADDRESS COUNTER PALS 33J AND 33H.

!INDEX0 !INDEX1 !INDEX2 !INDEX3 PINS 17 THRU 14. THESE PAL OUTPUTS FORM A 4-BIT BINARY COUNTER. A MICRO INSTRUCTION WILL LOAD THIS COUNTER WITH AN INDEX NUMBER AND THE MICRO SEQUENCER CAN THEN PERFORM A FIRMWARE LOOP OF MICRO INSTRUCTIONS SET BY THE NUMBER LOADED IN THE COUNTER.

CS1 PIN 13. THIS PAL OUTPUT SUPPLIES THE SECOND OF TWO CONTROL SIGNALS FOR THE MICRO-SEQUENCER ADDRESS COUNTER PALS 33J AND 33H.

PIN 12. THIS PIN IS NOT USED.



WR9\	S17	S16	INDEX	CS1	CS0	ADDRESS COUNTER	INDEX COUNTER
0	X	X	X	1	1	LOAD FROM DATA BUS	HOLD
1	0	0	X	0	0	HOLD	HOLD
1	0	1	X	0	1	INCREMENT	HOLD
1	1	0	X	0	1	INCREMENT	LOAD I0-I3
1	1	1	NOT ZERO*	1	0	LOAD FROM CAP REG	DECREMENT
1	1	1	ZERO*	0	1	INCREMENT	HOLD

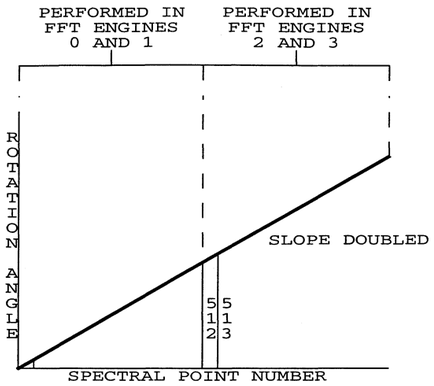
* POST DECREMENT

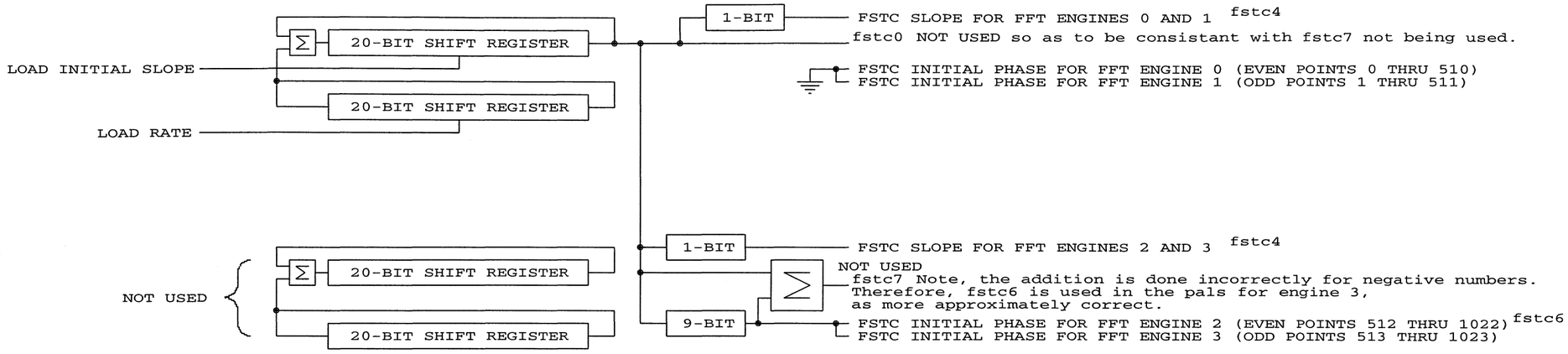
```
module PAL_34H

title 'MICRO-INSTRUCTION PROGRAM COUNTER CONTROL PAL

Ray Escoffier     8 August 1989'

                   U34H      device           'P16R4' ;

"inputs..........................................................."

                   I0                   PIN 2 ;
                   I1                   PIN 3 ;
                   I2                   PIN 4 ;
                   I3                   PIN 5 ;
                   !WR9                 PIN 7 ;
                   S16                  PIN 8 ;
                   S17                  PIN 9 ;

"          S17     S16            FUNCTION                           "
"    ---------------------------------------                         "
"           0       0      HOLD MA COUNT                             "
"           0       1      INCREMENT MA COUNT                        "
"           1       0      LOAD INDEX REGISTER   (AND INC MA COUNT)  "
"           1       1      TEST INDEX REGISTER   (IF = 0 INC, = 1 LOAD CAP) "
"          WR9 = 1, MA COUNT LOADS                                   "
"outputs.........................................................    "
                   CS0                 PIN 18 ;
                   !INDEX0             PIN 17 ;
                   !INDEX1             PIN 16 ;
                   !INDEX2             PIN 15 ;
                   !INDEX3             PIN 14 ;
                   CS1                 PIN 13 ;
"definitions......................................................"
                   MODE_IN      = [S17,S16]                       ;
                   MODE         = [CS1,CS0]                       ;
                   INDEX_LD     = [I3,I2,I1,I0]                   ;
                   INDEX        = [INDEX3,INDEX2,INDEX1,INDEX0]   ;
"equations........................................................"

equations

        MODE        =    [0,0] & (MODE_IN == [0,0]) & !WR9
                       # [0,1] & (MODE_IN == [0,1]) & !WR9
                       # [0,1] & (MODE_IN == [1,0]) & !WR9
                       # [1,0] & (MODE_IN == [1,1]) & !WR9 & (INDEX != 1)
                       # [0,1] & (MODE_IN == [1,1]) & !WR9 & (INDEX == 1)
                       # [1,1] &  WR9                                    ;

         INDEX    :=     INDEX      & !WR9 & (MODE_IN == [0,0])
                       #  INDEX      & !WR9 & (MODE_IN == [0,1])
                       # INDEX_LD    & !WR9 & (MODE_IN == [1,0])
                       # (INDEX - 1) & !WR9 & (MODE_IN == [1,1])        ;

      end PAL_34H
```

MOD GEN MICRO-SEQ CONTROL PAL		
Size: B	Document Number: PAL34H.SCH	REV
Date: October 20, 1997	Sheet 15 of 15	

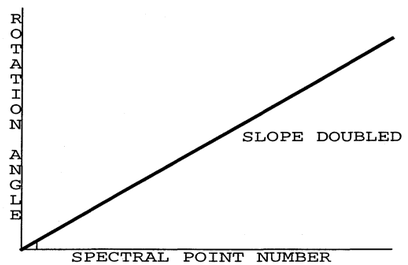
fstc0 through fstc7 refer to Xilinx outputs.

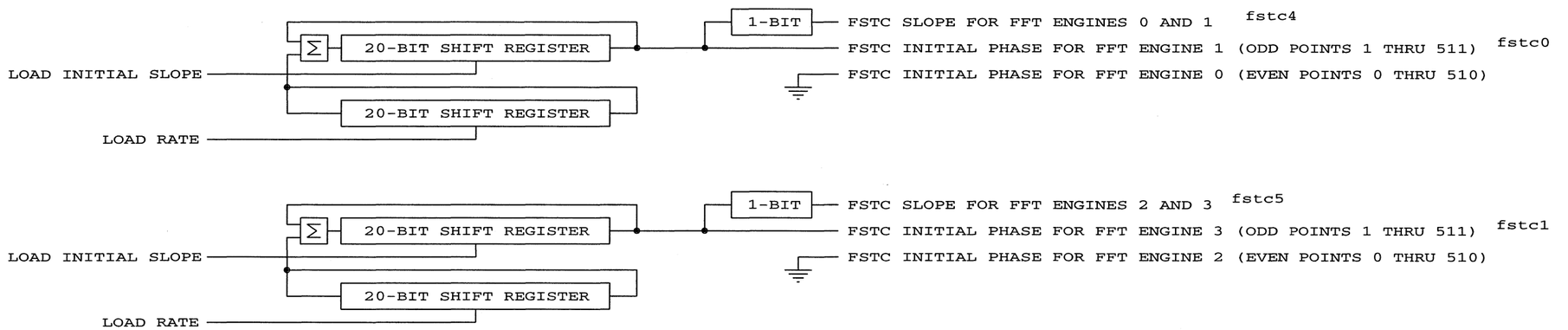
2048 POINT FFT



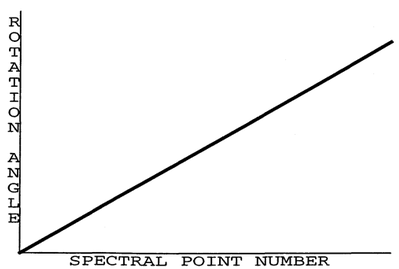


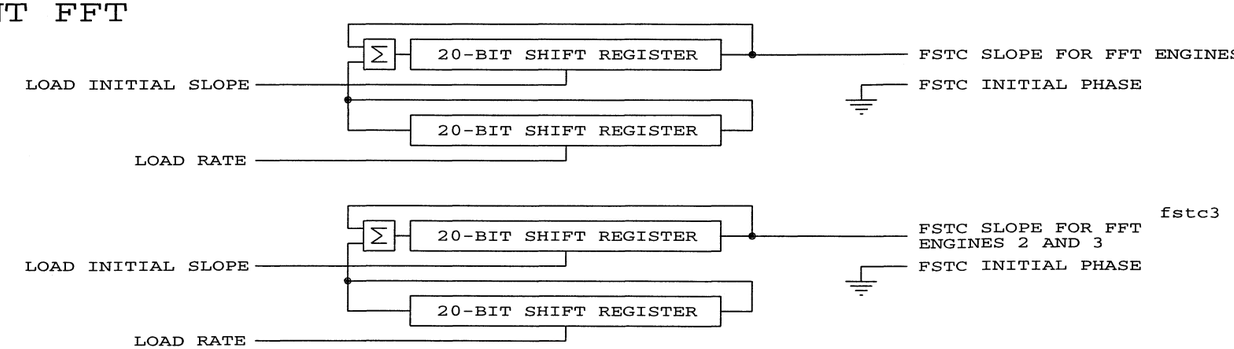
1024 POINT FFT





64 THRU 512 POINT FFT





See pal7e.abl and pal7f.abl
See fccasm/fcc.doc
In m:/fcc/sch/SCCS

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: FSTC XILINX DESIGN		
Size: B	Document Number: 56000K027 (K027D02.BLK)	REV
Date: July 24, 1997	Sheet 2 of 13	

FFT ENGINE 0:

INITIAL PHASE;

64 THRU 512 POINT FFT	ZERO
1024 POINT FFT	ZERO
2048 POINT FFT	ZERO

RATE PARAMETER;

64 THRU 512 POINT FFT	PHASE
1024 POINT FFT	PHASE X 2
2048 POINT FFT	PHASE X 2

FFT ENGINE 1:

INITIAL PHASE;

64 THRU 512 POINT FFT	ZERO
1024 POINT FFT	PHASE
2048 POINT FFT	PHASE

RATE PARAMETER;

64 THRU 512 POINT FFT	PHASE
1024 POINT FFT	PHASE X 2
2048 POINT FFT	PHASE X 2

FFT ENGINE 2:

INITIAL PHASE;

64 THRU 512 POINT FFT	ZERO
1024 POINT FFT	ZERO
2048 POINT FFT	PHASE X 512

RATE PARAMETER;

64 THRU 512 POINT FFT	PHASE
1024 POINT FFT	PHASE X 2
2048 POINT FFT	PHASE X 2

FFT ENGINE 3:

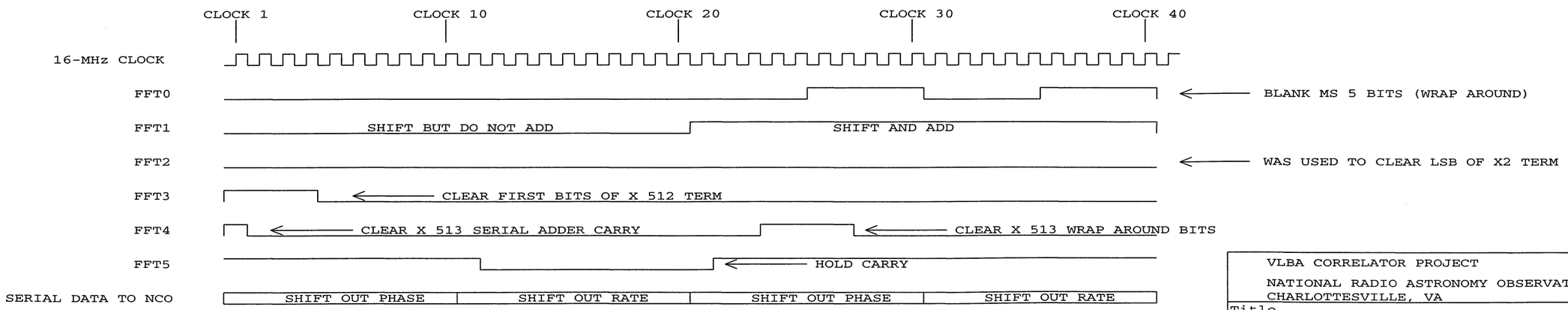
INITIAL PHASE;

64 THRU 512 POINT FFT	ZERO
1024 POINT FFT	PHASE
2048 POINT FFT	PHASE X 513

RATE PARAMETER;

64 THRU 512 POINT FFT	PHASE
1024 POINT FFT	PHASE X 2
2048 POINT FFT	PHASE X 2

	FFT ENGINE 0	FFT ENGINE 1	FFT ENGINE 2	FFT ENGINE 3	
FIRST TEN CLOCKS	INITIAL PHASE = 0	NCO-0P BITS 0 THRU 9 *	000000000 AND NCO-0P-0 **	* PLUS **	2048 POINT FFT
SECOND TEN CLOCKS	0 AND NCO-0P BITS 0 THRU 8	0 AND NCO-0P BITS 0 THRU 8	0 AND NCO-1P BITS 0 THRU 8	0 AND NCO-1P BITS 0 THRU 8	
THIRD TEN CLOCKS	INITIAL PHASE = 0	NCO-0P BITS 10 THRU 19 *	NCO-0P BITS 1 THRU 10 **	* PLUS **	
FOURTH TEN CLOCKS	NCO-0P-9 THRU 18	NCO-0P-9 THRU 18	NCO-1P-9 THRU 18	NCO-1P-9 THRU 18	
FIRST TEN CLOCKS	INITIAL PHASE = 0	NCO-0P BITS 0 THRU 9	INITIAL PHASE = 0	NCO-1P BITS 0 THRU 9	1024 POINT FFT
SECOND TEN CLOCKS	0 AND NCO-0P BITS 0 THRU 8	0 AND NCO-0P BITS 0 THRU 8	0 AND NCO-1P BITS 0 THRU 8	0 AND NCO-1P BITS 0 THRU 8	
THIRD TEN CLOCKS	INITIAL PHASE = 0	NCO-0P BITS 10 THRU 19	INITIAL PHASE = 0	NCO-1P BITS 10 THRU 19	
FOURTH TEN CLOCKS	NCO-0P-9 THRU 18	NCO-0P-9 THRU 18	NCO-1P-9 THRU 18	NCO-1P-9 THRU 18	
FIRST TEN CLOCKS	INITIAL PHASE = 0	SAME AS ENGINE 0	INITIAL PHASE = 0	SAME AS ENGINE 2	64 THRU 512 POINT FFT
SECOND TEN CLOCKS	NCO-0P BITS 0 THRU 9		NCO-1P BITS 0 THRU 9		
THIRD TEN CLOCKS	INITIAL PHASE = 0		INITIAL PHASE = 0		
FOURTH TEN CLOCKS	NCO-0P BITS 10 THRU 19		NCO-1P BITS 10 THRU 19		



NOTE: THE TIMING DIAGRAM ABOVE REPRESENTS IDEALIZED TIMING, PIPELINE STAGES IN THE XILINX CHIP MODIFY THE ACTUAL TIME REQUIREMENTS.

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: FSTC XILINX DESIGN

Size	Document Number	REV
B	56000K027 (K027D03.BLK)	

Date: May 2, 1990 Sheet 3 of 13

3 FFT Card Schematics, Layouts, PAL Schematic Representations

FFT Top Level Schematic l002d39.sch

FFT Card Block Diagrams k031d01.sch, k032d01.sch, k033d01.sch, k034d01.sch, k034d02.sch,l002d35-37

The Famous Star Diagram /corrdwgs/rackwire/l025/l025d26.sch

FFT Schematic l002d01.sch, 02 - 9, 10, 14, 21, 25, 32, 38

FFT Layout z001d01.lay

FFT Card Pal Descriptions L002D34.SCH

BLOCK DIAGRAMS

ASIC FFT FUNCTIONS
K031D01.SCH

FFT CARD SIMPLIFIED BLOCK DIAGRAM
K032D01.SCH

SIMPLIFIED NCO BLOCK DIAGRAM
K033D01.SCH

FFT CARD DETAILED BLOCK DIAGRAM
K034D01.SCH

FRINGE ROTATOR BLOCK DIAGRAM
K034D02.SCH

BIG ROM ANGLE PATHS
L002D37.SCH

2048 POINT FFT
L002D36.SCH

ASIC RAMS
L002D35.SCH

SCHEMATIC

FFT PIN CONNECTIONS
L002D01.SCH

FFT CARD INTERNALS
L002D02.SCH

STAGES 0-3
L002D03.SCH

STAGES 4-5
L002D04.SCH

RAMS
L002D05.SCH

NCO STORE
L002D32.SCH

ANGLE MUX BLOCK DIAGRAM
L002D07.SCH

ANGLE MUX
L002D06.SCH

CAPACITORS
L002D33.SCH

SHEETS 8 THROUGH 31 ARE THE INDIVIDUAL ASIC REPRESENTATIONS.
THEY ARE ACCESSIBLE THROUGH L002D03.SCH AND L002D04.SCH.

PAL DESCRIPTION

PALS
L002D34.SCH

LAYOUT

FFT CARD LAYOUT
Z001D01.LAY

TIMING DIAGRAMS ALSO SEE FFTTFIX/L015D17.SCH

FSTC CE AND LD TIMING
L002D38.SCH

SHEET 1 R2CNT0 TO ANGLE MUX
ANGCE.TIM

SHEET 2 ASIC TO ASIC
ASIC.TIM

SHEET 3 ASIC TO F399 REG
ATOR.TIM

SHEET 4 RAM TO ASIC TWID IN
DRAMTWID.TIM

SHEET 5 ASIC TO EXPOF FF
EXPOF.TIM

SHEET 6 EXT5 REG
EXT5.TIM

SHEET 7 NCO TO BIG ROM TO REG
NCOBROM.TIM

SHEET 8 NCO TO SM ROM TO 399
NCOSROM.TIM

SHEET 9 FR ROM TO ASIC
NEWFR.TIM

SHEET 10 R2CNT0 TO F399 WS
R2C0WS.TIM

SHEET 11 RAM TO ASIC EXT ADR
RAMEXTA.TIM

SHEET 12 RAM TO FSCE
RAMFSCE.TIM

SHEET 13 REGISTER TO ASIC
REG.TIM

SHEET 14 STORE
ST.TIM

SHEET 15 NCO CO TO CI
NCOCOCI.TIM

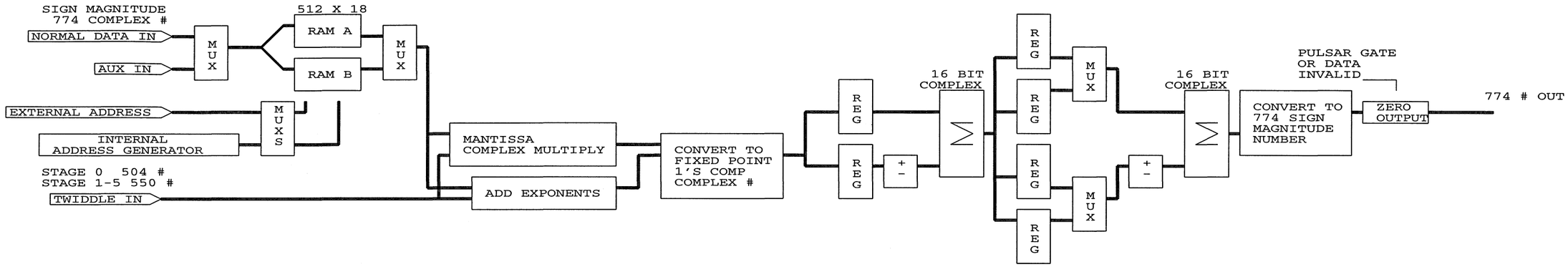
THE *.TIM SHEETS ARE NUMBERED 1 THROUGH 15 IN THE TITLE BLOCKS

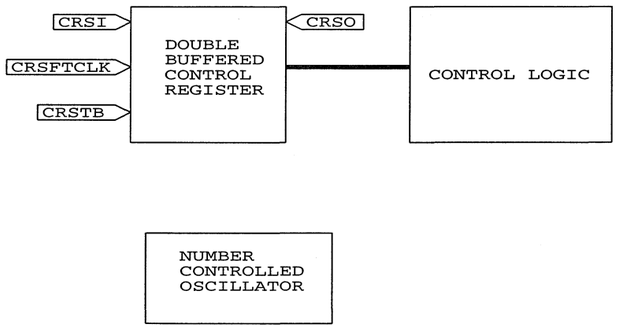
CHANGES TO PROTOTYPE

CHANGES
L002D40.SCH

CHANGES
L002D41.SCH

NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NM		
Title: FFT CARD TOP LEVEL MENU		
Size: B	Document Number: 56000L002 (L002D39.SCH)	REV
Date: May 6, 1997	Sheet 39 of 41	

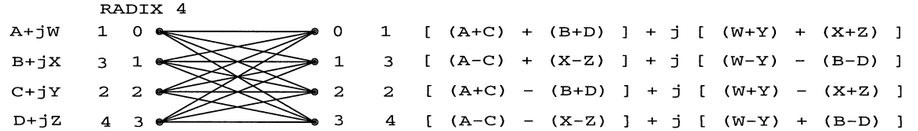




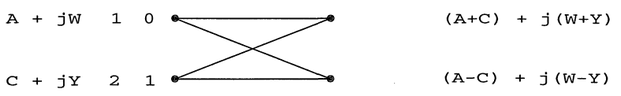
NUMBER
CONTROLLED
OSCILLATOR

RADIX 4 AND RADIX 2 BUTTERFLY OPERATIONS

RADIX 4

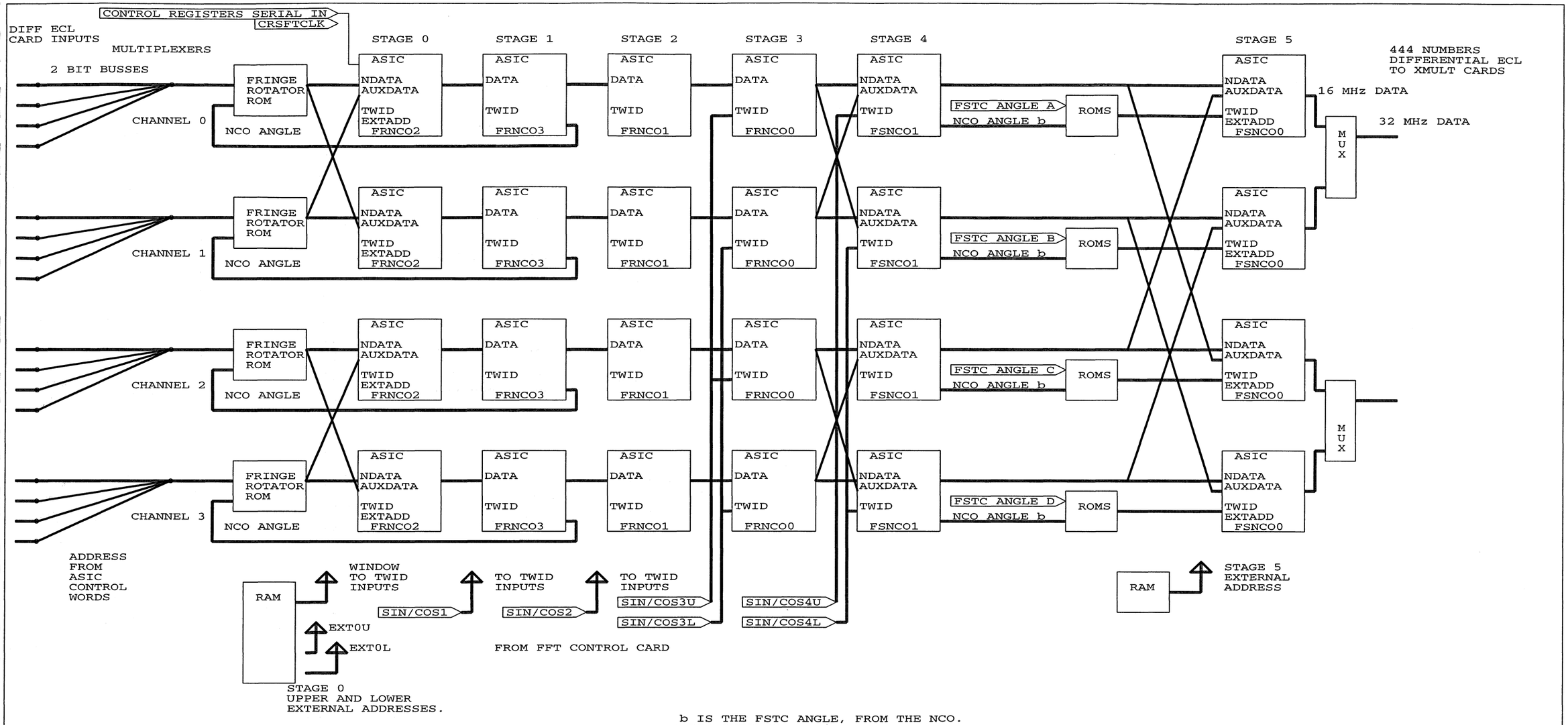


RADIX 2



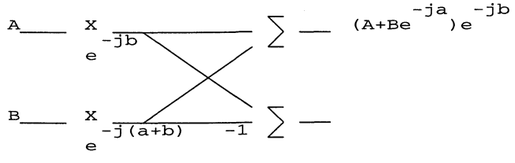
PIPELINE REGISTERS NOT SHOWN

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: ASIC FFT FUNCTIONS		
Size: B	Document Number: 56000K031 (K031D01.SCH)	REV:
Date: June 21, 1989	Sheet 1 of 1	



b IS THE FSTC ANGLE, FROM THE NCO.
A ROM OUTPUTS e**-jb.
a THE TWIDDLE ANGLE FROM THE FFT CONTROL CARD.
A ROM OUTPUTS e**-j(a+b).

FSTC USING RADIX 2 BUTTERFLY



IF FSTC ONLY (IE. NO RADIX 2 STAGE),
AN INPUT FROM THE CONTROL WORDS
TELLS THE ROMS TO OUTPUT e**-jb
ALTERNATED WITH 0.

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

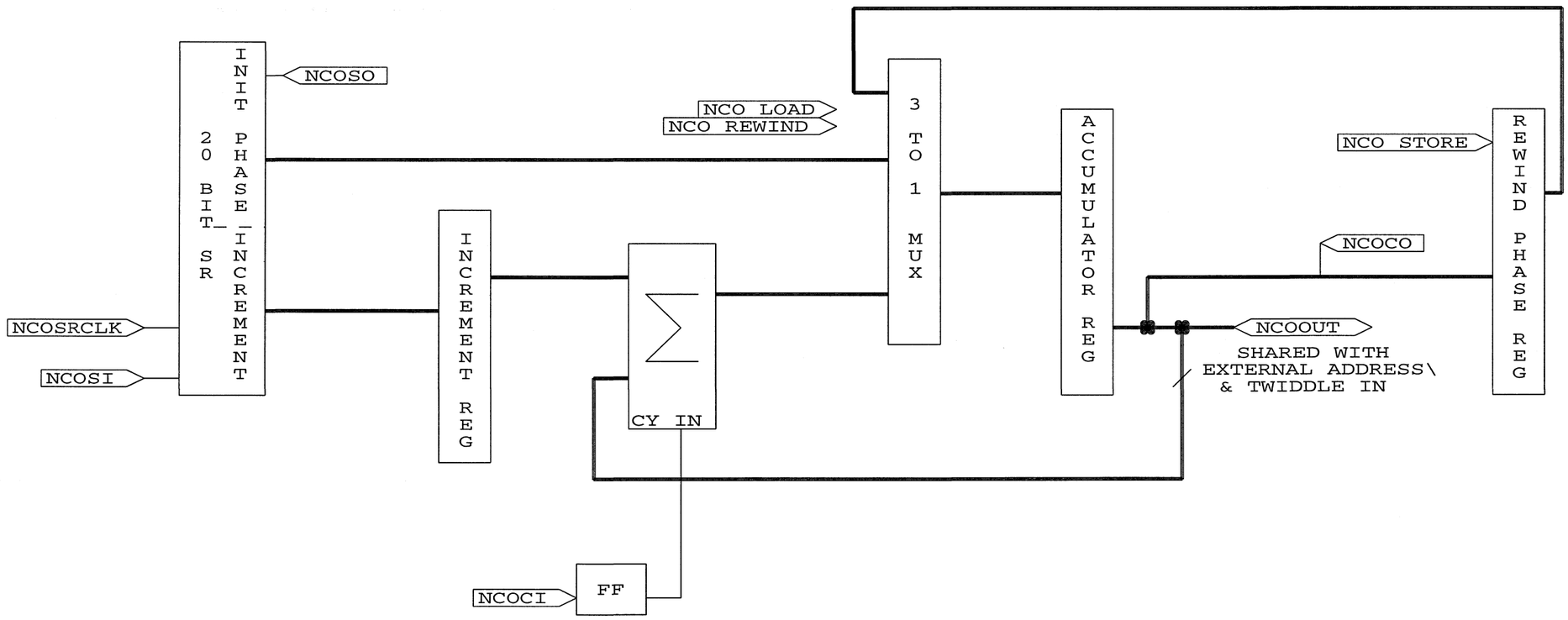
Title
FFT CARD SIMPLIFIED BLOCK DIAGRAM

Size	Document Number	REV
B	56000K032 (K032D01.SCH)	

Date: June 21, 1989 Sheet 1 of 1

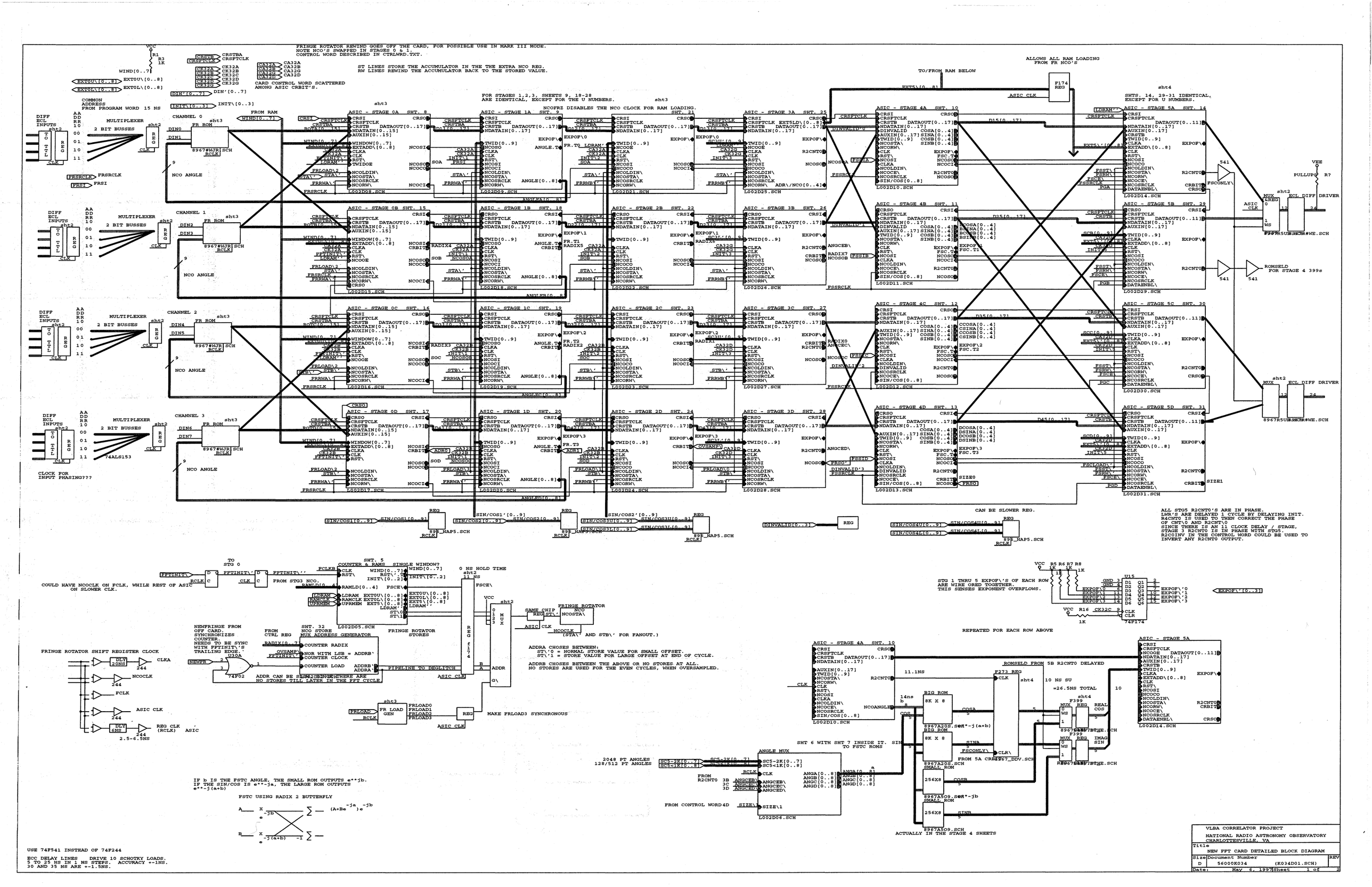
NCO

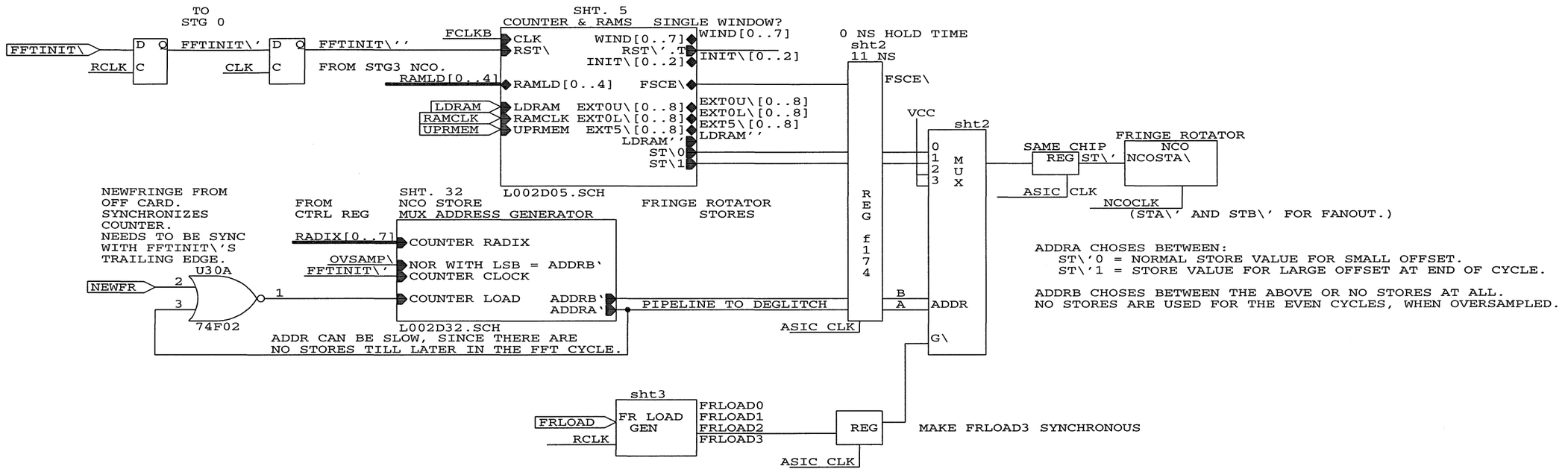
NUMBER CONTROLLED OSCILLATOR



CI FLIPFLOP ALSO REWOUND.

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: SIMPLIFIED NCO BLOCK DIAGRAM		
Size: A	Document Number: 56000K033 (K033D01.SCH)	REV:
Date: June 21, 1989	Sheet 1 of 1	


FRINGE ROTATOR REWIND GOES OFF THE CARD, FOR POSSIBLE USE IN MARK III MODE.
NOTE NCO'S SWAPPED IN STAGES 0 & 1.
CONTROL WORD DESCRIBED IN CTRLWRD.TXT.
ST LINES STORE THE ACCUMULATOR IN THE THE EXTRA NCO REG.
RW LINES REWIND THE ACCUMULATOR BACK TO THE STORED VALUE.
CARD CONTROL WORD SCATTERED AMONG ASIC CRBIT'S.
FOR STAGES 1,2,3, SHEETS 9, 18-28 ARE IDENTICAL, EXCEPT FOR THE U NUMBERS.
NCOFRZ DISABLES THE NCO CLOCK FOR RAM LOADING.
ALLOWS ALL RAM LOADING FROM FR NCO'S
TO/FROM RAM BELOW
SHTS. 14, 29-31 IDENTICAL, EXCEPT FOR U NUMBERS.
COMMON ADDRESS FROM PROGRAM WORD 15 NS
MULTIPLEXER 2 BIT BUSSES
CHANNEL 0
CHANNEL 1
CHANNEL 2
CHANNEL 3
NCO ANGLE
ROMSELD FOR STAGE 4 399#
ALL STG5 R2CNTO'S ARE IN PHASE. LWR'S ARE DELAYED 1 CYCLE BY DELAYING INIT. R4CNTO IS USED TO THEN CORRECT THE PHASE OF CNT\0 AND R2CNT\0 STAGE THREE IS AN 11 CLOCK DELAY / STAGE, STAGE 5 R2CNTO IS IN PHASE WITH STG5. R2CGINV IN THE CONTROL WORD COULD BE USED TO INVERT ANY R2CNTO OUTPUT.
CLOCK FOR INPUT PHASING???
COULD HAVE NCOCLK ON FCLK, WHILE REST OF ASIC ON SLOWER CLK.
FRINGE ROTATOR SHIFT REGISTER CLOCK
NEWFRINGE FROM OFF CARD. SYNCHRONIZES COUNTER. NEEDS TO BE SYNC WITH FFTINIT\'S TRAILING EDGE.
ADDR CAN BE SLEWED THERE ARE NO STORES TILL LATER IN THE FFT CYCLE
ADDRA CHOSES BETWEEN: ST\'0 = NORMAL STORE VALUE FOR SMALL OFFSET. ST\'1 = STORE VALUE FOR LARGE OFFSET AT END OF CYCLE.
ADDRB CHOSES BETWEEN THE ABOVE OR NO STORES AT ALL. NO STORES ARE USED FOR THE EVEN CYCLES, WHEN OVERSAMPLED.
STG 1 THRU 5 EXPOF\'S OF EACH ROW ARE WIRE ORED TOGETHER. THIS SENSES EXPONENT OVERFLOWS.
REPEATED FOR EACH ROW ABOVE
SHT 6 WITH SHT 7 INSIDE IT.
2048 PT ANGLES 128/512 PT ANGLES
IF b IS THE FSTC ANGLE, THE SMALL ROM OUTPUTS e**jb. IF THE SIN/COS IS e**-ja, THE LARGE ROM OUTPUTS e**-j(a+b)
FSTC USING RADIX 2 BUTTERFLY
USE 74F541 INSTRAD OF 74F244
ECC DELAY LINES DRIVE 10 SCHOTKY LOADS. 5 TO 25 NS IN 1 NS STEPS. ACCURACY +-1NS. 30 AND 35 NS ARE +-1.5NS.
ACTUALLY IN THE STAGE 4 SHEETS
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
NEW FFT CARD DETAILED BLOCK DIAGRAM
Size D
Document Number 56000K034 (K034D01.SCH)
REV
Date: May 6, 1997 Sheet 1 of 2



VLBA CORRELATOR PROJECT

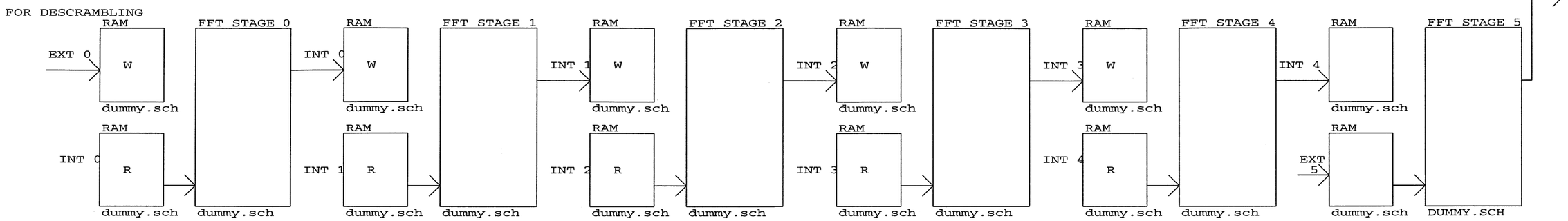
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
FRINGE ROTATOR STORE LOGIC BLOCK DIAGRAM

Size	Document Number	REV
B	56000K034 (K034D02.SCH)	

Date: February 6, 1998 | Sheet 2 of 2

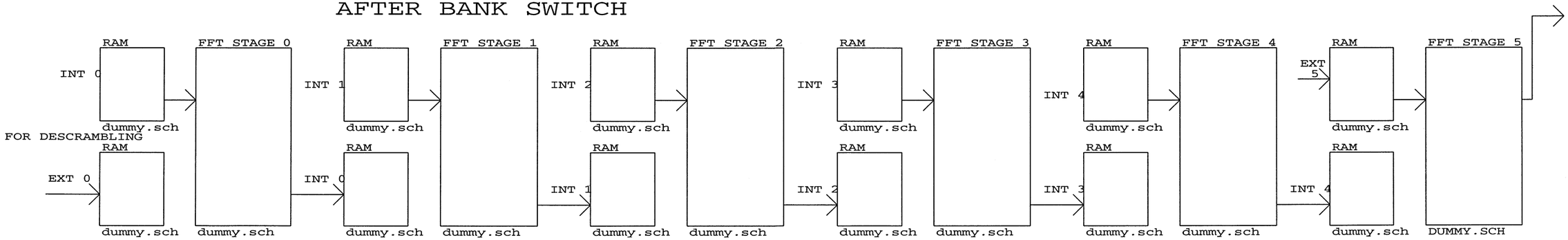
BEFORE BANK SWITCH



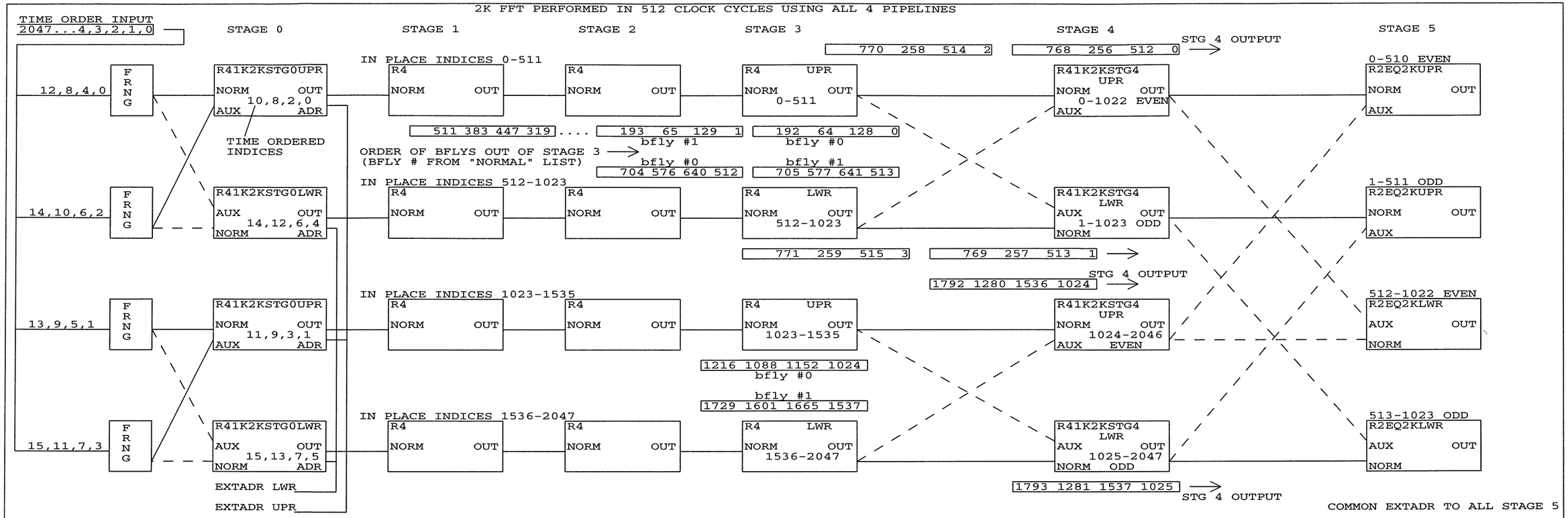
INT 0 THROUGH INT 4 REFER TO RAM ADDRESSES INTERNALLY GENERATED IN THE ASIC, FOR THE SPECIFIED STAGE.

EXT 0 AND EXT 5 REFER TO RAM ADDRESSES EXTERNALLY GENERATED FOR THE SPECIFIED STAGE.

AFTER BANK SWITCH



VLBA CORRELATOR PROJECT	
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA	
Title RAM LAYOUT & ADDRESS GENERATION	
Size B	Document Number 56000L002 (L002D35.SCH) REV
Date: February 4, 1998	Sheet 35 of 41



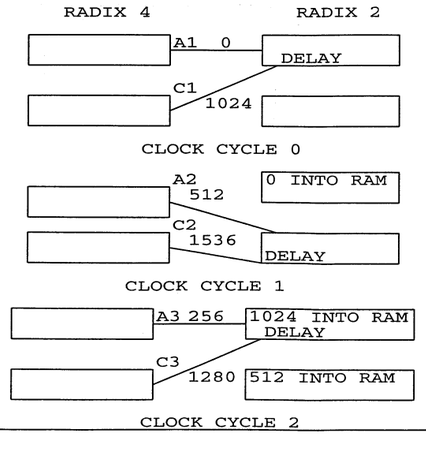
ALL POINT INDICES AFTER STAGE 0 REFER TO THE "IN PLACE" INDEX.

INDICES SHOWN AT STAGE 0 ARE THE TIME ORDERED INDEX.

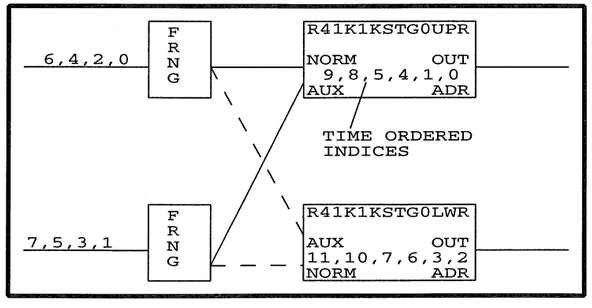
THE TIME ORDERED POINTS MUST BE PRESENTED EVENLY SPACED TO THE FRINGE DE-ROTATORS.

THE POINTS MUST THEN BE SHUFFLED TO GET THE CORRECT SEQUENCES OF POINTS INTO EACH PIPELINE.

THE REQUIRED SEQUENCES OF POINTS INTO EACH PIPELINE MAY BE OBSERVED IN LISTINGS OF THE SCRAMBLE SEQUENCE FOR A 2K FFT.



1K SEQUENCES AT INPUT



NOTE THE LOWER RADIX 2 STAGE IS DELAYED 1 CLOCK CYCLE. THIS CAN BE ACCOMPLISHED BY APPLYING THE RESET PULSE ONE CYCLE LATER, INTERNALLY. THE INPUT GOES INTO RAM. THE STAGGER WILL BE REMOVED ON READING THE RAM, USING THE EXTERNAL ADDRESS. THE EXTERNAL ADDRESS WITHDRAWS POINTS IN TIME ORDER FOR THE FSTC.

TOP PIPELINE (# 0)			BOT PIPELINE (# 3)			
"REAL" TIME INDEX	TIME INDEX ENTERING CHIP	"2K" RAM INDEX	"REAL" TIME INDEX	TIME INDEX ENTERING CHIP	"2K" RAM INDEX	"2K" RAM INDEX MINUS 1536
0	0	0	5	0	1536	0
2	1	256	7	1	1792	256
8	2	64	13	2	1600	64
10	3	320	15	3	1856	320
16	4	128	21	4	1664	128
18	5	384	23	5	1920	384
24	6	192	29	6	1728	192
26	7	448	31	7	1984	448
32	8	16	37	8	1552	16
34	9	272	39	9	1808	272
40	10	80	45	10	1616	80
42	11	336	47	11	1872	336

THE TABLE ABOVE WAS USED TO DETERMINE THAT THE SCRAMBLE SEQUENCE FOR EACH PIPELINE IS THE SAME AS FOR A 512 POINT FFT.

THE SEQUENCES WERE TAKEN FROM A LISTING OF THE SCRAMBLE SEQUENCE FOR A 2K FFT.

VLBA CORRELATOR PROJECT

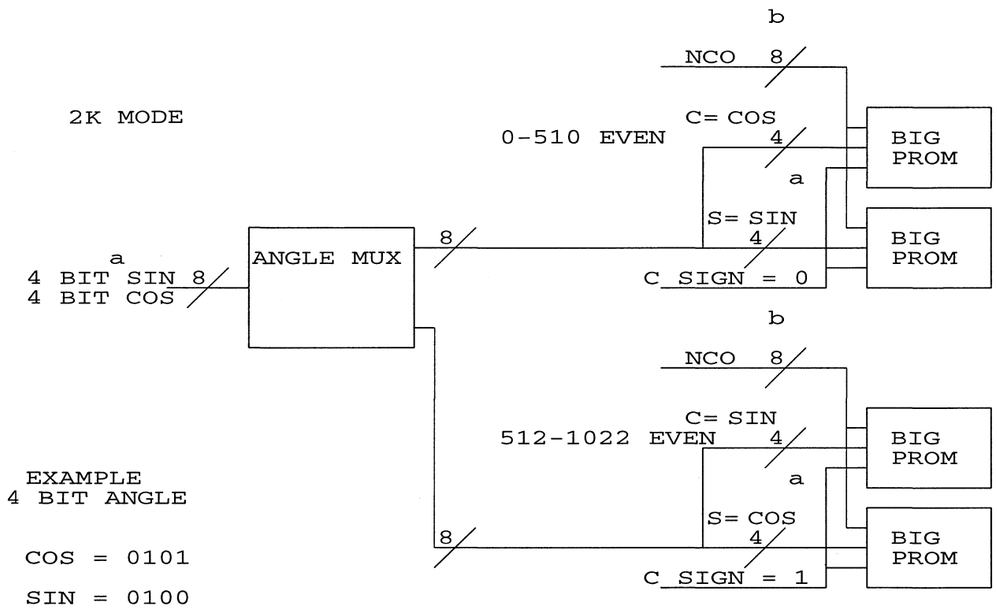
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: 1024 AND 2048 POINT FFT

Size	Document Number	REV
B	56000L002 (L002D36.SCH)	

Date: February 4, 1998 Sheet 36 of 41

SIGN MAGNITUDE ANGLES



EXAMPLE
4 BIT ANGLE

COS = 0101

SIN = 0100

WANT a + 90 DEGREES

C SIGN AS MSB ADDS 90 DEGREES

EXAMPLE
C=00101

PIPELINE A

-j(a+b)
e
TO ASIC TWID S=00100

C=10100

PIPELINE C

S=10101

1 IN MSB IS 90 DEGREES ADDED

4 BITS IN TRANSLATES TO 256 ANGLES IN
THIS IS TAKEN CARE OF BY ANGLE TABLES.
THESE INTERPOLATE TO GIVE MORE LSB'S.
EXAMPLE:
ACTUAL ANGLE DESIRED IS 01000010
HAVE 1 TABLE WITH 0101, FOR
EVERY 7 WITH 0100.

THUS, WHENEVER THE DATA IS SWAPED IN ONE DIRECTION
IN PIPELINE A, IT WILL BE SWAPPED IN THE OPPOSITE DIRECTION
IN PIPELINE C.

HAVE LINEARLY INTERPOLATED ANGLE. | ROM | SIN AND COSINE OF ANGLE

NCO OUTPUT ANGLE

ROM ADDS THE 2 ANGLES TOGETHER,
THEN TAKES THE SIN OR COS OF THE SUM.

QUESTION:
IS IT VALID USING ANGLE TABLES FOR INTERPOLATION,
WHEN THERE ARE DIFFERENT NCO OUTPUTS ADDED IN EACH TIME?
OR
WHEN WE ADD AN 8 BIT NCO OUTPUT, AND A 4BIT ANGLE, EXPANDED
BY ANGLE TABLES, ARE WE REALLY MAINTAINING 8 BITS PRECISION?

I'D GUESS NO, SINCE THE NCO OUTPUT IS DIFFERENT EACH
ITERATION OF THE ANGLE TABLE.

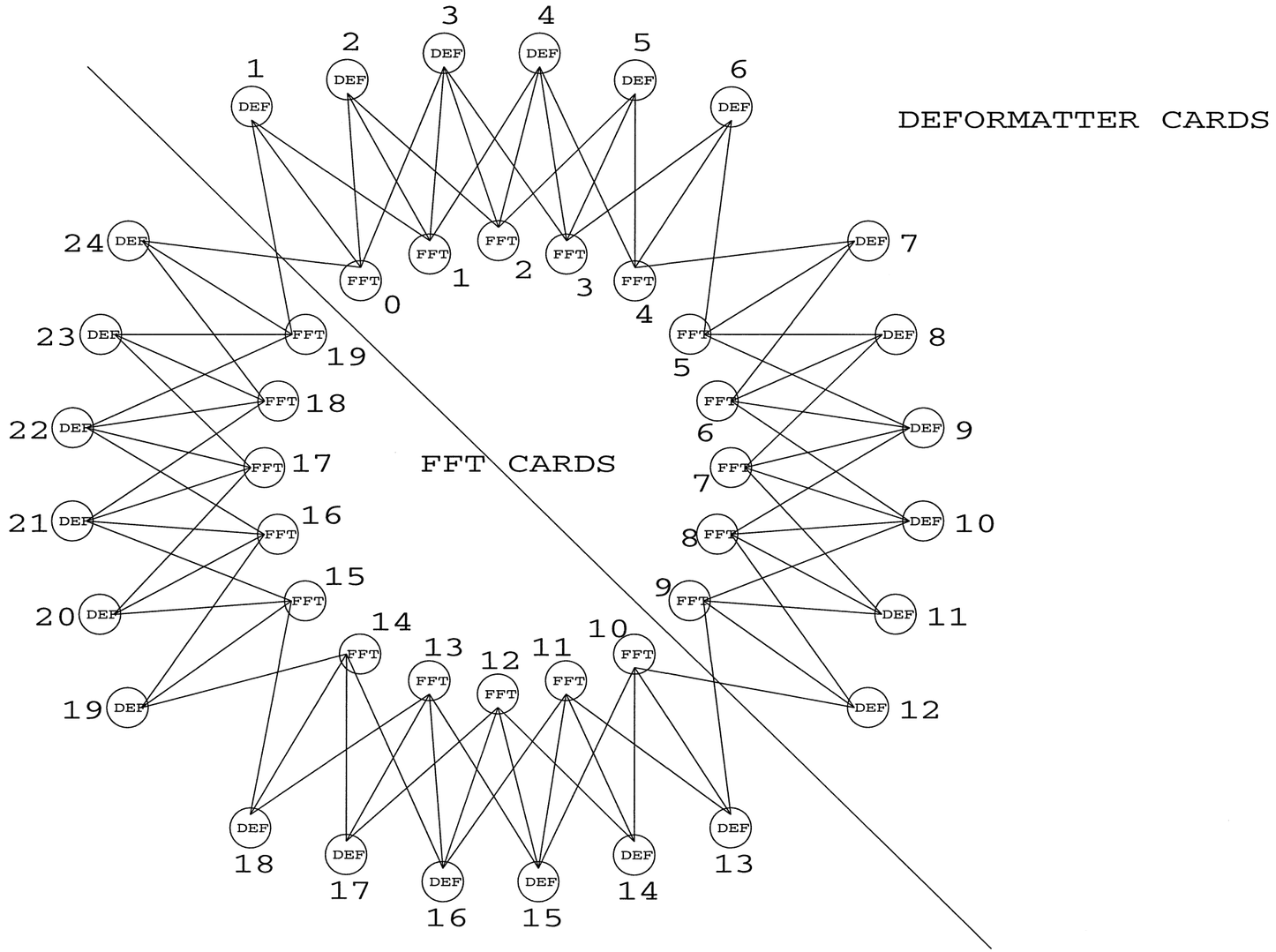
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
BIG ROM ANGLE PATHS

Size	Document Number	REV
A	56000L002 (L002D37.SCH)	

Date: May 6, 1997 Sheet 37 of 41



in m:/rackwire/1025

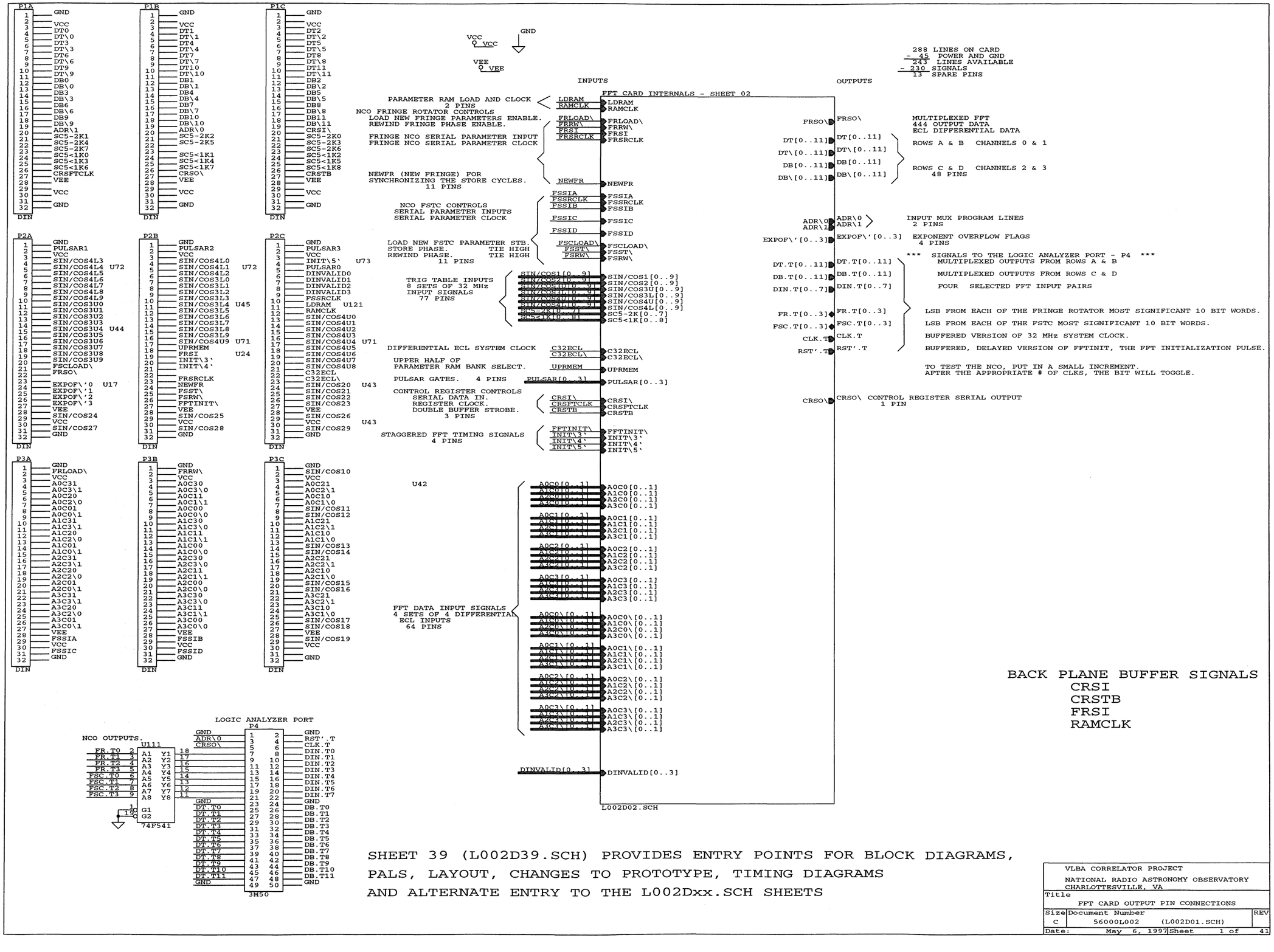
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title

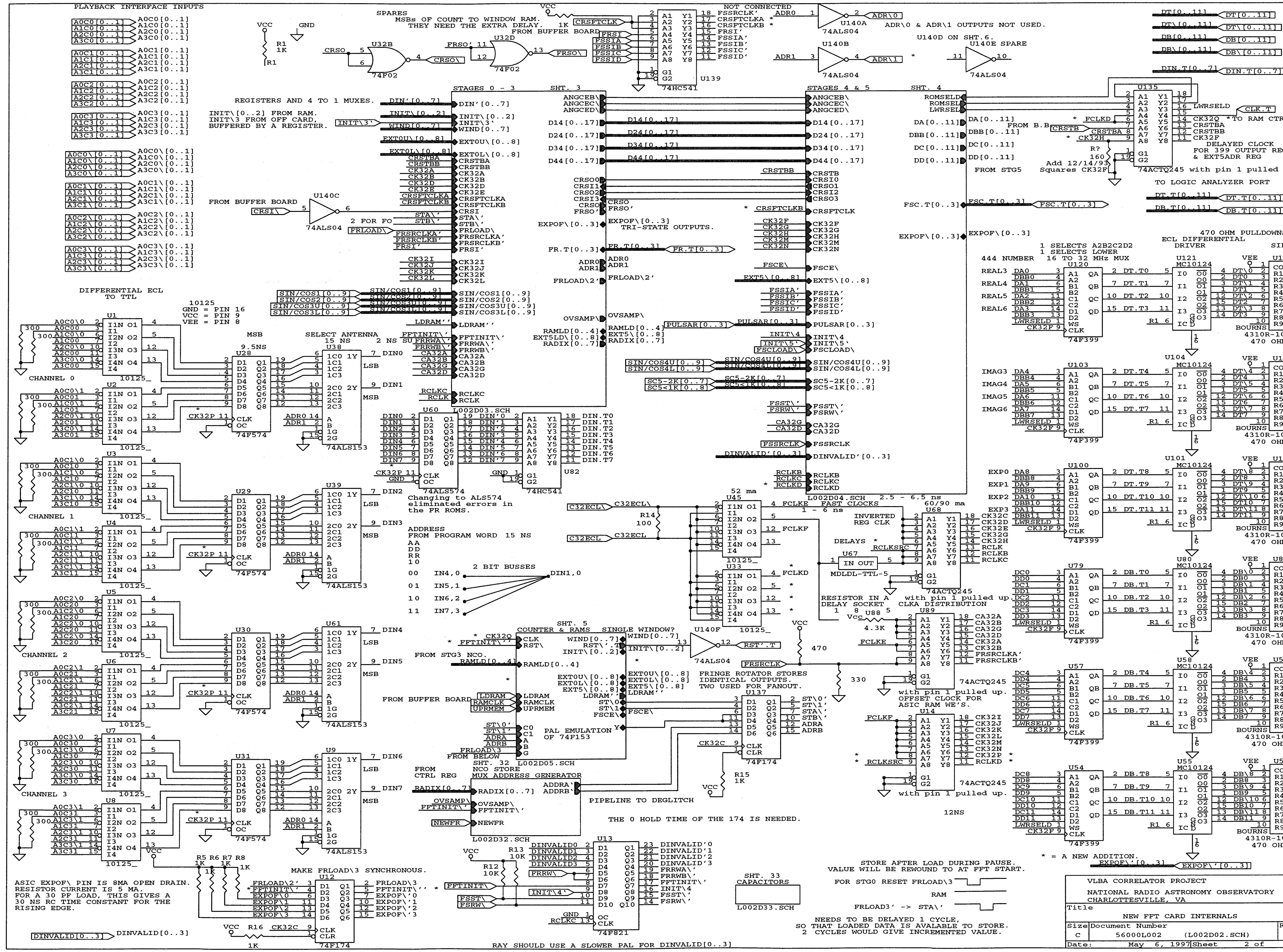
FAMOUS STAR DRAWING

Size	Document Number	REV
B	56000L025 (L025D26.SCH)	
Date: November 7, 1997	Sheet 26 of	



SHEET 39 (L002D39.SCH) PROVIDES ENTRY POINTS FOR BLOCK DIAGRAMS, PALS, LAYOUT, CHANGES TO PROTOTYPE, TIMING DIAGRAMS AND ALTERNATE ENTRY TO THE L002Dxx.SCH SHEETS

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: FFT CARD OUTPUT PIN CONNECTIONS		
Size: C	Document Number: 56000L002 (L002D01.SCH)	REV
Date: May 6, 1997	Sheet 1 of 41	


PLAYBACK INTERFACE INPUTS
SPARES
MSBs OF COUNT TO WINDOW RAM.
THEY NEED THE EXTRA DELAY.
FROM BUFFER BOARD
NOT CONNECTED
ADR\0 & ADR\1 OUTPUTS NOT USED.
U140D ON SHT.6.
U140E SPARE
REGISTERS AND 4 TO 1 MUXES.
INIT\[0..2] FROM RAM.
INIT\3 FROM OFF CARD,
BUFFERED BY A REGISTER.
STAGES 0 - 3 SHT. 3
STAGES 4 & 5 SHT. 4
FROM B.B.
DELAYED CLOCK
FOR 399 OUTPUT REG
& EXT5ADR REG
Add 12/14/93
Squares CK32F
FROM STG5
74ACTQ245 with pin 1 pulled up.
TO LOGIC ANALYZER PORT
EXPOF\[0..3]
TRI-STATE OUTPUTS.
470 OHM PULLDOWNS
ECL DIFFERENTIAL DRIVER
SIP
1 SELECTS A2B2C2D2
1 SELECTS LOWER
444 NUMBER 16 TO 32 MHz MUX
DIFFERENTIAL ECL TO TTL
10125
GND = PIN 16
VCC = PIN 9
VEE = PIN 8
MSB
9.5NS
SELECT ANTENNA
15 NS
2 NS
LSB
CHANNEL 0
CHANNEL 1
CHANNEL 2
CHANNEL 3
Changing to ALS574
eliminated errors in
the FR ROMS.
ADDRESS
FROM PROGRAM WORD 15 NS
2 BIT BUSSES
52 ma
FAST CLOCKS
1 - 6 ns
2.5 - 6.5 ns
60/90 ma
INVERTED
REG CLK
DELAYS
RESISTOR IN A
DELAY SOCKET
CLKA DISTRIBUTION
SHT. 5
COUNTER & RAMS SINGLE WINDOW?
FROM STG3 NCO.
FRINGE ROTATOR STORES
IDENTICAL OUTPUTS.
TWO USED FOR FANOUT.
with pin 1 pulled up.
OFFSET CLOCK FOR
ASIC RAM WE'S.
FROM BUFFER BOARD
PAL EMULATION
OF 74F153
FROM BELOW
SHT. 32 L002D05.SCH
NCO STORE
MUX ADDRESS GENERATOR
FROM CTRL REG
PIPELINE TO DEGLITCH
THE 0 HOLD TIME OF THE 174 IS NEEDED.
12NS
* = A NEW ADDITION.
MAKE FRLOAD\3 SYNCHRONOUS.
ASIC EXPOF\ PIN IS 8MA OPEN DRAIN.
RESISTOR CURRENT IS 5 MA.
FOR A 30 PF LOAD, THIS GIVES A
30 NS RC TIME CONSTANT FOR THE
RISING EDGE.
SHT. 33
CAPACITORS
L002D33.SCH
STORE AFTER LOAD DURING PAUSE.
VALUE WILL BE REWOUND TO AT FFT START.
FOR STG0 RESET FRLOAD\3
RAM
FRLOAD3' -> STA\'
NEEDS TO BE DELAYED 1 CYCLE,
SO THAT LOADED DATA IS AVALABLE TO STORE.
2 CYCLES WOULD GIVE INCREMENTED VALUE.
RAY SHOULD USE A SLOWER PAL FOR DINVALID[0..3]
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title
NEW FFT CARD INTERNALS
Size C
Document Number 56000L002 (L002D02.SCH)
REV
Date: May 6, 1997
Sheet 2 of 41

FRINGE ROTATOR REWIND GOES OFF THE CARD, FOR POSSIBLE USE IN MARK III MODE.
NOTE NCO'S SWAPPED IN STAGES 0 & 1.
CONTROL WORD DESCRIBED IN CTRLWRD.TXT.

ST LINES STORE THE ACCUMULATOR IN THE THE EXTRA NCO REG.
RW LINES REWIND THE ACCUMULATOR BACK TO THE STORED VALUE.

CARD CONTROL WORD SCATTERED AMONG ASIC CRBIT'S.

SEPARATE FR RW LINE ALLOWS THERE TO BE NO RW WHEN THERE IS A NCO LOAD.

FOR STAGES 1,2,3, SHEETS 9, 18-28 ARE IDENTICAL, EXCEPT FOR THE U NUMBERS.

NCO FRINGE STORE COUNT RADIX FOR OVERLAPPING. FROM CONTROL BITS.

NCOPRZ DISABLES THE NCO CLOCK FOR RAM LOADING.

STG3 R2CNT0 IN PHASE WITH STG5.

FRINGE ROTATOR ROMS

2K X 8 ROMS
24 PIN
$15 - PC, $19 - WC
6WKS. DEL
100 QUAN.
COULD NOT USE AMD 63RS1681 OR FUJITSU MB7238RA-20
20 NS ACCESS, 40 NS SU!

DELAYED CLOCK FOR REGISTERS THAT OUTPUT TO ASICS.

TO GENERATE STORE

DELAY NCO LOAD PULSES. STAGGERED 2 CYCLES.

FRINGE ROTATOR SHIFT REGISTER CLOCKS

VLBA CORRELATOR PROJECT	
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA	
Title	FFT STAGES 0 TO 3
Size C	Document Number 56000L002 (L002D03.SCH) REV
Date: May 6, 1997	Sheet 3 of 41

FSC ROMS INCLUDED IN STAGE 4 ASIC SHEETS.
SHTS. 10-13 IDENTICAL, EXCEPT FOR U NUMBERS.

SHTS. 14, 29-31 IDENTICAL,
EXCEPT FOR U NUMBERS.

CK32F CK32G CK32H CK32M CK32N

CRSFTCLK

CRSI0 CRSTB D14[0..17]

ASIC - STAGE 4A U113

CRSI CRSFTCLK CRSTB NDATAIN[0..17]

AUXIN[0..17] TWID[0..9] NCOSTA\ NCORW\ CLK RST\ NCOSI CLKA NCOLDIN\ NCOCE\ NCOSRCLK SIN/COS[0..8] DINVALID

CRSO DATAOUT[0..17] D15[0..17]

COSA[0..4] SINA[0..4] COSB[0..4] SINB[0..4]

EXPOF\0 FSC.T0 NCOSO NCOCI R2CNT0 R2CNTA

L002D10.SCH

D24[0..17] SC4U'[0..9] FSST\' FSRW\' CK32G INIT\4 CA32G FSSIA' FSCEA\ FSSRCLKA ANGA[0..8] DINVALID'0

CA32G CA32D RCLKB RCLKC

CRSO1

ASIC - STAGE 4B U91

PULSAR[0..3] INIT\4 D24[0..17] FSRW\' FSST\' DINVALID'[0..3]

DINVALID ALLOWS SETTING THE FFT DATA INVALID IF THERE WAS A TAPE ERROR. SET THE PGENBL BIT IN THE STAGE 4 CONTROL WORDS.

CRSO CRSFTCLK CRSTB NDATAIN[0..17]

AUXIN[0..17] TWID[0..9] NCOSTA\ NCORW\ CLK RST\ NCOSI CLKA NCOLDIN\ NCOCE\ NCOSRCLK SIN/COS[0..8] DINVALID

CRSI DATAOUT[0..17] D25[0..17]

BCOSA[0..4] BSINA[0..4] BCOSB[0..4] BSINB[0..4]

EXPOF\1 FSC.T1 NCOSO NCOCI R2CNTB

L002D11.SCH

D14[0..17] SC4U'[0..9] FSST\' FSRW\' CK32G INIT\4 FSSIB' FSCEA\ FSSRCLKA ANGB[0..8] DINVALID'1

CRSI2

ASIC - STAGE 4C U70

D34[0..17] EXT5\[0..8] SEE EXT5.TIM

CRSI CRSFTCLK CRSTB NDATAIN[0..17]

AUXIN[0..17] TWID[0..9] NCOSTA\ NCORW\ CLK RST\ NCOSI CLKA NCOLDIN\ NCOSRCLK NCOCE\ SIN/COS[0..8] DINVALID

CRSO DATAOUT[0..17] D35[0..17]

COSA[0..4] SINA[0..4] COSB[0..4] SINB[0..4]

EXPOF\2 FSC.T2 NCOSO NCOCI R2CNTC

L002D12.SCH

D44[0..17] SC4U'[0..9] FSST\' FSRW\' CK32M INIT\4 FSSIC' CA32D FSSRCLKB FSCEA\ ANGC[0..8] DINVALID'2

CRSO3

ASIC - STAGE 4D U47

D44[0..17] NEED AN F FOR THE 4 NS SU.

CRSI DATAOUT[0..17] D45[0..17]

DCOSA[0..4] DSINA[0..4] DCOSB[0..4] DSINB[0..4]

EXPOF\3 FSC.T3 NCOSO NCOCI R2CNTD SIZE\1 CRBIT

TO MUX

L002D13.SCH

D34[0..17] SC4U'[0..9] FSST\' FSRW\' CK32M INIT\4 FSSID' CA32D FSCLOAD\'' FSSRCLKB FSCEA\ ANGD[0..8] DINVALID'3

* WAS FROM FSCLOAD\'''

EXTERNAL ADDRESS 5 IS LOADED INTO RAM FROM NCO 3A. THE REGISTER BREAKS UP THE LONG PATH AND PROVIDES FANOUT TO THE 4 ASICS.

ASIC - STAGE 5A U119

CRSI CRSFTCLK CRSTB DATAOUT[0..11]

NDATAIN[0..17] AUXIN[0..17] CRSTB TWID[0..9] CLKA EXTADD\[0..8] CLK INIT\5 NCOSI NCOCO NCOLDIN\ NCOSTA\ NCORW\ NCOCE\ NCOSRCLK DATAENBL\

DA[0..11] EXPOF\ R2CNT0 CRBIT CRSO

D45[0..17] SCD[0..9] CA32D EXT5\'[0..8] CK32H

FSST\' FSRW\' FSCE\ FSSRCLKC PGA

L002D14.SCH

EXPOF\[0..3] FSC.T[0..3]

EXPOF\0 1 SELECTS X2 FROM STG4

FSCONLY\ LWRSEL

CLK FROM STG4 R2CNT0

3 MA LOAD TO FSTC ROM MUX

ASIC - STAGE 5B U99

CRSI CRSFTCLK CRSTB DATAOUT[0..11]

NDATAIN[0..17] AUXIN[0..17] TWID[0..9] CLKA EXTADD\[0..8] CLK RST\ NCOSI NCOCO NCOLDIN\ NCOSTA\ NCORW\ NCOCE\ NCOSRCLK DATAENBL\

DBB[0..11] EXPOF\ R2CNT0

D25[0..17] SCB[0..9] CA32G EXT5\'[0..8] CK32H INIT\5

FSST\' FSRW\' FSCE\ FSSRCLKC PGB

L002D29.SCH

DBB[0..11]

EXPOF\1

ROMSEL ROMSELD THRU 2 U135, 541 SECTIONS.

ASIC - STAGE 5C U78

CRSI CRSFTCLK CRSTB DATAOUT[0..11]

NDATAIN[0..17] AUXIN[0..17] TWID[0..9] CLKA EXTADD\[0..8] CLK RST\ NCOSI NCOCO NCOLDIN\ NCOSTA\ NCORW\ NCOCE\ NCOSRCLK DATAENBL\

DC[0..11] EXPOF\ CRSO

D35[0..17] SCC[0..9] CA32D EXT5\'[0..8] CK32N INIT\5

FSST\' FSRW\' FSCE\ FSSRCLKD PGC

L002D30.SCH

DC[0..11]

1 SELECTS DD

EXPOF\2

ASIC - STAGE 5D U53

CRSI CRSFTCLK CRSTB DATAOUT[0..11]

NDATAIN[0..17] AUXIN[0..17] TWID[0..9] CLKA EXTADD\[0..8] CLK RST\ NCOSI NCOCO NCOLDIN\ NCOSTA\ NCORW\ NCOCE\ NCOSRCLK DATAENBL\

DD[0..11] EXPOF\ FSCONLY\ LWRSEL

D45[0..17] SCD[0..9] CA32D EXT5\'[0..8] CK32N INIT\5

FSST\' FSRW\' FSCE\ FSSRCLKD PGD

L002D31.SCH

DD[0..11]

EXPOF\3

CAN BE SLOWER REG.

ALL STG5 R2CNT0'S ARE IN PHASE. LWR'S ARE DELAYED 1 CYCLE BY DELAYING INIT. R4CNT0 IS USED TO THEN CORRECT THE PHASE OF R2CNT\0. SINCE THERE IS AN 11 CLOCK DELAY / STAGE, STAGE 3 R2CNT0 IS IN PHASE WITH STG5.

MUX FSC ROM OUTPUTS. 4.5NS SU U118

WS 10NS SU

1 SELECTS A2B2C2D2
1 SELECTS SMALL ROM.

BIG ROM REG U134

ACOSA0 ACOSA1 ACOSA2 ACOSA3 ASINA0 ASINA1 ASINA2 R2CNTA FSCONLY\ → 74P273

ACOSB0 ACOSB1 ACOSB2 ACOSB3 ROMSELD_1 RCLKB_9 → 74F399 → SCA0 SCA1 SCA2 SCA3

U98

ACOSB4 ASINB0 ASINB1 ASINB2 ROMSELD_1 RCLKB_9 → 74F399 → SCA4 SCA5 SCA6 SCA7

A & B SHARE THIS CHIP.

U97

ASINB3 ASINB4 BCOSB0 BCOSB1 ROMSELD_1 RCLKB_9 → 74F399 → SCA8 SCA9 SCB0 SCB1

U133

ASINA3 ASINA4 BCOSA0 BCOSA1 BCOSA2 BCOSA3 BCOSA4 BSINA0 R2CNTB FSCONLY\ → 74P273

U96

BCOSB2 BCOSB3 BCOSB4 BSINB0 ROMSELD_1 RCLKB_9 → 74F399 → SCB2 SCB3 SCB4 SCB5

U95

BSINB1 BSINB2 BSINB3 BSINB4 ROMSELD_1 RCLKB_9 → 74F399 → SCB6 SCB7 SCB8 SCB9

U92

BSINA1 BSINA2 BSINA3 BSINA4 CCOSA0 CCOSA1 CCOSA2 CCOSA3 R2CNTC FSCONLY\ → 74P273

U94

CCOSB0 CCOSB1 CCOSB2 CCOSB3 ROMSELD_1 RCLKB_9 → 74F399 → SCC0 SCC1 SCC2 SCC3

U93

CCOSB4 CSINB0 CSINB1 CSINB2 ROMSELD_1 RCLKB_9 → 74F399 → SCC4 SCC5 SCC6 SCC7

U76

CCOSA4 CSINA0 CSINA1 CSINA2 CSINA3 CSINA4 DCOSA0 DCOSA1 R2CNTC FSCONLY\ → 74P273

U77

CSINB3 CSINB4 DCOSB0 DCOSB1 ROMSELD_1 RCLKB_9 → 74F399 → SCC8 SCC9 SCD0 SCD1

U75

DCOSB2 DCOSB3 DCOSB4 DSINB0 ROMSELD_1 RCLKB_9 → 74F399 → SCD2 SCD3 SCD4 SCD5

U35

DCOSA2 DCOSA3 DCOSA4 DSINA0 DSINA1 DSINA2 DSINA3 DSINA4 R2CNTD FSCONLY\ → 74P273

U52

DSINB1 DSINB2 DSINB3 DSINB4 ROMSELD_1 RCLKB_9 → 74F399 → SCD6 SCD7 SCD8 SCD9

THE PIGGYBACK BUFFER GETS RID OF RINGING IN FSSRCLK.

U20 PIGGYBACK 74HC541

FSSRCLK → FSSRCLKA FSSRCLKB FSSRCLKC FSSRCLKD

U20 74F574

PULSAR0 PULSAR1 PULSAR2 PULSAR3 → PGA PGB PGC PGD

FSCLOAD\ FSCLOAD\' STG 5 FSCLOAD\'' STG 4

INIT\5' → INIT\5

RCLKC → OC

FSCLOAD\ LOADS STAGGERED BY 1 CYCLE. SEE TIMING IN CETIM.SCH

FSST\ (FSTC STORE\) AND FSRW\ ARE OUTPUT OFF CARD JUST IN CASE NEEDED. NORMALLY TIE PINS HIGH.

SIN/COS4U[0..9] SIN/COS4L[0..9]

U18 74F821 → SC4U'0 SC4U'1 SC4U'2 SC4U'3 SC4U'4 SC4U'5 SC4U'7 SC4U'8 SC4U'9

U19 74F821 → SC4L'0 SC4L'1 SC4L'2 SC4L'3 SC4L'4 SC4L'5 SC4L'6 SC4L'7 SC4L'8 SC4L'9

2048 PT ANGLES
128/512 PT ANGLES

SHT 6 WITH SHT 7 INSIDE IT. TO FSTC ROMS

ANGLE MUX L002D06.SCH

SC5-2K[0..7] SC5<1K[0..8] RCLKD → CLK

FROM R2CNT0 3B 3C 3D → ANGCEB\ ANGCEC\ ANGCED\

ANGA[0..8] ANGB[0..8] ANGC[0..8] ANGD[0..8]

FROM CONTROL WORD 4D SIZE\1

VCC R17 1K R1

EXT5\[0..8]

SEE EXT5.TIM

U143 74F174

EXT5\0 EXT5\1 EXT5\2 EXT5\3 EXT5\4 EXT5\5 → EXT5\'0 EXT5\'1 EXT5\'2 EXT5\'3 EXT5\'4 EXT5\'5

CK32F R1 → CLK CLR

U142 74F174

EXT5\6 EXT5\7 EXT5\8 FSCE\ → EXT5\'6 EXT5\'7 EXT5\'8 FSCE\ FSCEA\

CK32F R1 → CLK CLR

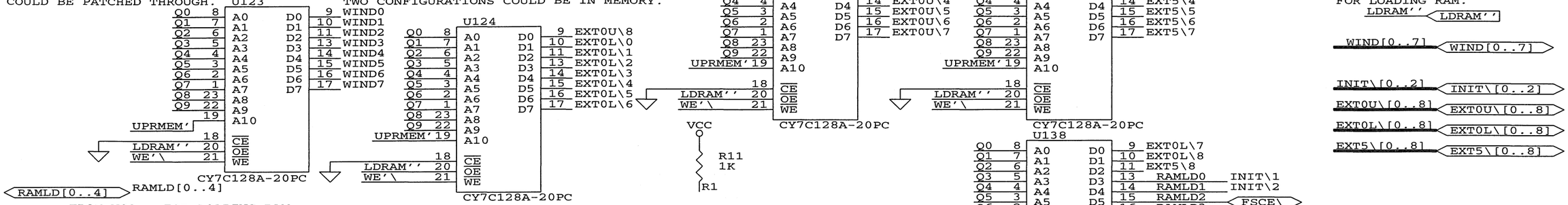
VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA			
Title FFT STAGES 4 & 5			
Size C	Document Number 56000L002 (L002D04.SCH)		REV
Date: May 6, 1997	Sheet 4 of 41		

PERFORMANCE P4C116-15PC $22.32, 280 QUAN, 12-15WKS 300 MIL, 24 PIN
CY7C128-20PC, 100 QUAN, $9 1WK

ADDR PINOUT SCRAMBLED.

FOR OVERLAP MODE 2 FRST SCHEDULES ARE NEEDED. UPRMEM ALLOWS AN ALTERNATE SCHEDULE. NOTE THE REST OF THE RAM VALUES WOULD HAVE TO BE DUPLICATED. TWO CONFIGURATIONS COULD BE IN MEMORY.

*
ELIMINATED 541, U136
COULD BE PATCHED THROUGH.



FROM NCO. FOR LOADING RAM.

DELAY SO ENOUGH HOLD TIME TO TWIDDLE
 SEE DRAMTWID.TIM
SEE RAMEXTA.TIM FOR RAM TO EXTERNAL ADDRESS TIMING
SEE RAMFSCE.TIM FOR RAM TO FSCE TIMING.
SEE ST.TIM FOR RAM TO REG FOR STORE TIMING.

HAVE INIT\3, 4, AND 5 SYSTEM WIDE CARD INPUTS

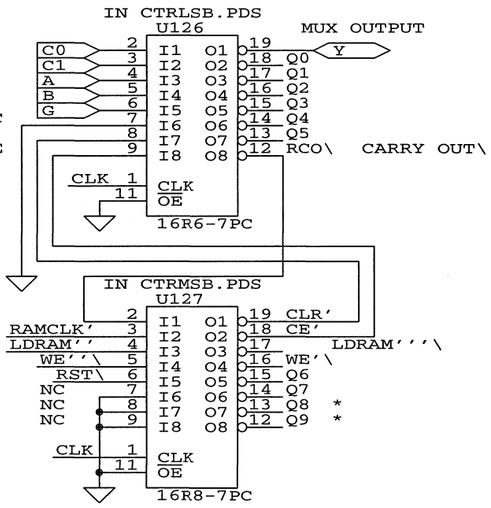
LOW SPEED.
TO ENABLE NCO OUTPUTS
FOR LOADING RAM.

SEE L002D34.SCH FOR A DESCRIPTION OF BOTH PALS.

6.5 NS CLK TO OUTPUT
10 BIT COUNTER
IN CTRLSB.PDS

HALF OF PAL EMULATES A 74F153
C2 & C3 ASSUMED LOGIC 1
G INSTEAD OF G\

Y=G*/B*/A*C0 +
G*/B*A*C1 +
G*B*/A +
G*B*A

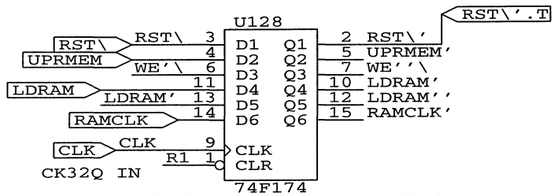


Q8 & Q9 TO BE DELAYED FOR WINDOW RAM.

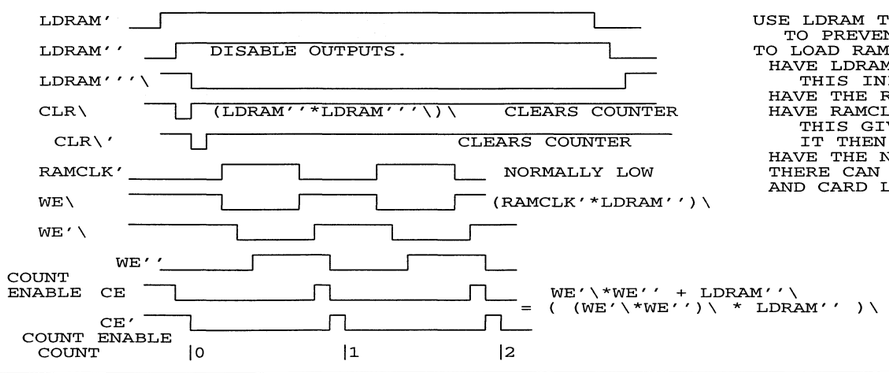
CLEAR COUNT ENABLE CLR': = RST + LDRAM''*LDRAM'''\
CE' := (LDRAM'' * (WE'*WE'')\ )\

LOAD RAM WITH ALL 1'S EXCEPT 0'S AT:
 INIT\1 = PT 8
 INIT\2 = PT 19 11 SPACING
 INIT\3 = PT 30
 INIT\4 = PT 41
 INIT\5 = PT 52

10 NS



ALSO TO U140 11, INVERTER TO TEST CONN.



USE LDRAM TO DISABLE OUTPUT WHEN SHIFTING ASIC CTRL WORD
 TO PREVENT BUS CONTENTION FROM NCO OUTPUTS.
TO LOAD RAMS,
 HAVE LDRAM HIGH.
  THIS INITIALLY CLEARS THE COUNTER.
 HAVE THE RAM WIDE WORD OUTPUT VIA THE NCO'S.
 HAVE RAMCLK GIVE A NEGATIVE PULSE.
  THIS GIVES THE WE\
  IT THEN INCREMENTS THE COUNTER.
 HAVE THE NCO'S OUTPUT THE NEXT WORD.
 THERE CAN BE A SINGLE SYSTEM WIDE RAMCLK SIGNAL,
 AND CARD LEVEL LDRAMS.

ENABLED ALL THE TIME WHEN NOT LOADING RAM.

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
COUNTER, WINDOW RAMS, INIT RAM

Size	Document Number	REV
B	56000L002 (L002D05.SCH)	
Date: May 6, 1997	Sheet 5 of 41	

2048 EVEN AND ODD
SC5-2K[0..7] 2K[0..7]
128 UPPER AND 512 LOWER
SC5<1K[0..8] <1K[0..8]
CLK CLK
RCLK INPUT

VCC
R9
1K
R1

REG D
128 OR 512 PTS OUT
U34
C0 2 C1 3 C2 4 C3 5 C4 6 C5 7 C6 8 C7 9 C8 10 CLK 13 ANGCED\ 14 SIZE1 1 R1 11
D1 Q1 D2 Q2 D3 Q3 D4 Q4 D5 Q5 D6 Q6 D7 Q7 D8 Q8 D9 Q9 CLK CLKEN OC CLR
23 ANGA0 22 ANGA1 21 ANGA2 20 ANGA3 19 ANGA4 18 ANGA5 17 ANGA6 16 ANGA7 15 ANGA8
74F823

WIRE ORED TOGETHER
11 NS
6NS SU

REG Y
2K PTS OUT
U24
COS0 2 COS1 3 COS2 4 COS3 5 6 SIN0 7 SIN1 8 SIN2 9 SIN3 10 CLK 13 ANGCED\ 14 SIZE\1 1 R1 11
D1 Q1 D2 Q2 D3 Q3 D4 Q4 D5 Q5 D6 Q6 D7 Q7 D8 Q8 D9 Q9 CLK CLKEN OC CLR
23 ANGA0 R0 COS0
22 ANGA1 R1
21 ANGA2 R2
20 ANGA3 R3 COS3
19 ANGA4 R4 COS SIGN
18 ANGA5 R0 SIN0
17 ANGA6 R1
16 ANGA7 R2
15 ANGA8 R3 SIN3
74F823

SIGN MAGNITUDE ANGLES
ANGA[0..8] ANGA[0..8]
ANGB[0..8] ANGB[0..8]
0-510 EVEN
ANGC[0..8] ANGC[0..8]
ANGD[0..8] ANGD[0..8]

THE ORIGINAL SINES AND COSINES TO THE FSTC ROMS
HAVE BEEN REPLACED WITH A FIVE BIT ANGLE INDEX.
THE FOUR LSB'S ARE SENT TWICE.
THE MSB IS SENT ONCE.
THE MSB REPRESENTS 90 DEGREES.
THE BUS IS SHOWN AS R[0..4].

FROM 4D
SIZE\1 SIZE\1 9 U140D 8 SIZE1
74ALS04 USED TO BE AN F
INVERTER PREVENTS BUS CONTENTION.

U22
C0 2 C1 3 C2 4 C3 5 C4 6 C5 7 C6 8 C7 9 C8 10 CLK 13 ANGCED\ 14 SIZE1 1 R1 11
D1 Q1 D2 Q2 D3 Q3 D4 Q4 D5 Q5 D6 Q6 D7 Q7 D8 Q8 D9 Q9 CLK CLKEN OC CLR
23 ANGB0 22 ANGB1 21 ANGB2 20 ANGB3 19 ANGB4 18 ANGB5 17 ANGB6 16 ANGB7 15 ANGB8
74F823

U27
COS'0 2 COS'1 3 COS'2 4 COS'3 5 6 SIN'0 7 SIN'1 8 SIN'2 9 SIN'3 10 CLK 13 ANGCEB\ 14 SIZE\1 1 R1 11
D1 Q1 D2 Q2 D3 Q3 D4 Q4 D5 Q5 D6 Q6 D7 Q7 D8 Q8 D9 Q9 CLK CLKEN OC CLR
23 ANGB0 R0 COS0
22 ANGB1 R1
21 ANGB2 R2
20 ANGB3 R3 COS3
19 ANGB4 R4 COS SIGN
18 ANGB5 R0 SIN0
17 ANGB6 R1
16 ANGB7 R2
15 ANGB8 R3 SIN3
74F823

823 HAS 3NS SU
FROM 3D R2CNT0
ANGCED\ ANGCED\

THESE TWO ARE IDENTICAL,
USED FOR FANOUT.

FROM 3B R2CNT0
ANGCEB\ ANGCEB\

U36
C0 2 C1 3 C2 4 C3 5 C5 6 C6 7 C7 8 C8 9 SIZE1 1 19
A1 Y1 A2 Y2 A3 Y3 A4 Y4 A5 Y5 A6 Y6 A7 Y7 A8 Y8 G1 G2
18 17 16 15 14 13 12 11
74F541

U37
SIN0 2 SIN1 3 SIN2 4 SIN3 5 C4 6 COS0 7 COS1 8 COS2 9 COS3 10 CLK 13 ANGCEB\ 14 1 R1 11
D1 Q1 D2 Q2 D3 Q3 D4 Q4 D5 Q5 D6 Q6 D7 Q7 D8 Q8 D9 Q9 CLK CLKEN OC CLR
23 ANGC0 R0 COS0
22 ANGC1 R1
21 ANGC2 R2
20 ANGC3 R3 COS3
19 ANGC4 R4 COS SIGN
18 ANGC5 R0 SIN0
17 ANGC6 R1
16 ANGC7 R2
15 ANGC8 R3 SIN3
74F823
C4 HELD HIGH BY BELOW PU.

512 - 1022 EVEN
90 TO 180 DEGREES
R4 = 1

REG C
U21
<1K0 2 <1K1 3 <1K2 4 <1K3 5 <1K4 6 <1K5 7 <1K6 8 <1K7 9 <1K8 10 CLK 13 14 SIZE1 1 R1 11
D1 Q1 D2 Q2 D3 Q3 D4 Q4 D5 Q5 D6 Q6 D7 Q7 D8 Q8 D9 Q9 CLK CLKEN OC CLR
23 C0 22 C1 21 C2 20 C3 19 C4 18 C5 17 C6 16 C7 15 C8
74F823

FROM 3C
R2CNT0
ANGCEC\
CLKEN
3NS SU
0NS HT
2NS DATA HT

MAKE R4=1 TO ADD 90 DEGREES
VCC
R10
2.2K
VCC
R18
820
ADDED UNDER BOARD TO FIX
ERRORS IN 128 PT MODE

U25
C0 SIN'0 2 C1 SIN'1 3 C2 SIN'2 4 C3 SIN'3 5 C4 6 C5 COS'0 7 C6 COS'1 8 C7 COS'2 9 C8 COS'3 10 CLK 13 ANGCEB\ 14 R1 11
D1 Q1 D2 Q2 D3 Q3 D4 Q4 D5 Q5 D6 Q6 D7 Q7 D8 Q8 D9 Q9 CLK CLKEN OC CLR
23 ANGD0 R0 COS0
22 ANGD1 R1
21 ANGD2 R2
20 ANGD3 R3 COS3
19 ANGD4 R4 COS SIGN
18 ANGD5 R0 SIN0
17 ANGD6 R1
16 ANGD7 R2
15 ANGD8 R3 SIN3
74F823

513 - 1023 ODD
C= -SIN'
S= +COS'

SHARE INPUTS OF LAST CHIP HERE.

2K EVEN/ODD IN REG W
U23
2K0 2 2K1 3 2K2 4 2K3 5 2K4 6 2K5 7 2K6 8 2K7 9 CLK 11 SIZE\1 1
D1 Q1 D2 Q2 D3 Q3 D4 Q4 D5 Q5 D6 Q6 D7 Q7 D8 Q8 CLK OC
19 18 17 16 15 14 13 12
74F574

ODD REG X
U26
COS0 2 COS1 3 COS2 4 COS3 5 SIN0 6 SIN1 7 SIN2 8 SIN3 9 CLK 11 SIZE\1 1
D1 Q1 D2 Q2 D3 Q3 D4 Q4 D5 Q5 D6 Q6 D7 Q7 D8 Q8 CLK OC
19 COS'0 18 COS'1 17 COS'2 16 COS'3 15 SIN'0 14 SIN'1 13 SIN'2 12 SIN'3
74F574

USE R2C0INV IN ASIC CONTROL WORDS.
THIS INVERTS THE PHASE OF THE R2CNT0,
16 MHz SIGNAL FOR THE ASIC.

```
 333
 DBC

 RRR
 222
 CCC
S000
IIII
ZNNN
EVVV
1
```

0110	512 PT RADIX 2	HAVE ANCCEC\ OUT OF PHASE WITH ANGCE\ TO REG D & Y.
0111	128 PT RADIX 2	HAVE ANGCEC\ IN PHASE WITH ANGCE\ TO REG D & Y.
1110	2048 PT RADIX 2	HAVE ANCCEC\ OUT OF PHASE WITH ANGCE\ TO REG D & Y.

SHT 7
BLK DIA & TIMING
L002D07.SCH

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title	MUX FSTC ANGLES	
Size B	Document Number 56000L002 (L002D06.SCH)	REV
Date: December 10, 1997	Sheet 6 of 41	

2048 RADIX 2 EVEN OR ODD SELECT

ANGCE = R2CNT0 FROM STG3 WITH R2C0INV = 0

ANGCE ANGCE\

2K DATA IN |O1 |E1 |O2 |E2 |O3 |E3 |

REG W |O1 |E1 |O2 |E2 |O3 |E3 |

EVEN REG Y |E1 |E2 |E3 ANGCE\

ODD REG X |O1 |E1 |O2 |E2 |O3 |E3 |

NOT USED

ODD REG Y |O1 |O2 |O3 ANGCE\

CE\

USE R2C0INV IN ASIC CONTROL WORDS.
THIS INVERTS THE PHASE OF THE R2CNT0, 16 MHz SIGNAL FOR THE ASIC.

128 OR 512 RADIX 2 LABEL 128 PTS A, 512 PTS B.

128/512 IN |A1 |B1 |A2 |B2 |

3C R2C0INV = 1 128 REG C |A1 |A2 ANGCE\

3C R2C0INV = 0 512 REG C |B1 |B2 ANGCE

128 REG D |A1 |A2 ANGCE\

512 REG D |B1 |B2 ANGCE\

ELIMINATE STAGGER.
NOTE A1,B1,O1, AND E1 ALL LINE UP.

* = 2K MODE REGISTERS
0 - 510 EVEN & 1 - 510 ODD
ARE DEMULTIPLEXED FROM DATA STREAM.
512 - 1022 EVEN AND 513 - 1023 ODD
ARE OBTAINED BY SWITCHING SIN AND COSINE
AND INVERTING SIN'S SIGN.

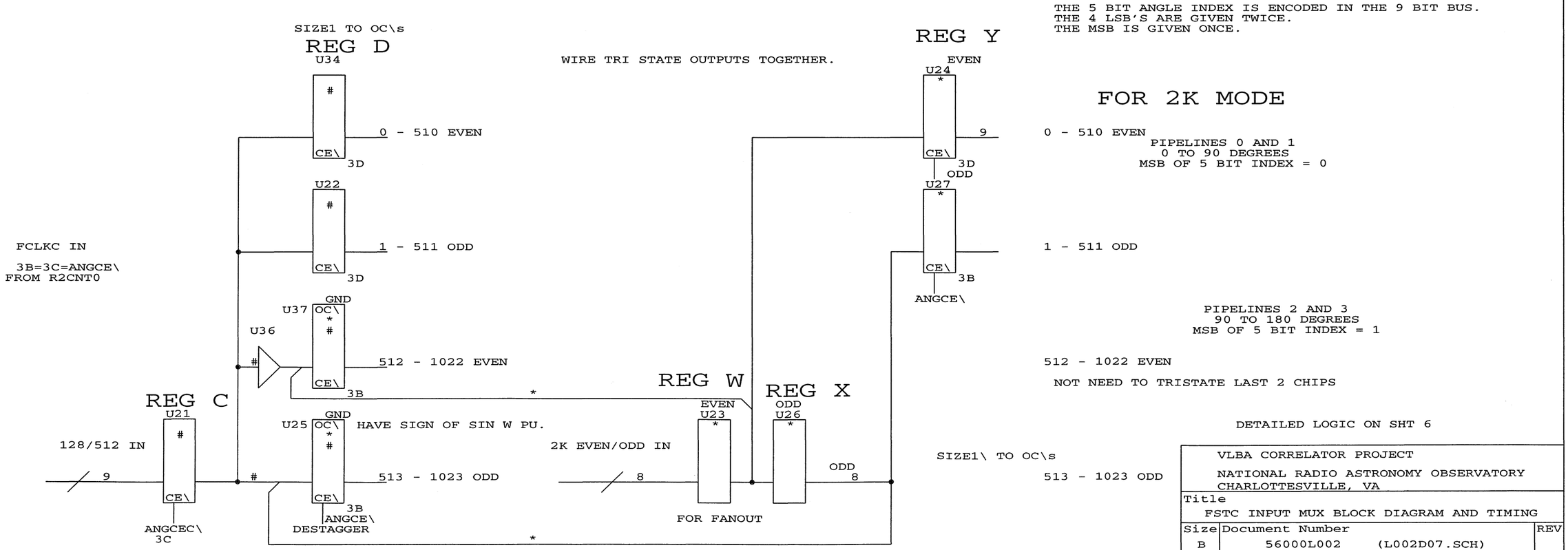
\# = 128 OR 512 POINT REGISTERS.
PHASE OF ANGCEC TO REG C
DETERMINES WHETHER 128 OR 512 IS CHOSEN.
REG D DESTAGGERS.

IN FSC ONLY MODE, THE OUTPUT OF THE BIG ROM IS ZEROED IN THE SUBSEQUENT 273 REGISTER. THUS, IT DOES NOT MATTER WHAT ANGLE COMES OUT OF THIS ANGLE MUX.

0110	512 PT RADIX 2	HAVE ANCCEC\ OUT OF PHASE WITH ANGCE\ TO REG D & Y.
0111	128 PT RADIX 2	HAVE ANGCEC\ IN PHASE WITH ANGCE\ TO REG D & Y.
1110	2048 PT RADIX 2	HAVE ANCCEC\ OUT OF PHASE WITH ANGCE\ TO REG D & Y.

AS823 CE, TRI-STATE REG

THE 5 BIT ANGLE INDEX IS ENCODED IN THE 9 BIT BUS.
THE 4 LSB'S ARE GIVEN TWICE.
THE MSB IS GIVEN ONCE.



VLBA CORRELATOR PROJECT		
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: FSTC INPUT MUX BLOCK DIAGRAM AND TIMING		
Size: B	Document Number: 56000L002 (L002D07.SCH)	REV:
Date: December 10, 1997	Sheet 7 of 41	

STAGE 0A

U106

CRSI N10 CRSI
CRSFTCLK L9 CRSFTCLK
CRSTB M10 CRSTB
CLK H13 CLK
B7 FCLK
WINDOW[0..7] A7 CLKA
RST\ J13 RST
WINDOW0 H3 TWID0
WINDOW1 J1 TWID1
WINDOW2 J2 TWID2
WINDOW3 K1 TWID3
REAL SIGN L7 TWID4
WINDOW4 K2 TWID5
WINDOW5 L1 TWID6
WINDOW6 M1 TWID7
MSB WINDOW7 K3 TWID8
IMAG SIGN M2 TWID9

POSITIVE REAL
5,0,4 REAL NUMBER.

NDATAIN[0..15]

NDATAIN0 C1 NDATAIN0
NDATAIN1 D3 NDATAIN1
NDATAIN2 B2 NDATAIN2
NDATAIN3 B3 NDATAIN3
NDATAIN4 A2 NDATAIN4
NDATAIN5 B4 NDATAIN5
NDATAIN6 A4 NDATAIN6
NDATAIN7 A5 NDATAIN7
NDATAIN8 B6 NDATAIN8
NDATAIN9 A8 NDATAIN9
NDATAIN10 C8 NDATAIN10
NDATAIN11 B9 NDATAIN11
NDATAIN12 C9 NDATAIN12
NDATAIN13 A11 NDATAIN13
NDATAIN14 C10 NDATAIN14
NDATAIN15 B12 NDATAIN15
D11 NDATAIN16
C13 NDATAIN17

FROM FRINGE ROTATOR ROM

772 #

GROUND 2 MSB'S OF EXPONENT.

AUXIN[0..15]

AUXIN0 D2 AUXIN0
AUXIN1 C2 AUXIN1
AUXIN2 B1 AUXIN2
AUXIN3 C4 AUXIN3
AUXIN4 A3 AUXIN4
AUXIN5 C5 AUXIN5
AUXIN6 B5 AUXIN6
AUXIN7 C6 AUXIN7
AUXIN8 A6 AUXIN8
AUXIN9 B8 AUXIN9
AUXIN10 A9 AUXIN10
AUXIN11 A10 AUXIN11
AUXIN12 B10 AUXIN12
AUXIN13 B11 AUXIN13
AUXIN14 A12 AUXIN14
AUXIN15 C12 AUXIN15
B13 AUXIN16
D12 AUXIN17

FROM FRINGE ROTATOR ROM

772 #

M3 NCOOE
TWIDOE N3 TWIDOE

CLK J3 NCOCLK
M4 NCOCE
N7 DATAENBL

NCOSI N2 NCOSI
NCOCI L4 NCOCI
NCOLDIN\ N4 NCOLDIN
NCOSRCLK L5 NCOSRCLK
NCOSTA\ N5 NCOSTA
NCORW\ L6 NCORW

L8 WEINA
N9 WEINB
N8 EXTASEL
M8 EXTBSEL

ASIC

DATAOUT[0..17]

OUT0 E11 DATAOUT0
OUT1 D13 DATAOUT1
OUT2 E12 DATAOUT2
OUT3 E13 DATAOUT3
OUT4 F11 DATAOUT4
OUT5 F12 DATAOUT5
OUT6 F13 DATAOUT6
OUT7 G13 DATAOUT7
OUT8 J12 DATAOUT8
OUT9 K13 DATAOUT9
OUT10 J11 DATAOUT10
OUT11 K12 DATAOUT11
OUT12 L13 DATAOUT12
OUT13 L12 DATAOUT13
OUT14 K11 DATAOUT14
OUT15 M13 DATAOUT15
OUT16 M12 DATAOUT16
OUT17 L11 DATAOUT17

FOR VIEWING ASYMETRICAL RAM WE PULSE.
HAVE WEOUT BIT SET IN THE CONTROL WORD.
GET WE\ OUT = CLK * CLKA

PROBE TEST POINT
TP1

CRSO N11 CRSO
CRBIT N12

TEKTRONIX
131-4244-00

ACTUALLY CONSISTS OF A CENTER SIGNAL PIN
AND 4 SURROUNDING GROUND PINS

R2CNT0 L2

EXPOF M9

CAN OUTPUT NCO DATA TO LOAD RAM.

EXTADD\[0..8]

EXTADD_0 E3 EXTADD\0
EXTADD_1 D1 EXTADD\1
EXTADD_2 E2 EXTADD\2
EXTADD_3 E1 EXTADD\3
EXTADD_4 F3 EXTADD\4
EXTADD_5 F2 EXTADD\5
EXTADD_6 F1 EXTADD\6
EXTADD_7 G2 EXTADD\7
EXTADD_8 H1 EXTADD\8
NCODOUT9 H2

PIN 9 NCO ONLY

NCOSO M5 NCOSO
NCOCO M6 NCOCO

VLBA CORRELATOR PROJECT

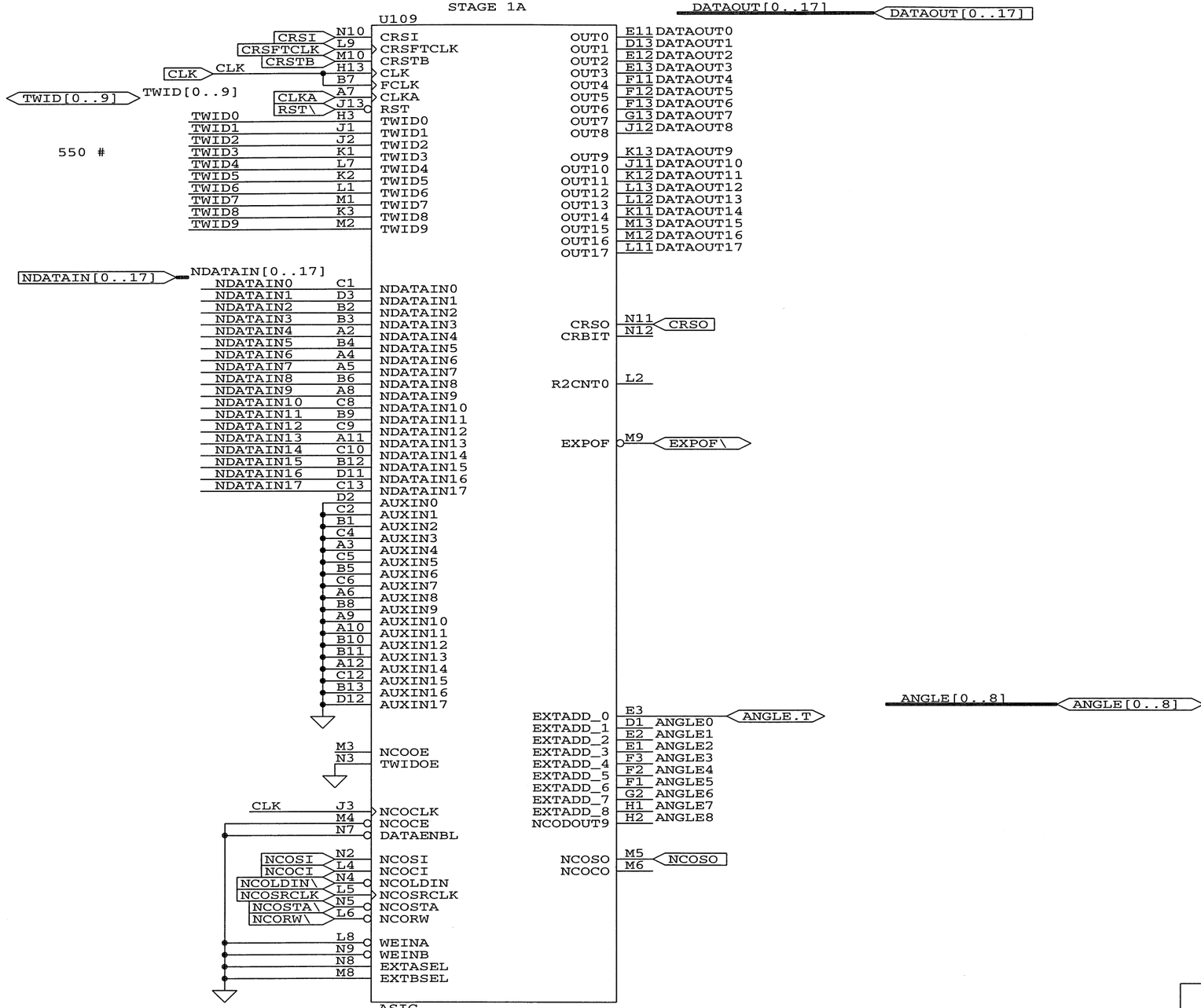
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
STAGE 0A ASIC HOOKUP

Size	Document Number	REV
B	56000L002 (L002D08.SCH)	
Date: May 6, 1997	Sheet 8 of 41	

STAGE 1A

U109



VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title STAGES 1 ASIC HOOKUP		
Size B	Document Number 56000L002 (L002D09.SCH)	REV
Date: May 6, 1997	Sheet 9 of 41	

F823 9.5 NS OUT MAX.

TWID[0..9] TWID[0..9]

NDATAIN[0..17] NDATAIN[0..17]

AUXIN[0..17] AUXIN[0..17]

STAGE 4A

U113

	CRSI	N10	CRSI	OUT0	E11 DATAOUT0
	CRSFTCLK	L9	CRSFTCLK	OUT1	D13 DATAOUT1
	CRSTB	M10	CRSTB	OUT2	E12 DATAOUT2
CLK	CLK	H13	CLK	OUT3	E13 DATAOUT3
		B7	FCLK	OUT4	F11 DATAOUT4
550 #	CLKA	A7	CLKA	OUT5	F12 DATAOUT5
	RST\	J13	RST	OUT6	F13 DATAOUT6
TWID0		H3	TWID0	OUT7	G13 DATAOUT7
TWID1		J1	TWID1	OUT8	J12 DATAOUT8
TWID2		J2	TWID2		
TWID3		K1	TWID3	OUT9	K13 DATAOUT9
TWID4		L7	TWID4	OUT10	J11 DATAOUT10
TWID5		K2	TWID5	OUT11	K12 DATAOUT11
TWID6		L1	TWID6	OUT12	L13 DATAOUT12
TWID7		M1	TWID7	OUT13	L12 DATAOUT13
TWID8		K3	TWID8	OUT14	K11 DATAOUT14
TWID9		M2	TWID9	OUT15	M13 DATAOUT15
				OUT16	M12 DATAOUT16
				OUT17	L11 DATAOUT17
NDATAIN0		C1	NDATAIN0		
NDATAIN1		D3	NDATAIN1		
NDATAIN2		B2	NDATAIN2		
NDATAIN3		B3	NDATAIN3	CRSO	N11 CRSO
NDATAIN4		A2	NDATAIN4	CRBIT	N12
NDATAIN5		B4	NDATAIN5		
NDATAIN6		A4	NDATAIN6		
NDATAIN7		A5	NDATAIN7		
NDATAIN8		B6	NDATAIN8	R2CNT0	L2 R2CNT0
NDATAIN9		A8	NDATAIN9		
NDATAIN10		C8	NDATAIN10		
NDATAIN11		B9	NDATAIN11		
NDATAIN12		C9	NDATAIN12		
NDATAIN13		A11	NDATAIN13	EXPOF	M9 EXPOF\
NDATAIN14		C10	NDATAIN14		
NDATAIN15		B12	NDATAIN15		
NDATAIN16		D11	NDATAIN16		
NDATAIN17		C13	NDATAIN17		
AUXIN0		D2	AUXIN0		
AUXIN1		C2	AUXIN1		
AUXIN2		B1	AUXIN2		
AUXIN3		C4	AUXIN3		
AUXIN4		A3	AUXIN4		
AUXIN5		C5	AUXIN5		
AUXIN6		B5	AUXIN6		
AUXIN7		C6	AUXIN7		
AUXIN8		A6	AUXIN8		
AUXIN9		B8	AUXIN9		
AUXIN10		A9	AUXIN10		
AUXIN11		A10	AUXIN11		
AUXIN12		B10	AUXIN12		
AUXIN13		B11	AUXIN13		
AUXIN14		A12	AUXIN14		
AUXIN15		C12	AUXIN15		
AUXIN16		B13	AUXIN16		
AUXIN17		D12	AUXIN17		
				EXTADD_0	E3
				EXTADD_1	D1 FSC.T
				EXTADD_2	E2 ANGLE0
				EXTADD_3	E1 ANGLE1
				EXTADD_4	F3 ANGLE2
				EXTADD_5	F2 ANGLE3
				EXTADD_6	F1 ANGLE4
				EXTADD_7	G2 ANGLE5
				EXTADD_8	H1 ANGLE6
				NCODOUT9	H2 ANGLE7
					MSB
	NCOOE	M3			
	TWIDOE	N3			
CLK		J3	NCOCLK		
NCOCE\		M4	NCOCE		
DINVALID		N7	DATAENBL		
	NCOSI	N2	NCOSI	NCOSO	M5 NCOSO
	NCOCI	L4	NCOCI	NCOCO	M6
	NCOLDIN\	N4	NCOLDIN		
	NCOSRCLK	L5	NCOSRCLK		
	NCOSTA\	N5	NCOSTA		
	NCORW\	L6	NCORW		
		L8	WEINA		
		N9	WEINB		
		N8	EXTASEL		
		M8	EXTBSEL		

ASIC

8K X 8 PROM
24 PIN 300 MIL

U129

R0	COS0	8	A0	O0	9 COSA0
R1	COS1	7	A1	O1	10 COSA1
a R2	COS2	6	A2	O2	11 COSA2
R3	COS3	5	A3	O3	13 COSA3
R4	COS4	4	A4	O4	14 COSA4
ANGLE0		3	A5	O5	15
ANGLE1		2	A6	O6	16
ANGLE2		1	A7	O7	17
ANGLE3		23	A8		
b ANGLE4		22	A9		
ANGLE5		21	A10		
ANGLE6		19	A11		
ANGLE7		18	A12		
		20	CS/VPP		

AT27HC642-55DC
ATMEL

COSA[0..4] COSA[0..4]

TO REGISTER, THEN MUX

ALSO MADE BY CYPRESS, GIM, GOLDSTAR, ICT, WAFERSCALE, FUJITSU, SIGNETICS

e**-j(a+b)

U130

R0	SIN0	8	A0	O0	9 SINA0
R1	SIN1	7	A1	O1	10 SINA1
a R2	SIN2	6	A2	O2	11 SINA2
R3	SIN3	5	A3	O3	13 SINA3
R4	COS4	4	A4	O4	14 SINA4
ANGLE0		3	A5	O5	15
ANGLE1		2	A6	O6	16
ANGLE2		1	A7	O7	17
ANGLE3		23	A8		
b ANGLE4		22	A9		
ANGLE5		21	A10		
ANGLE6		19	A11		
ANGLE7		18	A12		
		20	CS/VPP		

AT27HC642-55DC

SINA[0..4] SINA[0..4]

256 X 8 PROM 45 NS
20 PIN, 300 MIL

U131

ANGLE0		1	A0	O1	6 COSB0
ANGLE1		2	A1	O2	7 COSB1
b ANGLE2		3	A2	O3	8 COSB2
ANGLE3		4	A3	O4	9 COSB3
ANGLE4		5	A4	O5	11 COSB4
ANGLE5		17	A5	O6	12
ANGLE6		18	A6	O7	13
ANGLE7		19	A7	O8	14
		15	E1		
		16	E2		

63S281
MMI

e**-jb

COSB[0..4] COSB[0..4]

U132

ANGLE0		1	A0	O1	6 SINB0
ANGLE1		2	A1	O2	7 SINB1
b ANGLE2		3	A2	O3	8 SINB2
ANGLE3		4	A3	O4	9 SINB3
ANGLE4		5	A4	O5	11 SINB4
ANGLE5		17	A5	O6	12
ANGLE6		18	A6	O7	13
ANGLE7		19	A7	O8	14
		15	E1		
		16	E2		

63S281

SINB[0..4] SINB[0..4]

TO MUX

WHEN STAGE 5 IS DOING FSE ONLY (NO RADIX 2),
HAVE THE REG FROM THE LARGE PROM CLEARED.
WHEN THE MUX SWITCHES TO IT, IT WILL READ 0.

COULD USE 2 8K X 8 RAMS(PERFORMANCE P4C164). 20 NS.
INSTEAD OF SWITCHING BETWEEN ROMS.
COULD LOAD RAMS THROUGH NCO AND SIN/COS ANGLES IN.
WOULD NEED TO STAGGER CLKS, SINCE ONLY 15 NS AVAILABLE.

DATAOUT[0..17] DATAOUT[0..17]

CY7C263 8K X 8 PROM
-45PC OR WC - $22
-55PC OR WC - $18

THE ORIGINAL SINES AND COSINES TO THE FSTC ROMS
HAVE BEEN REPLACED WITH A FIVE BIT ANGLE INDEX.
THE FOUR LSB'S ARE SENT TWICE.
THE MSB IS SENT ONCE.
THE MSB REPRESENTS 90 DEGREES.
THE BUS IS SHOWN AS R[0..4].

SIN/COS[0..8] SIN/COS[0..8]

FROM ANGLE MUX
CLOCKED BY FCLK

SIN/COS0	COS0	R0	ANGLE a
SIN/COS1	COS1	R1	
SIN/COS2	COS2	R2	
SIN/COS3	COS3	R3	
SIN/COS4	COS4	R4	
SIN/COS5	SIN0	R0	
SIN/COS6	SIN1	R1	
SIN/COS7	SIN2	R2	
SIN/COS8	SIN3	R3	

BIG ROM TIMING
62 NS CYCLE
-3 NS SU
-9.5NS ANGLE MUX REG
+2.5NS FCLK TO ANGLE MUX
+3.9 NS BC DE NCO
55.9 NS PROM REQ.

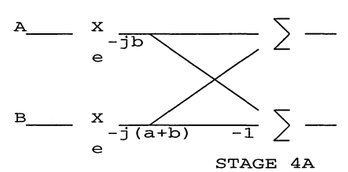
SMALL ROM TIMING
62 NS CYCLE
-12 NS SU FROM NCO
-3 NS SU
47 NS PROM REQ.
|0NS

5 NS CLK TO Q

S/C FROM ANGLE MUX |9.5NS DLY ANGLE2 |
UPDATE ANGLE b|3.9 NS BC FROM NCO |
R2CNT0 FROM STG4 CLK BIG ROM REG |1 12 NS DLY 3NS SU|2
DELAY ABOVE THRU FF 9.5NS SU MUX WORD SEL | SEL BIG 1 | SEL SMALL2
399 MUX CLK 4.5 NS SU |CLK SMALL1 |CLK BIG 1 |CLK SML2

IF b IS THE FSTC ANGLE, THE SMALL ROM OUTPUTS e**jb.
IF THE SIN/COS IS THE ANGLE a, THE LARGE ROM OUTPUTS e**-j(a+b)

FSTC USING RADIX 2 BUTTERFLY



STAGE 4A

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
STAGE 4 FFTS WITH FSTC ROMS

Size	Document Number	REV
B	56000L002 (L002D10.SCH)	

Date: December 10, 1997 Sheet 10 of 41

STAGE 5A

U119

CRSI	N10	CRSI	OUT0	E11		R0
CRSFTCLK	L9	CRSFTCLK	OUT1	D13		R1
CRSTB	M10	CRSTB	OUT2	E12		R2
CLK	H13	CLK	OUT3	E13	DATAOUT0	R3
CLK	B7	FCLK	OUT4	F11	DATAOUT1	R4
TWID[0..9]	A7	CLKA	OUT5	F12	DATAOUT2	R5
	J13	RST	OUT6	F13	DATAOUT3	R6
TWID0	H3	TWID0	OUT7	G13		I0
TWID1	J1	TWID1	OUT8	J12		I1
TWID2	J2	TWID2				
TWID3	K1	TWID3	OUT9	K13		I2
TWID4	L7	TWID4	OUT10	J11	DATAOUT4	I3
TWID5	K2	TWID5	OUT11	K12	DATAOUT5	I4
TWID6	L1	TWID6	OUT12	L13	DATAOUT6	I5
TWID7	M1	TWID7	OUT13	L12	DATAOUT7	I6
TWID8	K3	TWID8	OUT14	K11	DATAOUT8	E0
TWID9	M2	TWID9	OUT15	M13	DATAOUT9	E1
			OUT16	M12	DATAOUT10	E2
			OUT17	L11	DATAOUT11	E3

DATAOUT[0..11] DATAOUT[0..11]

4,4,4 NUMBER OUT

550 #

NDATAIN[0..17] NDATAIN[0..17]

NDATAIN0	C1	NDATAIN0
NDATAIN1	D3	NDATAIN1
NDATAIN2	B2	NDATAIN2
NDATAIN3	B3	NDATAIN3
NDATAIN4	A2	NDATAIN4
NDATAIN5	B4	NDATAIN5
NDATAIN6	A4	NDATAIN6
NDATAIN7	A5	NDATAIN7
NDATAIN8	B6	NDATAIN8
NDATAIN9	A8	NDATAIN9
NDATAIN10	C8	NDATAIN10
NDATAIN11	B9	NDATAIN11
NDATAIN12	C9	NDATAIN12
NDATAIN13	A11	NDATAIN13
NDATAIN14	C10	NDATAIN14
NDATAIN15	B12	NDATAIN15
NDATAIN16	D11	NDATAIN16
NDATAIN17	C13	NDATAIN17

CRSO N11 CRSO

CRBIT N12 CRBIT

R2CNT0 L2 R2CNT0

EXPOF M9 EXPOF\

AUXIN[0..17] AUXIN[0..17]

AUXIN0	D2	AUXIN0
AUXIN1	C2	AUXIN1
AUXIN2	B1	AUXIN2
AUXIN3	C4	AUXIN3
AUXIN4	A3	AUXIN4
AUXIN5	C5	AUXIN5
AUXIN6	B5	AUXIN6
AUXIN7	C6	AUXIN7
AUXIN8	A6	AUXIN8
AUXIN9	B8	AUXIN9
AUXIN10	A9	AUXIN10
AUXIN11	A10	AUXIN11
AUXIN12	B10	AUXIN12
AUXIN13	B11	AUXIN13
AUXIN14	A12	AUXIN14
AUXIN15	C12	AUXIN15
AUXIN16	B13	AUXIN16
AUXIN17	D12	AUXIN17

EXTADD\[0..8] EXTADD\[0..8]

EXTADD_0	E3	EXTADD\0
EXTADD_1	D1	EXTADD\1
EXTADD_2	E2	EXTADD\2
EXTADD_3	E1	EXTADD\3
EXTADD_4	F3	EXTADD\4
EXTADD_5	F2	EXTADD\5
EXTADD_6	F1	EXTADD\6
EXTADD_7	G2	EXTADD\7
EXTADD_8	H1	EXTADD\8
NCODOUT9	H2	MSB

	M3	NCOOE			
	N3	TWIDOE			
CLK	J3	NCOCLK			
NCOCE\	M4	NCOCE			
DATAENBL\	N7	DATAENBL			
NCOSI	N2	NCOSI	NCOSO	M5	
	L4	NCOCI	NCOCO	M6	NCOCO
NCOLDIN\	N4	NCOLDIN			
NCOSRCLK	L5	NCOSRCLK			
NCOSTA\	N5	NCOSTA			
NCORW\	L6	NCORW			
	L8	WEINA			
	N9	WEINB			
	N8	EXTASEL			
	M8	EXTBSEL			

ASIC

NCOCE\ FROM RAM.
GIVES VARIABLE RATE.
USE FRZNCO IN ASIC CTRL WORD
FOR RAM LOADING.

STAGE 5A

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
FFT STAGE 5 ASIC HOOKUP

Size	Document Number	REV
B	56000L002 (L002D14.SCH)	

Date: May 6, 1997 Sheet 14 of 41

STAGE 2A

U110

CRSI	N10	CRSI	OUT0	E11	DATAOUT0
CRSFTCLK	L9	CRSFTCLK	OUT1	D13	DATAOUT1
CRSTB	M10	CRSTB	OUT2	E12	DATAOUT2
CLK	H13	CLK	OUT3	E13	DATAOUT3
	B7	FCLK	OUT4	F11	DATAOUT4
TWID[0..9]	A7	CLKA	OUT5	F12	DATAOUT5
CLKA	J13	RST	OUT6	F13	DATAOUT6
RST\	H3	TWID0	OUT7	G13	DATAOUT7
TWID0	J1	TWID1	OUT8	J12	DATAOUT8
TWID1	J2	TWID2			
TWID2	K1	TWID3	OUT9	K13	DATAOUT9
TWID3	L7	TWID4	OUT10	J11	DATAOUT10
TWID4	K2	TWID5	OUT11	K12	DATAOUT11
TWID5	L1	TWID6	OUT12	L13	DATAOUT12
TWID6	M1	TWID7	OUT13	L12	DATAOUT13
TWID7	K3	TWID8	OUT14	K11	DATAOUT14
TWID8	M2	TWID9	OUT15	M13	DATAOUT15
TWID9			OUT16	M12	DATAOUT16
			OUT17	L11	DATAOUT17
NDATAIN[0..17]					
NDATAIN0	C1	NDATAIN0			
NDATAIN1	D3	NDATAIN1			
NDATAIN2	B2	NDATAIN2			
NDATAIN3	B3	NDATAIN3	CRSO	N11	CRSO
NDATAIN4	A2	NDATAIN4	CRBIT	N12	
NDATAIN5	B4	NDATAIN5			
NDATAIN6	A4	NDATAIN6			
NDATAIN7	A5	NDATAIN7			
NDATAIN8	B6	NDATAIN8	R2CNT0	L2	
NDATAIN9	A8	NDATAIN9			
NDATAIN10	C8	NDATAIN10			
NDATAIN11	B9	NDATAIN11			
NDATAIN12	C9	NDATAIN12			
NDATAIN13	A11	NDATAIN13	EXPOF	M9	EXPOF\
NDATAIN14	C10	NDATAIN14			
NDATAIN15	B12	NDATAIN15			
NDATAIN16	D11	NDATAIN16			
NDATAIN17	C13	NDATAIN17			
	D2	AUXIN0			
	C2	AUXIN1			
	B1	AUXIN2			
	C4	AUXIN3			
	A3	AUXIN4			
	C5	AUXIN5			
	B5	AUXIN6			
	C6	AUXIN7			
	A6	AUXIN8			
	B8	AUXIN9			
	A9	AUXIN10			
	A10	AUXIN11			
	B10	AUXIN12			
	B11	AUXIN13			
	A12	AUXIN14			
	C12	AUXIN15			
	B13	AUXIN16			
	D12	AUXIN17			
NCOOE	M3	NCOOE			
	N3	TWIDOE			
CLK	J3	NCOCLK			
	M4	NCOCE			
	N7	DATAENBL			
NCOSI	N2	NCOSI	NCOSO	M5	NCOSO
NCOCI	L4	NCOCI	NCOCO	M6	NCOCO
NCOLDIN\	N4	NCOLDIN			
NCOSRCLK	L5	NCOSRCLK			
NCOSTA\	N5	NCOSTA			
NCORW\	L6	NCORW			
	L8	WEINA			
	N9	WEINB			
	N8	EXTASEL			
	M8	EXTBSEL			

ASIC

DATAOUT[0..17] — DATAOUT[0..17]

550 #

FOR LOADING MISCELLANEOUS RAM VALUES.

RAM FUNCTION

EXTADD_0	E3	RAMLD0	INIT\1	RAMLD[0..4]	RAMLD[0..4]
EXTADD_1	D1	RAMLD1	INIT\2		
EXTADD_2	E2	RAMLD2	FSCE\		
EXTADD_3	E1	RAMLD3	ST\0		
EXTADD_4	F3	RAMLD4	ST\1		
EXTADD_5	F2				
EXTADD_6	F1				
EXTADD_7	G2				
EXTADD_8	H1				
NCODOUT9	H2				

STAGE 2A

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: STAGES 2 ASIC HOOKUP

Size	Document Number	REV
B	56000L002 (L002D21.SCH)	

Date: May 6, 1997 | Sheet 21 of 41

STAGE 3A

U112

CRSI	N10	CRSI	
CRSFTCLK	L9	CRSFTCLK	
CRSTB	M10	CRSTB	
CLK	H13	CLK	
CLK	B7	FCLK	
CLKA	A7	CLKA	
RST\	J13	RST	
TWID[0..9]	TWID[0..9]		
TWID0	H3	TWID0	
TWID1	J1	TWID1	
TWID2	J2	TWID2	
550 #			
TWID3	K1	TWID3	
TWID4	L7	TWID4	
TWID5	K2	TWID5	
TWID6	L1	TWID6	
TWID7	M1	TWID7	
TWID8	K3	TWID8	
TWID9	M2	TWID9	
NDATAIN[0..17]	NDATAIN[0..17]		
NDATAIN0	C1	NDATAIN0	
NDATAIN1	D3	NDATAIN1	
NDATAIN2	B2	NDATAIN2	
NDATAIN3	B3	NDATAIN3	
NDATAIN4	A2	NDATAIN4	
NDATAIN5	B4	NDATAIN5	
NDATAIN6	A4	NDATAIN6	
NDATAIN7	A5	NDATAIN7	
NDATAIN8	B6	NDATAIN8	
NDATAIN9	A8	NDATAIN9	
NDATAIN10	C8	NDATAIN10	
NDATAIN11	B9	NDATAIN11	
NDATAIN12	C9	NDATAIN12	
NDATAIN13	A11	NDATAIN13	
NDATAIN14	C10	NDATAIN14	
NDATAIN15	B12	NDATAIN15	
NDATAIN16	D11	NDATAIN16	
NDATAIN17	C13	NDATAIN17	
	D2	AUXIN0	
	C2	AUXIN1	
	B1	AUXIN2	
	C4	AUXIN3	
	A3	AUXIN4	
	C5	AUXIN5	
	B5	AUXIN6	
	C6	AUXIN7	
	A6	AUXIN8	
	B8	AUXIN9	
	A9	AUXIN10	
	A10	AUXIN11	
	B10	AUXIN12	
	B11	AUXIN13	
	A12	AUXIN14	
	C12	AUXIN15	
	B13	AUXIN16	
	D12	AUXIN17	
NCOOE	M3	NCOOE	
	N3	TWIDOE	
CLK	J3	NCOCLK	
	M4	NCOCE	
	N7	DATAENBL	
NCOSI	N2	NCOSI	
	L4	NCOCI	
NCOLDIN\	N4	NCOLDIN	
NCOSRCLK	L5	NCOSRCLK	
NCOSTA\	N5	NCOSTA	
NCORW\	L6	NCORW	
	L8	WEINA	
	N9	WEINB	
	N8	EXTASEL	
	M8	EXTBSEL	

ASIC

DATAOUT[0..17] — DATAOUT[0..17]

OUT0	E11	DATAOUT0
OUT1	D13	DATAOUT1
OUT2	E12	DATAOUT2
OUT3	E13	DATAOUT3
OUT4	F11	DATAOUT4
OUT5	F12	DATAOUT5
OUT6	F13	DATAOUT6
OUT7	G13	DATAOUT7
OUT8	J12	DATAOUT8
OUT9	K13	DATAOUT9
OUT10	J11	DATAOUT10
OUT11	K12	DATAOUT11
OUT12	L13	DATAOUT12
OUT13	L12	DATAOUT13
OUT14	K11	DATAOUT14
OUT15	M13	DATAOUT15
OUT16	M12	DATAOUT16
OUT17	L11	DATAOUT17
CRSO	N11	CRSO
CRBIT	N12	
R2CNT0	L2	
EXPOF	M9	EXPOF\

EXT5LD\[0..8] — EXT5LD\[0..8]

EXTADD_0	E3	EXT5LD\0
EXTADD_1	D1	EXT5LD\1
EXTADD_2	E2	EXT5LD\2
EXTADD_3	E1	EXT5LD\3
EXTADD_4	F3	EXT5LD\4
EXTADD_5	F2	EXT5LD\5
EXTADD_6	F1	EXT5LD\6
EXTADD_7	G2	EXT5LD\7
EXTADD_8	H1	EXT5LD\8
NCODOUT9	H2	
NCOSO	M5	NCOSO
NCOCO	M6	NCOCO

STAGE 3A

VLBA CORRELATOR PROJECT		
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title STAGES 3 ASIC HOOKUP WITH RAMLD OUT		
Size B	Document Number 56000L002 (L002D25.SCH)	REV
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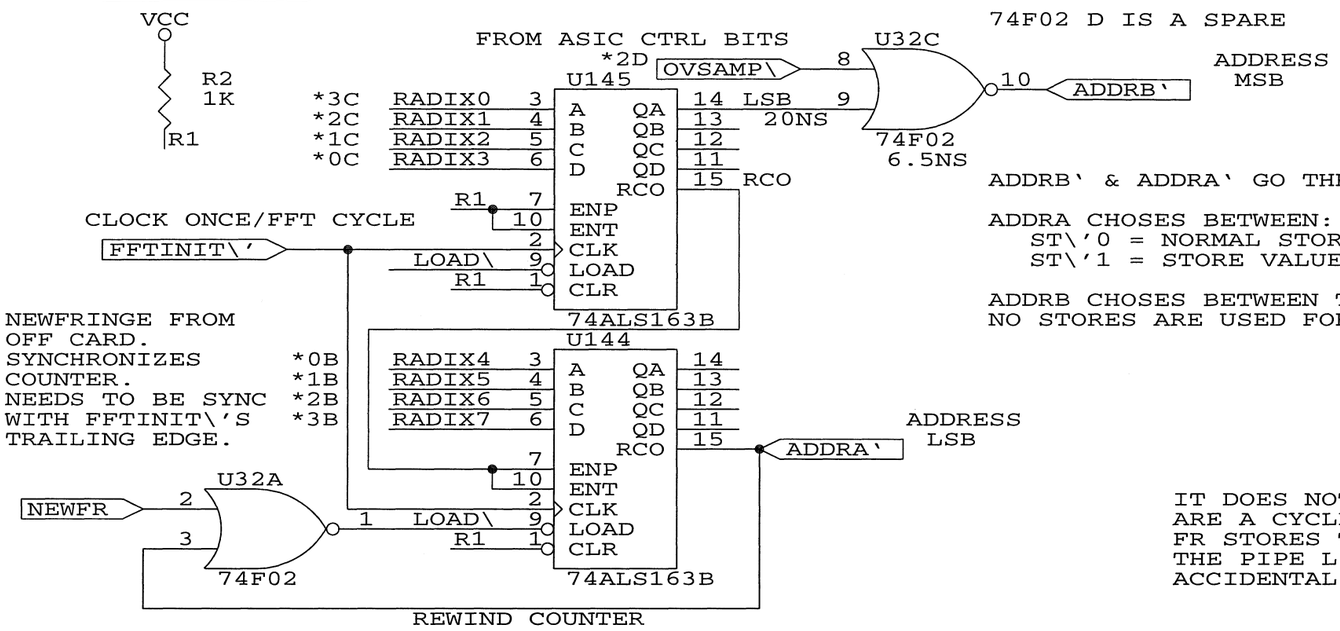
FROM ASIC CONTROL BITS OUT

RADIX[0..7]

RADIX[0..7]

RADIX OF 0 CAUSES ONLY FRST\0 TO BE USED, AS IN NO OVERLAPPING OR OVERSAMPLING.



74F02 D IS A SPARE

ADDRB` & ADDRA` GO THRU A PIPELINE REG TO A 4 TO 1 MUX

ADDRA CHOSES BETWEEN:
ST\'0 = NORMAL STORE VALUE FOR SMALL OFFSET.
ST\'1 = STORE VALUE FOR LARGE OFFSET AT END OF CYCLE.

ADDRB CHOSES BETWEEN THE ABOVE OR NO STORES AT ALL.
NO STORES ARE USED FOR THE EVEN CYCLES, WHEN OVERSAMPLED.

IT DOES NOT MATTER IF ADDRA` & ADDRB`
ARE A CYCLE LATE, SINCE THERE ARE NO
FR STORES TILL LATER IN THE FFT CYCLE.
THE PIPE LINE REGISTER PREVENTS AN
ACCIDENTAL STORE DUE TO A MULTIPLEXER GLITCH.

RADIX=FC

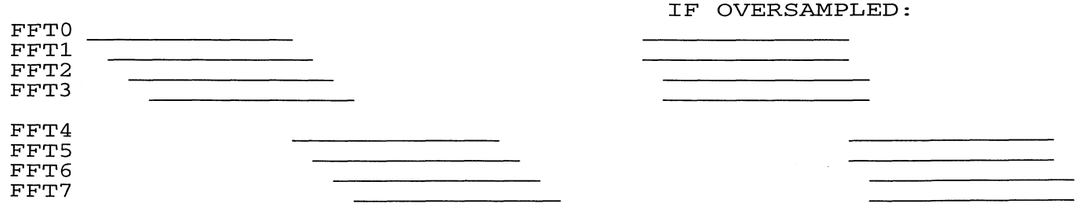
IF NOT OVERSAMPLED HAVE ADDRB=0
IF OVERSAMPLED TOGGLE
ADDRB 0=GENERATE STORES
1=NO STORES

CTR STATE		RC0	LSB	ADDRB
FFT0	FC	0	0	1
FFT1	FD	0	1	0
FFT2	FE	0	0	1
FFT3	FF	1	1	0
FFT4	FC	0	0	1
FFT5	FD	0	1	0
FFT6	FE	0	0	1
FFT7	FF	1	1	0

ADDRB INVERTED FROM LSB

WHAT IF RAM INC TO ANOTHER ST AFTER LOAD?
PAUSE WILL BE AN INTEGRAL # OF FFT CYCLES.
HAVE LOAD AT END OF FFT CYCLE.

WITH RADIX = FC:
IF NOT OVERSAMPLED:



IF OVERSAMPLED:

*3C REFERS TO A SIGNAL FROM CRBIT OF COLUMN 3 ROW C.

VLBA CORRELATOR PROJECT

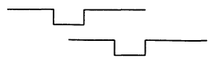
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
NCO STORE MUX ADDRESS GENERATOR

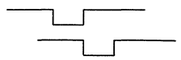
Size	Document Number	REV
A	56000L002 (L002D32.SCH)	

Date: May 6, 1997 Sheet 32 of 41

For the Fringe Rotator NCO, the Load pulses between stages are separated by an extra 32 ns as shown below:



For the FSTC NCO, we can have the load pulses right next to each other as shown below:



This works, since the clock enable to the FSTC allows the carry-in/carry-out pipelining to become invisible.

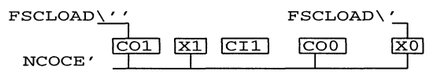
This sheet shows how the closer together load pulses works for 16 MHz operation (512, 1024, or 2048 point ffts).

This sheet also shows the closer together load pulses become essential for 8 MHz operation (256 point ffts).

Therefore, using the closer together load pulses works for all cases.

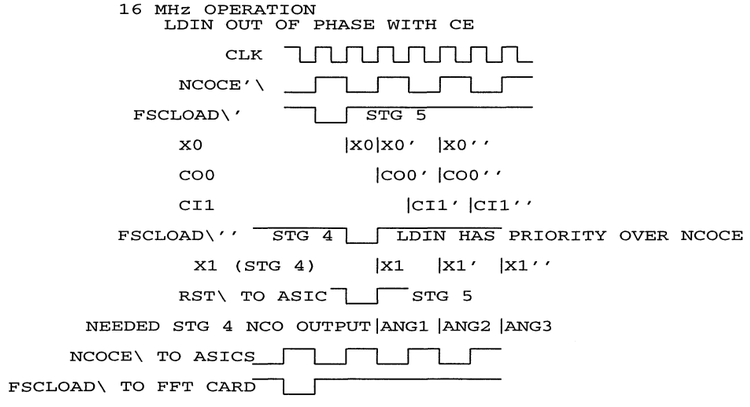
CLOSE TOGETHER LOAD PULSES - 16 MHZ

NCOCE'\ & FSCLOAD\' IN THIS BLOCK, AFTER AN INTERNAL ASIC PIPELINE.



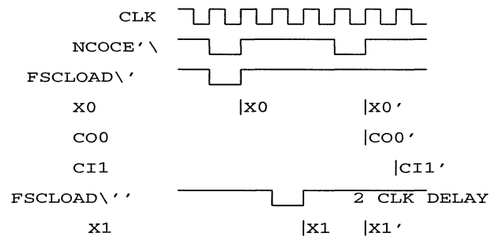
X0'=INIT X0 PHASE PLUS ONE INCREMENT.

16 MHz OPERATION
LDIN OUT OF PHASE WITH CE



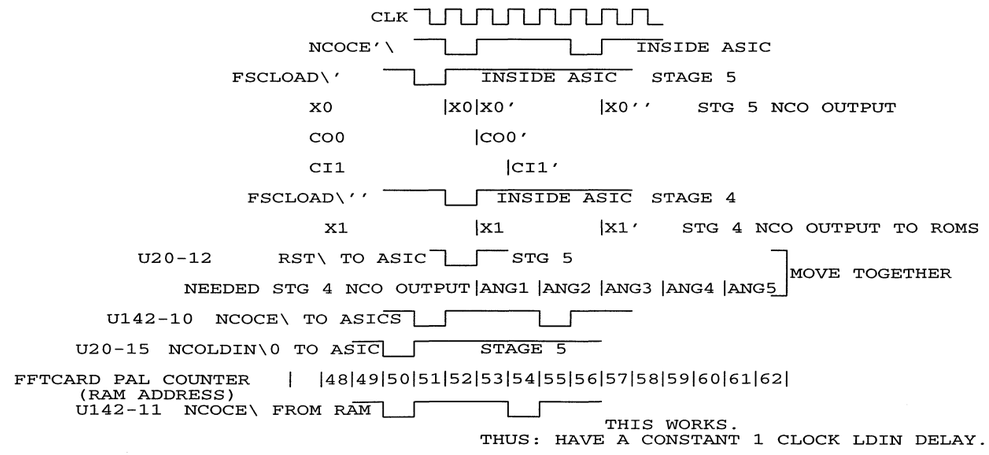
NEED 1 CLK DELAY BETWEEN LOADINS.

SEPARATED LOAD PULSES - 8MHZ



ABOVE DOES NOT WORK!!!
CI1' NEEDED FOR X1' GENERATION.

CLOSE TOGETHER LOAD PULSES - 8 MHZ



THIS WORKS.
THUS: HAVE A CONSTANT 1 CLOCK LDIN DELAY.

RST\ TO STG1 8
RST\ TO STG2 19
RST\ TO STG3 30
RST\ TO STG4 41
RST\ TO STG5 52
ONLY THE RST\ TO STG5 IS RELEVANT TO THIS DRAWING

CE AND RW MUX AUTOMATICALLY GIVE 1 BIT DELAY FOR 2K LOWER.

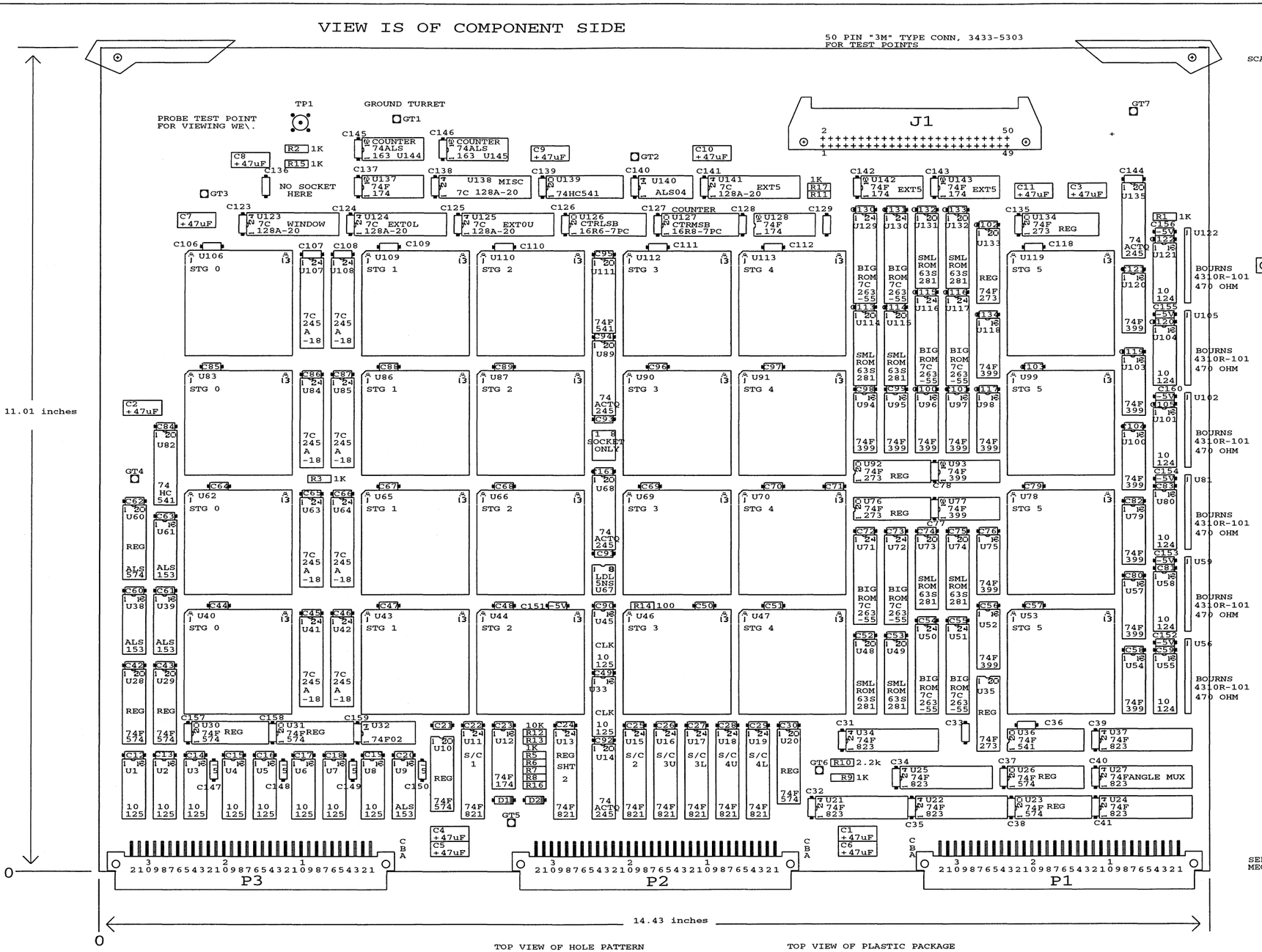
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: FSTC CE AND LD TIMING

Size	Document Number	REV
B	56000L002 (L002D38.SCH)	

Date: June 16, 1997 Sheet 38 of 41

VIEW IS OF COMPONENT SIDE



9U X 280 CARD
14.5 X 11.0 INCHES

SEE NRAO DRAWING # 56000M003 FOR
MECHANICAL DETAILS OF CARD.

THIS SKETCH DETAILS THE APPROXIMATE
LOCATIONS OF ALL COMPONENTS.

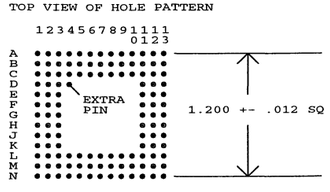
ALL COMPONENTS WILL BE ON GRID UNLESS OTHERWISE NOTED.

NOTE CHIP OUTLINES INCLUDE AN EXTRA 0.1 INCH LENGTH.

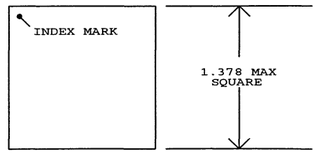
BYPASS CAPACITORS TO -5.2V BYPASS CAPACITORS TO +5 VOLTS

FOR THE SMALL BYPASS CAPACITORS, PIN 1 IS TO THE TOP OR RIGHT,
UNLESS MARKED -5V, WHERE PIN 1 IS TO THE BOTTOM OR LEFT.

TOP VIEW OF HOLE PATTERN



TOP VIEW OF PLASTIC PACKAGE



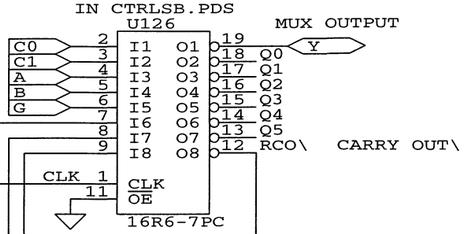
IN m:/fft/sch/SCCS
EDIT IN j:/orcad/fft

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title FFT CARD COMPONENT LAYOUT SKETCH		
Size C	Document Number 56000Z001 (Z001D01.LAY)	REV D
Date: August 8, 1996	Sheet 1 of	1

6.5 NS CLK TO OUTPUT
10 BIT COUNTER

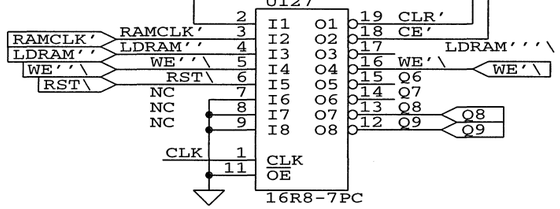
IN CTRLSB.PDS

HALF OF PAL EMULATES A 74F153
C2 & C3 ASSUMED LOGIC 1
G INSTEAD OF G\



IN CTRMSB.PDS

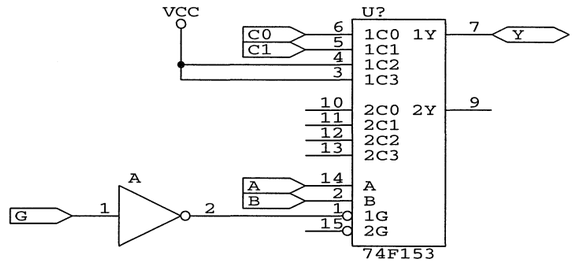
FROM EXTERNAL FF



Q8 & Q9 TO BE DELAYED FOR WINDOW RAM.

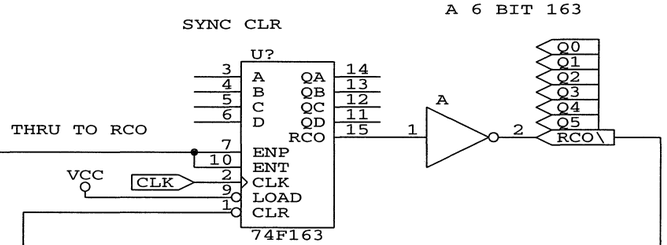
CLEAR CLR':= RST + LDRAM''*LDRAM'''\
COUNT ENABLE CE' := (LDRAM'' * (WE'*WE'')\ )\

16R6 U126 CTRLSB.PDS

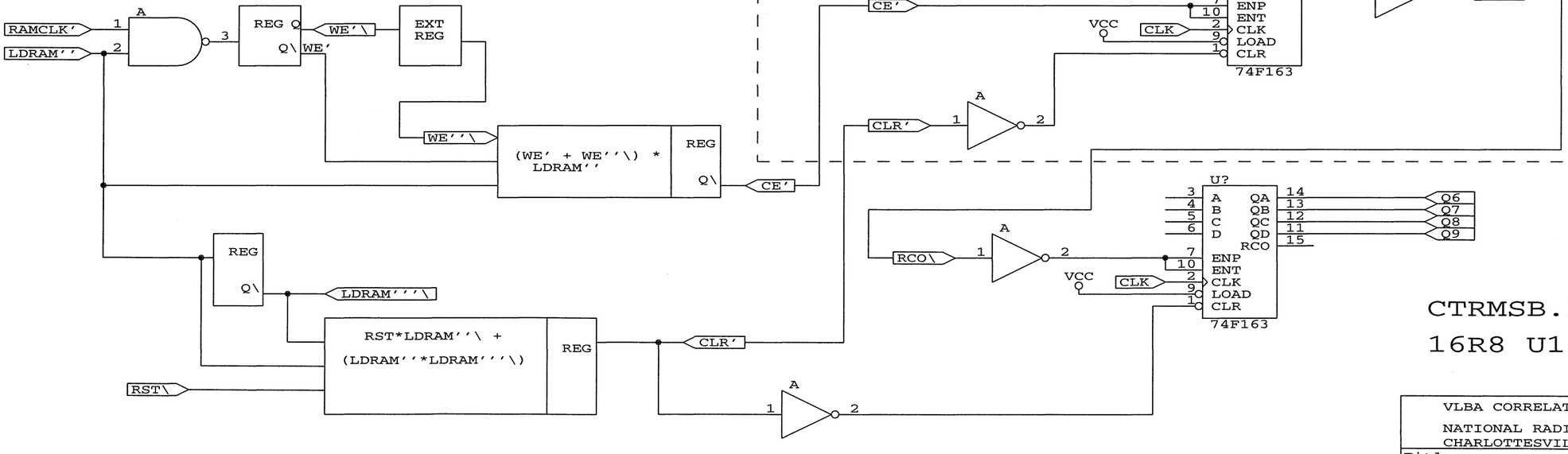


A 6 BIT 163

SYNC CLR



THRU TO RCO



CTRMSB.PDS
16R8 U127

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title PAL DESCRIPTIONS		
Size B	Document Number 56000L002 (L002D34.SCH)	REV
Date: May 6, 1997	Sheet 34 of 41	

4 FFT Bin Schematics

Schematics l025d09.sch, 01, 02, 03, 04, 40, 42, 45, 46

SHT. 14 BELOW CONTAINS THE RACK CONNECTORS
TO THE PLAYBACK DRIVES.

RACK 0

RACK 1

RACK 2

RACK 3

RACK 0 T CHANNELS 0 - 3
B CHANNELS 4 - 7
PLAYBACK DRIVES 1 TO 6
PLAYBACK INTERFACE BIN SHT. 14

DUP1TPBD[1..16]
1TPBD[1..16]
2TPBD[1..16]
3TPBD[1..16]
4TPBD[1..16]
5TPBD[1..16]
6TPBD[1..16]
DUP6TPBD[1..16]

DUP1BPBD[1..16]
1BPBD[1..16]
2BPBD[1..16]
3BPBD[1..16]
4BPBD[1..16]
5BPBD[1..16]
6BPBD[1..16]
DUP6BPBD[1..16]

VALP[0..47]
VALP16[0..47]

1CDLY[0..3]
1DDLY[0..3]
ADLY[0..17]
BDLY[0..17]
6CDLY[0..3]
6DDLY[0..3]

L025D14.sch

RACK 1 T CHANNELS 0 - 3
B CHANNELS 4 - 7
PLAYBACK DRIVES 7 - 12
PLAYBACK INTERFACE BIN SHT. 14

VALP712[0..47]

RACK 2 T CHANNELS 0 - 3
B CHANNELS 4 - 7
PLAYBACK DRIVES 13 - 18
PLAYBACK INTERFACE BIN SHT. 14

VALP1318[0..47]

RACK 3 T CHANNELS 0 - 3
B CHANNELS 4 - 7
PLAYBACK DRIVES 19 - 24
PLAYBACK INTERFACE BIN SHT. 14

VALP1924[0..47]

DIFFERENTIAL
FROM DF CARD

RACK 0 STATIONS 0 - 9 OUT
CHANNELS 0 - 3
PLAYBACK DRIVES 24, 1 - 13 IN
FFT BIN SHT. 5

0PBD[1..16]
1PBD[1..16]
2PBD[1..16]
3PBD[1..16]
4PBD[1..16]
5PBD[1..16]
6PBD[1..16]
7PBD[1..16]
8PBD[1..16]
9PBD[1..16]
10PBD[1..16]
11PBD[1..16]
12PBD[1..16]
13PBD[1..16]

0DT[1..24]
1DT[1..24]
2DT[1..24]
3DT[1..24]
4DT[1..24]
5DT[1..24]
6DT[1..24]
7DT[1..24]
8DT[1..24]
9DT[1..24]

0DB[1..24]
1DB[1..24]
2DB[1..24]
3DB[1..24]
4DB[1..24]
5DB[1..24]
6DB[1..24]
7DB[1..24]
8DB[1..24]
9DB[1..24]

DICOL[0..9]
DICOU[0..9]
DIC1L[0..9]
DIC1U[0..9]
DIVA[0..9]
DIVB[0..9]
DIVC[0..9]
DIVD[0..9]

16DLY[0..17]
712DLY[0..17]
13DLY[0..3]
0DLY[0..3]

L025D05.SCH

RACK 1 STATIONS 10 - 19 OUT
CHANNELS 0 - 3
PLAYBACK DRIVES 12 - 24, 1 IN
FFT BIN SHT. 5

DIC2U[0..9]
DIC3L[0..9]
DIC3U[0..9]

RACK 2 STATIONS 0 - 9 OUT
CHANNELS 4 - 7
PLAYBACK DRIVES 24, 1 - 13 IN
FFT BIN SHT. 5

DIC4L[0..9]
DIC4U[0..9]
DIC5L[0..9]
DIC5U[0..9]

RACK 3 STATIONS 10 - 19 OUT
CHANNELS 4 - 7
PLAYBACK DRIVES 12 - 24, 1 IN
FFT BIN SHT. 5

DIC6L[0..9]
DIC6U[0..9]
DIC7L[0..9]
DIC7U[0..9]

SINGLE ENDED
TO FFT CARDS

DIFFERENTIAL
FROM FFT CTRL
3M THRU DIN

GRP[1..96]
0STA[1..24]
1STA[1..24]
2STA[1..24]
3STA[1..24]

L025D13.sch

G0T[1..96]
G1T[1..96]
G2T[1..96]
G3T[1..96]
G4T[1..96]
G5T[1..96]
G0B[1..96]
G1B[1..96]
G2B[1..96]
G3B[1..96]
G4B[1..96]
G5B[1..96]
G0TL[1..96]
G1TL[1..96]
G2TL[1..96]
G3TL[1..96]
G4TL[1..96]
G5TL[1..96]
G0BL[1..96]
G1BL[1..96]
G2BL[1..96]
G3BL[1..96]
G4BL[1..96]
G5BL[1..96]

RACK0CTRLIN2 INT CYC ENA
RACK0CTRLIN[0..2]

STATIONS 0 - 19
CHANNELS 0 - 1
MAC BIN CABLING SHT. 15

CTRLIN[0..2]
0GRP[1..96]
1GRP[1..96]
2GRP[1..96]
3GRP[1..96]
4GRP[1..96]
DIVALST[0..9]
DIVAUST[0..9]
DIVBLST[0..9]
DIVBUST[0..9]
TIMETICK
VALC0A[1..24]
VALC1A[1..24]
VALA[1..24]
VALB[1..24]
CTRLOUT[0..2]

L025D15.SCH

STATIONS 0 - 19
CHANNELS 2 - 3
MAC BIN CABLING SHT. 15

VALC2A[1..24]
VALC3A[1..24]

STATIONS 0 - 19
CHANNELS 4 - 5
MAC BIN CABLING SHT. 15

VALC4A[1..24]
VALC5A[1..24]

STATIONS 0 - 19
CHANNELS 6 - 7
MAC BIN CABLING SHT. 15

VALC6A[1..24]
VALC7A[1..24]

L = STATIONS 0 - 9
U = STATIONS 10 - 19

SINGLE ENDED
DATA VALIDS
TO FFT CARDS

TO
FFT
BINS

FROM PBI BINS

VALP16[0..47]
VALP712[0..47]
VALP1318[0..47]
VALP1924[0..47]

SINGLE ENDED
FROM DF CARDS

PBD VALID SPLICE SHT. 21
L025D21.sch
TOTAL CRISS CROSS OF SIGNALS

VALC0A[1..24]
VALC1A[1..24]
VALC2A[1..24]
VALC3A[1..24]
VALC4A[1..24]
VALC5A[1..24]
VALC6A[1..24]
VALC7A[1..24]

TO MAC BINS
PBD VALIDS
BY CHANNELS

SINGLE ENDED
TO MASTER CONTROL CARD

M:\RACKWIRE\L025\L025D09.SCH

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
RACK INTERCONNECT

Size	Document Number	REV
D	56000L025 (L025D09.SCH)	
Date: June 17, 1997	Sheet 9 of	

SLIP ON RESISTORS

CLOCK DISTRIBUTION SEPARATE DRAWING

100 OHM

A1C0[0..1] A1C1[0..1] A1C2[0..1] A1C3[0..1] A1C0\[0..1] A1C1\[0..1] A1C2\[0..1] A1C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D04.SCH

100 OHM

A2C0[0..1] A2C1[0..1] A2C2[0..1] A2C3[0..1] A2C0\[0..1] A2C1\[0..1] A2C2\[0..1] A2C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D04.SCH

100 OHM

A3C0[0..1] A3C1[0..1] A3C2[0..1] A3C3[0..1] A3C0\[0..1] A3C1\[0..1] A3C2\[0..1] A3C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D04.SCH

100 OHM

A4C0[0..1] A4C1[0..1] A4C2[0..1] A4C3[0..1] A4C0\[0..1] A4C1\[0..1] A4C2\[0..1] A4C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D04.SCH

100 AND 300 OHM

A5C0[0..1] A5C1[0..1] A5C2[0..1] A5C3[0..1] A5C0\[0..1] A5C1\[0..1] A5C2\[0..1] A5C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D44.SCH

100 OHM

A6C0[0..1] A6C1[0..1] A6C2[0..1] A6C3[0..1] A6C0\[0..1] A6C1\[0..1] A6C2\[0..1] A6C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D04.SCH

100 OHM

A7C0[0..1] A7C1[0..1] A7C2[0..1] A7C3[0..1] A7C0\[0..1] A7C1\[0..1] A7C2\[0..1] A7C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D04.SCH

100 OHM

A8C0[0..1] A8C1[0..1] A8C2[0..1] A8C3[0..1] A8C0\[0..1] A8C1\[0..1] A8C2\[0..1] A8C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D04.SCH

100 OHM

A9C0[0..1] A9C1[0..1] A9C2[0..1] A9C3[0..1] A9C0\[0..1] A9C1\[0..1] A9C2\[0..1] A9C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D04.SCH

100 OHM

A10C0[0..1] A10C1[0..1] A10C2[0..1] A10C3[0..1] A10C0\[0..1] A10C1\[0..1] A10C2\[0..1] A10C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D04.SCH

100 AND 300 OHM

A11C0[0..1] A11C1[0..1] A11C2[0..1] A11C3[0..1] A11C0\[0..1] A11C1\[0..1] A11C2\[0..1] A11C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D44.SCH

100 AND 300 OHM

A12C0[0..1] A12C1[0..1] A12C2[0..1] A12C3[0..1] A12C0\[0..1] A12C1\[0..1] A12C2\[0..1] A12C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D44.SCH

100 AND 300 OHM

A13C0[0..1] A13C1[0..1] A13C2[0..1] A13C3[0..1] A13C0\[0..1] A13C1\[0..1] A13C2\[0..1] A13C3\[0..1]
A[0..1] B[0..1] C[0..1] D[0..1] A\[0..1] B\[0..1] C\[0..1] D\[0..1]

L025D44.SCH

SEE L025D07.SCH FOR CABLING BLOCK DIAGRAM

CARDS 0 THRU 4
5 FFT CARDS - SHEET 02

LDRAMA[0..4] LDRAM[0..4]
RAMCLKA[0..4] RAMCLK[0..4]
FRLOAD\A FRLOAD\
FRRW\A FRRW\
FRSIA[0..4] FRSI[0..4]
FRSRCLKA[0..4] FRSRCLK[0..4]
FSSRCLKA[0..4] FSSRCLK[0..4]
NEW FRA NEWFR
FSSI-A FSSIA024
FSSI-B FSSIB024
FSSI-C FSSIC024
SWAP FOR OTHER 5 CARDS FSSI-D FSSID024
FSSI-E FSSIA13
FSSI-F FSSIB13
FSSI-G FSSIC13
FSSI-H FSSID13
FSCLOAD\A FSCLOAD\
SIN/COS-A1[0..9] SIN/COS1[0..9]
SIN/COS-A2[0..9] SIN/COS2[0..9]
SIN/COS-A3U[0..9] SIN/COS3U[0..9]
SIN/COS-A3L[0..9] SIN/COS3L[0..9]
SIN/COS-A4U[0..9] SIN/COS4U[0..9]
SIN/COS-A4L[0..9] SIN/COS4L[0..9]
SC5-A2K[0..7] SC5-2K[0..7]
SC5-A<1K[0..8] SC5<1K[0..8]
PULSARA[0..3] PULSAR[0..3]
CRSI\A[0..4] CRSI\[0..4]
CRSFTCLKA[0..4] CRSFTCLK[0..4]
CRSTBA[0..3] CRSTB[0..4]
FFTINIT\A FFTINIT\
INIT\3A INIT\3`
INIT\4A INIT\4`
INIT\5A INIT\5`
A0C0[0..1] A0C1[0..1] A0C2[0..1] A0C3[0..1] A0C0\[0..1] A0C1\[0..1] A0C2\[0..1] A0C3\[0..1]
A1C0[0..1] A1C1[0..1] A1C2[0..1] A1C3[0..1] A1C0\[0..1] A1C1\[0..1] A1C2\[0..1] A1C3\[0..1]
A2C0[0..1] A2C1[0..1] A2C2[0..1] A2C3[0..1] A2C0\[0..1] A2C1\[0..1] A2C2\[0..1] A2C3\[0..1]
A3C0[0..1] A3C1[0..1] A3C2[0..1] A3C3[0..1] A3C0\[0..1] A3C1\[0..1] A3C2\[0..1] A3C3\[0..1]
A4C0[0..1] A4C1[0..1] A4C2[0..1] A4C3[0..1] A4C0\[0..1] A4C1\[0..1] A4C2\[0..1] A4C3\[0..1]
A5C0[0..1] A5C1[0..1] A5C2[0..1] A5C3[0..1] A5C0\[0..1] A5C1\[0..1] A5C2\[0..1] A5C3\[0..1]
A6C0[0..1] A6C1[0..1] A6C2[0..1] A6C3[0..1] A6C0\[0..1] A6C1\[0..1] A6C2\[0..1] A6C3\[0..1]
A7C0[0..1] A7C1[0..1] A7C2[0..1] A7C3[0..1] A7C0\[0..1] A7C1\[0..1] A7C2\[0..1] A7C3\[0..1]

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CARDS 5 THRU 9
5 FFT CARDS - SHEET 02

LDRAMB[0..4] LDRAM[0..4]
RAMCLKB[0..4] RAMCLK[0..4]
FRLOAD\B FRLOAD\
FRRW\B FRRW\
FRSIB[0..4] FRSI[0..4]
FRSRCLKB[0..4] FRSRCLK[0..4]
FSSRCLKB[0..4] FSSRCLK[0..4]
NEW FRB NEWFR
FSSI-E FSSIA024
FSSI-F FSSIB024
FSSI-G FSSIC024
SWAP FOR OTHER 5 CARDS FSSI-H FSSID024
FSSI-A FSSIA13
FSSI-B FSSIB13
FSSI-C FSSIC13
FSSI-D FSSID13
FSCLOAD\B FSCLOAD\
SIN/COS-B1[0..9] SIN/COS1[0..9]
SIN/COS-B2[0..9] SIN/COS2[0..9]
SIN/COS-B3U[0..9] SIN/COS3U[0..9]
SIN/COS-B3L[0..9] SIN/COS3L[0..9]
SIN/COS-B4U[0..9] SIN/COS4U[0..9]
SIN/COS-B4L[0..9] SIN/COS4L[0..9]
SC5-B2K[0..7] SC5-2K[0..7]
SC5-B<1K[0..8] SC5<1K[0..8]
PULSARB[0..3] PULSAR[0..3]
CRSI\B[0..4] CRSI\[0..4]
CRSFTCLKB[0..4] CRSFTCLK[0..4]
CRSTBB[0..3] CRSTB[0..4]
FFTINIT\B FFTINIT\
INIT\3B INIT\3`
INIT\4B INIT\4`
INIT\5B INIT\5`
A0C0[0..1] A0C1[0..1] A0C2[0..1] A0C3[0..1] A0C0\[0..1] A0C1\[0..1] A0C2\[0..1] A0C3\[0..1]
A1C0[0..1] A1C1[0..1] A1C2[0..1] A1C3[0..1] A1C0\[0..1] A1C1\[0..1] A1C2\[0..1] A1C3\[0..1]
A2C0[0..1] A2C1[0..1] A2C2[0..1] A2C3[0..1] A2C0\[0..1] A2C1\[0..1] A2C2\[0..1] A2C3\[0..1]
A3C0[0..1] A3C1[0..1] A3C2[0..1] A3C3[0..1] A3C0\[0..1] A3C1\[0..1] A3C2\[0..1] A3C3\[0..1]
A4C0[0..1] A4C1[0..1] A4C2[0..1] A4C3[0..1] A4C0\[0..1] A4C1\[0..1] A4C2\[0..1] A4C3\[0..1]
A5C0[0..1] A5C1[0..1] A5C2[0..1] A5C3[0..1] A5C0\[0..1] A5C1\[0..1] A5C2\[0..1] A5C3\[0..1]
A6C0[0..1] A6C1[0..1] A6C2[0..1] A6C3[0..1] A6C0\[0..1] A6C1\[0..1] A6C2\[0..1] A6C3\[0..1]
A7C0[0..1] A7C1[0..1] A7C2[0..1] A7C3[0..1] A7C0\[0..1] A7C1\[0..1] A7C2\[0..1] A7C3\[0..1]

L025D02.SCH

FFT CTRL CARD

7J1C

GND	1	
B-ENA\	2	
VCC	3	
SC5-B2K0	4	
SC5-B2K3	5	
SC5-B2K6	6	
SC5-B<1K2	7	
SC5-B<1K5	8	
SC5-B<1K8	9	
SIN/COS-B4U0	10	
SIN/COS-B4U1	11	
SIN/COS-B4U2	12	
SIN/COS-B4U3	13	
SIN/COS-B4U4	14	
SIN/COS-B4U5	15	
SIN/COS-B4U6	16	
SIN/COS-B4U7	17	
SIN/COS-B4U8	18	
SIN/COS-B4U9	19	
CRSI\A	20	
SC5-A2K0	21	
SC5-A2K3	22	
SC5-A2K6	23	
SC5-A<1K2	24	
SC5-A<1K5	25	
SC5-A<1K8	26	
CRSTBB	27	
	28	
SIN/COS-B3L6	29	
VCC	30	
SIN/COS-B3L9	31	
GND	32	

DIN

7J1B

GND	1	
C16.0 OFF C16.0 IN	2	
VCC	3	
SC5-B2K2	4	
SC5-B2K5	5	
A-ENA\	6	
SC5-B<1K1	7	
SC5-B<1K4	8	
SC5-B<1K7	9	
SIN/COS-B4L0	10	
SIN/COS-B4L1	11	
SIN/COS-B4L2	12	
SIN/COS-B3U0	13	
SIN/COS-B3U1	14	
SIN/COS-B3U2	15	
SIN/COS-B3U3	16	
SIN/COS-B3U4	17	
SIN/COS-B3U5	18	
SIN/COS-B3U6	19	
SIN/COS-B3U7	20	
SC5-A2K2	21	
SC5-A2K5	22	
CRSI\B	23	
SC5-A<1K1	24	
SC5-A<1K4	25	
SC5-A<1K7	26	
SIN/COS-B3L3	27	
	28	
SIN/COS-B3L5	29	
VCC	30	
SIN/COS-B3L8	31	
GND	32	

DIN

FFT CTRL CARD

7J1A

GND	1	
C16.0 OFF	2	
VCC	3	
SC5-B2K1	4	
SC5-B2K4	5	
SC5-B2K7	6	
SC5-B<1K0	7	
SC5-B<1K3	8	
SC5-B<1K6	9	
SIN/COS-B4L3	10	
SIN/COS-B4L4	11	
SIN/COS-B4L5	12	
SIN/COS-B4L6	13	
SIN/COS-B4L7	14	
SIN/COS-B4L8	15	
SIN/COS-B4L9	16	
SIN/COS-B3U8	17	
SIN/COS-B3U9	18	
SIN/COS-B3L0	19	
SIN/COS-B3L1	20	
SC5-A2K1	21	
SC5-A2K4	22	
SC5-A2K7	23	
SC5-A<1K0	24	
SC5-A<1K3	25	
SC5-A<1K6	26	
SIN/COS-B3L2	27	
CRSTBA	28	
SIN/COS-B3L4	29	
VCC	30	
SIN/COS-B3L7	31	
GND	32	

DIN

TO uP CARD

7J2C

GND	1	
PULSARA3	2	
VCC	3	
INIT\5A	4	
PULSARA0	5	
FSSRCLK-A	6	
FSSRCLK-B	7	
FSSRCLK-C	8	
FSSRCLK-D	9	
FSSRCLK-E	10	
RAMCLKB	11	
RAMCLKA	12	
SIN/COS-A4U0	13	
SIN/COS-A4U1	14	
SIN/COS-A4U2	15	
SIN/COS-A4U3	16	
SIN/COS-A4U4	17	
SIN/COS-A4U5	18	
SIN/COS-A4U6	19	
SIN/COS-A4U7	20	
SIN/COS-A4U8	21	
ECL CLK32	22	
ECL CLK32\	23	
SIN/COS-A20	24	
SIN/COS-A21	25	
SIN/COS-A22	26	
SIN/COS-A23	27	
VEE	28	
SIN/COS-A26	29	
	30	
SIN/COS-A29	31	
GND	32	

DIN

7J2B

GND	1	
PULSARA2	2	
VCC	3	
SIN/COS-A4L0	4	
SIN/COS-A4L1	5	
SIN/COS-A4L2	6	
SIN/COS-A3L0	7	
SIN/COS-A3L1	8	
SIN/COS-A3L2	9	
SIN/COS-A3L3	10	
SIN/COS-A3L4	11	
SIN/COS-A3L5	12	
SIN/COS-A3L6	13	
SIN/COS-A3L7	14	
SIN/COS-A3L8	15	
SIN/COS-A3L9	16	
SIN/COS-A4U9	17	
FRSIB	18	
FRSIA	19	
INIT\3A	20	
INIT\4A	21	
INIT\3B	22	
INIT\4B	23	
NEW FRA	24	
NEW FRB	25	
FFTINIT\B	26	
FFTINIT\A	27	
VEE	28	
SIN/COS-A25	29	
VCC	30	
SIN/COS-A28	31	
GND	32	

DIN

VEE

7J2A

GND	1	
PULSARA1	2	
VCC	3	
SIN/COS-A4L3	4	
SIN/COS-A4L4	5	
SIN/COS-A4L5	6	
SIN/COS-A4L6	7	
SIN/COS-A4L7	8	
SIN/COS-A4L8	9	
SIN/COS-A4L9	10	
SIN/COS-A3U0	11	
SIN/COS-A3U1	12	
SIN/COS-A3U2	13	
SIN/COS-A3U3	14	
SIN/COS-A3U4	15	
SIN/COS-A3U5	16	
SIN/COS-A3U6	17	
SIN/COS-A3U7	18	
SIN/COS-A3U8	19	
SIN/COS-A3U9	20	
FSCLOAD\A	21	
FSCLOAD\B	22	
INIT\5B	23	
PULSARB0	24	
PULSARB1	25	
PULSARB2	26	
PULSARB3	27	
VEE	28	
SIN/COS-A24	29	
VCC	30	
SIN/COS-A27	31	
GND	32	

DIN

7J3C

GND	1	
SIN/COS-A10	2	
VCC	3	
SIN/COS-B10	4	
	5	
SIN/COS-B11	6	
SIN/COS-B12	7	
SIN/COS-A11	8	
SIN/COS-A12	9	
	10	
SIN/COS-B13	11	
SIN/COS-B14	12	
SIN/COS-A13	13	
SIN/COS-A14	14	
	15	
SIN/COS-B15	16	
SIN/COS-B16	17	
SIN/COS-A15	18	
SIN/COS-A16	19	
	20	
SIN/COS-B17	21	
SIN/COS-B18	22	
SIN/COS-B19	23	
SIN/COS-A17	24	
SIN/COS-A18	25	
	26	
SIN/COS-A19	27	
VCC	28	
FSSI-E	29	
GND	30	
	31	
	32	

DIN

7J3B

GND	1	
FRRW\A	2	
VCC	3	
FRRW\B	4	
SIN/COS-B20	5	
SIN/COS-B21	6	
SIN/COS-B22	7	
SIN/COS-B23	8	
SIN/COS-B24	9	
LDRAMA0 LDRAM0	10	
LDRAMA1 LDRAM1	11	
LDRAMA2 LDRAM2	12	
LDRAMA3 LDRAM3	13	
LDRAMA4 LDRAM4	14	
LDRAMB0 LDRAM5	15	
LDRAMB1 LDRAM6	16	
LDRAMB2 LDRAM7	17	
LDRAMB3 LDRAM8	18	
LDRAMB4 LDRAM9	19	
FRSRCLKB0 FRSRCLK5	20	
FRSRCLKB1 FRSRCLK6	21	
FRSRCLKB2 FRSRCLK7	22	
FRSRCLKB3 FRSRCLK8	23	
FRSRCLKB4 FRSRCLK9	24	
NEWFRINGE FSSI-G	25	
FSSI-H	26	
	27	
FSSI-B	28	
VCC	29	
FSSI-D	30	
GND	31	
	32	

DIN

VCC

7J3A

GND	1	
FRLOAD\A	2	
VCC	3	
FRLOAD\B	4	
SIN/COS-B25	5	
SIN/COS-B26	6	
SIN/COS-B27	7	
SIN/COS-B28	8	
SIN/COS-B29	9	
CRSFTCLKA0 CRSFTCLK0	10	
CRSFTCLKA1 CRSFTCLK1	11	
CRSFTCLKA2 CRSFTCLK2	12	
CRSFTCLKA3 CRSFTCLK3	13	
CRSFTCLKA4 CRSFTCLK4	14	
CRSFTCLKB0 CRSFTCLK5	15	
CRSFTCLKB1 CRSFTCLK6	16	
CRSFTCLKB2 CRSFTCLK7	17	
CRSFTCLKB3 CRSFTCLK8	18	
CRSFTCLKB4 CRSFTCLK9	19	
FRSRCLKA0 FRSRCLK0	20	
FRSRCLKA1 FRSRCLK1	21	
FRSRCLKA2 FRSRCLK2	22	
FRSRCLKA3 FRSRCLK3	23	
FRSRCLKA4 FRSRCLK4	24	
ECLFFTINIT\	25	
ECLFFTINIT	26	
FSSI-F	27	
	28	
FSSI-A	29	
VCC	30	
FSSI-C	31	
GND	32	

DIN

BACKPLANE BUFFER BOARDS

CRSI\A CRSI\B → CRSI\A CRSI\B → CRSI\A[0..4] CRSI\B[0..4]
CRSTBA CRSTBB → CRSTBA CRSTBB → CRSTBA[0..4] CRSTBB[0..4]
RAMCLKA RAMCLKB → RAMCLKA RAMCLKB → RAMCLKA[0..4] RAMCLKB[0..4]
FRSIA FRSIB → FRSIA FRSIB → FRSIA[0..4] FRSIB[0..4]

L025D40.SCH

SEE L025D45.SCH FOR RACKS 0 AND 1.
SEE L025D05 FOR CABLING TOP LEVEL

FFT CARDS 0-4

FSSRCLK-A	FSSRCLKA0
FSSRCLK-A	FSSRCLKA1
FSSRCLK-B	FSSRCLKA2
FSSRCLK-B	FSSRCLKA3
FSSRCLK-C	FSSRCLKA4

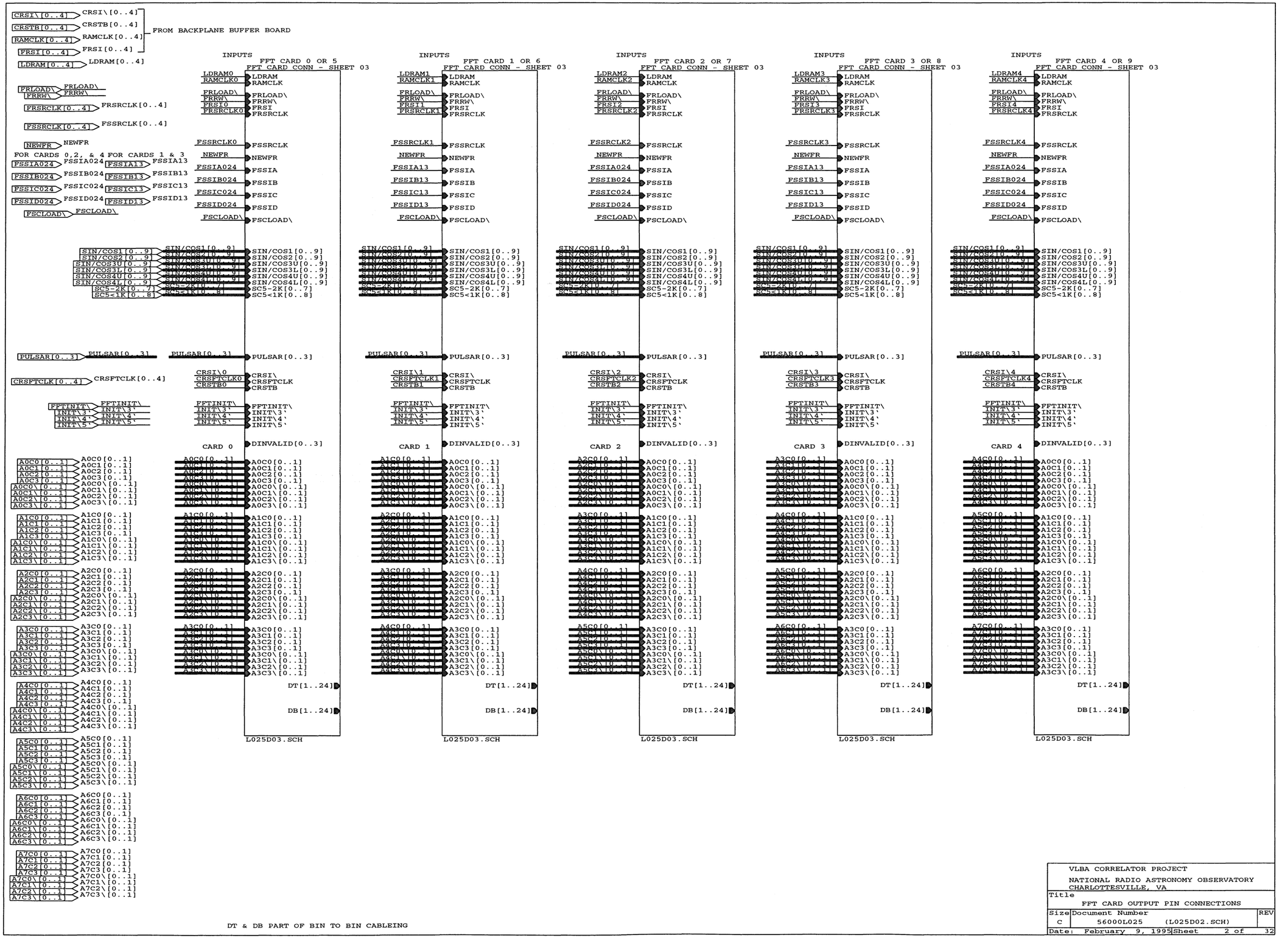
FFT CARDS 5-9

FSSRCLK-C	FSSRCLKB0
FSSRCLK-D	FSSRCLKB1
FSSRCLK-D	FSSRCLKB2
FSSRCLK-E	FSSRCLKB3
FSSRCLK-E	FSSRCLKB4

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: FFT BIN (RACKS 2 AND 3)

Size	Document Number	REV
C	56000L025 (L025D01.SCH)	
Date: July 23, 1996	Sheet 1 of 32	


CRSI\[0..4]
CRSTB[0..4]
RAMCLK[0..4]
FRSI[0..4]
LDRAM[0..4]
FROM BACKPLANE BUFFER BOARD
FRLOAD\
FRRW\
FRSRCLK[0..4]
FSSRCLK[0..4]
NEWFR
FOR CARDS 0,2, & 4 FOR CARDS 1 & 3
FSSIA024
FSSIA13
FSSIB024
FSSIB13
FSSIC024
FSSIC13
FSSID024
FSSID13
FSCLOAD\
SIN/COS1[0..9]
SIN/COS2[0..9]
SIN/COS3U[0..9]
SIN/COS3L[0..9]
SIN/COS4U[0..9]
SIN/COS4L[0..9]
SC5-2K[0..7]
SC5<1K[0..8]
PULSAR[0..3]
CRSFTCLK[0..4]
FFTINIT\
INIT\3`
INIT\4`
INIT\5`
A0C0[0..1]
A0C1[0..1]
A0C2[0..1]
A0C3[0..1]
A0C0\[0..1]
A0C1\[0..1]
A0C2\[0..1]
A0C3\[0..1]
A1C0[0..1]
A1C1[0..1]
A1C2[0..1]
A1C3[0..1]
A1C0\[0..1]
A1C1\[0..1]
A1C2\[0..1]
A1C3\[0..1]
A2C0[0..1]
A2C1[0..1]
A2C2[0..1]
A2C3[0..1]
A2C0\[0..1]
A2C1\[0..1]
A2C2\[0..1]
A2C3\[0..1]
A3C0[0..1]
A3C1[0..1]
A3C2[0..1]
A3C3[0..1]
A3C0\[0..1]
A3C1\[0..1]
A3C2\[0..1]
A3C3\[0..1]
A4C0[0..1]
A4C1[0..1]
A4C2[0..1]
A4C3[0..1]
A4C0\[0..1]
A4C1\[0..1]
A4C2\[0..1]
A4C3\[0..1]
A5C0[0..1]
A5C1[0..1]
A5C2[0..1]
A5C3[0..1]
A5C0\[0..1]
A5C1\[0..1]
A5C2\[0..1]
A5C3\[0..1]
A6C0[0..1]
A6C1[0..1]
A6C2[0..1]
A6C3[0..1]
A6C0\[0..1]
A6C1\[0..1]
A6C2\[0..1]
A6C3\[0..1]
A7C0[0..1]
A7C1[0..1]
A7C2[0..1]
A7C3[0..1]
A7C0\[0..1]
A7C1\[0..1]
A7C2\[0..1]
A7C3\[0..1]
DT & DB PART OF BIN TO BIN CABLEING
INPUTS
FFT CARD 0 OR 5
FFT CARD CONN - SHEET 03
LDRAM0
RAMCLK0
FRSRCLK0
CRSTB0
CARD 0
DINVALID[0..3]
DT[1..24]
DB[1..24]
L025D03.SCH
INPUTS
FFT CARD 1 OR 6
FFT CARD CONN - SHEET 03
LDRAM1
RAMCLK1
FRSRCLK1
CRSTB1
CARD 1
DINVALID[0..3]
DT[1..24]
DB[1..24]
L025D03.SCH
INPUTS
FFT CARD 2 OR 7
FFT CARD CONN - SHEET 03
LDRAM2
RAMCLK2
FRSRCLK2
CRSTB2
CARD 2
DINVALID[0..3]
DT[1..24]
DB[1..24]
L025D03.SCH
INPUTS
FFT CARD 3 OR 8
FFT CARD CONN - SHEET 03
LDRAM3
RAMCLK3
FRSRCLK3
CRSTB3
CARD 3
DINVALID[0..3]
DT[1..24]
DB[1..24]
L025D03.SCH
INPUTS
FFT CARD 4 OR 9
FFT CARD CONN - SHEET 03
LDRAM4
RAMCLK4
FRSRCLK4
CRSTB4
CARD 4
DINVALID[0..3]
DT[1..24]
DB[1..24]
L025D03.SCH
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title
FFT CARD OUTPUT PIN CONNECTIONS
Size C
Document Number 56000L025 (L025D02.SCH)
REV
Date: February 9, 1995
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TWISTED PAIRS

A0C0[0..1] A0C1[0..1] A0C2[0..1] A0C3[0..1] A0C0\[0..1] A0C1\[0..1] A0C2\[0..1] A0C3\[0..1]

A1C0[0..1] A1C1[0..1] A1C2[0..1] A1C3[0..1] A1C0\[0..1] A1C1\[0..1] A1C2\[0..1] A1C3\[0..1]

A2C0[0..1] A2C1[0..1] A2C2[0..1] A2C3[0..1] A2C0\[0..1] A2C1\[0..1] A2C2\[0..1] A2C3\[0..1]

A3C0[0..1] A3C1[0..1] A3C2[0..1] A3C3[0..1] A3C0\[0..1] A3C1\[0..1] A3C2\[0..1] A3C3\[0..1]

FRLOAD FRLOAD\

CRSI CRSI\

INIT\3` INIT\3`
FSSRCLK FSSRCLK

FRSRCLK FRSRCLK

FRSI FRSI
FSSIA FSSIA
FSSIB FSSIB
FSSIC FSSIC
FSSID FSSID

CRSFTCLK CRSFTCLK

CRSTB CRSTB

FFTINIT\ FFTINIT\

LDRAM LDRAM
RAMCLK RAMCLK

PULSAR[0..3] PULSAR[0..3]

INIT\5` INIT\5`
FSCLOAD\ FSCLOAD\

SIN/COS4U[0..9] SIN/COS4U[0..9]
SIN/COS4L[0..9] SIN/COS4L[0..9]

SC5-2K[0..7] SC5-2K[0..7]
SC5<1K[0..8] SC5<1K[0..8]

SIN/COS1[0..9] SIN/COS1[0..9]
SIN/COS2[0..9] SIN/COS2[0..9]
SIN/COS3U[0..9] SIN/COS3U[0..9]
SIN/COS3L[0..9] SIN/COS3L[0..9]

DINVALID[0..3] DINVALID[0..3]

NEWFR NEWFR

FRRW\ FRRW\

INIT\4` INIT\4`

FOR DT & DB:

THE 1ST COLUMN IS COMMENTS CORRESPONDING TO SIGNAL NAMES ON THE FFT CARD.

THE 2ND COLUMN IS LABELS CORRESPONDING TO PIN NAMES ON THE 2 CONNECTORS.

2, 24 PIN CONNECTORS

P1C

1	GND	
2		
3	VCC	
4	DT2	DT17
5	DT\2	DT18
6	DT5	DT19
7	DT\5	DT20
8	DT8	DT21
9	DT\8	DT22
10	DT11	DT23
11	DT\11	DT24
12	DB2	DB17
13	DB\2	DB18
14	DB5	DB19
15	DB\5	DB20
16	DB8	DB21
17	DB\8	DB22
18	DB11	DB23
19	DB\11	DB24
20	CRST\	
21	SC5-2K0	
22	SC5-2K3	
23	SC5-2K6	
24	SC5<1K2	
25	SC5<1K5	
26	SC5<1K8	
27	CRSTB	
28	VEE	
29		
30	VCC	
31		
32	GND	

DIN

P1B

1	GND	
2		
3	VCC	
4	DT1	DT9
5	DT\1	DT10
6	DT4	DT11
7	DT\4	DT12
8	DT7	DT13
9	DT\7	DT14
10	DT10	DT15
11	DT\10	DT16
12	DB1	DB9
13	DB\1	DB10
14	DB4	DB11
15	DB\4	DB12
16	DB7	DB13
17	DB\7	DB14
18	DB10	DB15
19	DB\10	DB16
20	ADR\0	
21	SC5-2K2	
22	SC5-2K5	
23		
24	SC5<1K1	
25	SC5<1K4	
26	SC5<1K7	
27	CRSO\	
28	VEE	
29		
30	VCC	
31		
32	GND	

DIN

P1A

1	GND	
2		
3	VCC	
4	DT0	DT1
5	DT\0	DT2
6	DT3	DT3
7	DT\3	DT4
8	DT6	DT5
9	DT\6	DT6
10	DT9	DT7
11	DT\9	DT8
12	DB0	DB1
13	DB\0	DB2
14	DB3	DB3
15	DB\3	DB4
16	DB6	DB5
17	DB\6	DB6
18	DB9	DB7
19	DB\9	DB8
20	ADR\1	
21	SC5-2K1	
22	SC5-2K4	
23	SC5-2K7	
24	SC5<1K0	
25	SC5<1K3	
26	SC5<1K6	
27	CRSFTCLK	VEE
28	VEE	
29	VCC	VCC
30		
31	VCC	
32	GND	

DIN

P2C

1	GND	
2	PULSAR3	
3	VCC	
4	INIT\5`	U73
5	PULSAR0	
6	DINVALID0	
7	DINVALID1	
8	DINVALID2	
9	DINVALID3	
10	FSSRCLK	
11	LDRAM	U121
12	RAMCLK	
13	SIN/COS4U0	
14	SIN/COS4U1	
15	SIN/COS4U2	
16	SIN/COS4U3	
17	SIN/COS4U4	U71
18	SIN/COS4U5	
19	SIN/COS4U6	
20	SIN/COS4U7	
21	SIN/COS4U8	
22	C32ECL	
23	C32ECL\	
24	SIN/COS20	U43
25	SIN/COS21	
26	SIN/COS22	
27	SIN/COS23	
28	VEE	
29	SIN/COS26	
30	VCC	U43
31	SIN/COS29	
32	GND	

DIN

P2B

1	GND	
2	PULSAR2	
3	VCC	
4	SIN/COS4L0	
5	SIN/COS4L1	U72
6	SIN/COS4L2	
7	SIN/COS3L0	
8	SIN/COS3L1	
9	SIN/COS3L2	
10	SIN/COS3L3	
11	SIN/COS3L4	U45
12	SIN/COS3L5	
13	SIN/COS3L6	
14	SIN/COS3L7	
15	SIN/COS3L8	
16	SIN/COS3L9	
17	SIN/COS4U9	U71
18	GND	
19	FRSI	U24
20	INIT\3`	
21	INIT\4`	
22		
23	FRSRCLK	
24	NEWFR	
25	FSST\	
26	FSRW\	
27	FFTINIT\	
28	VEE	
29	SIN/COS25	
30	VCC	
31	SIN/COS28	
32	GND	

DIN

P2A

1	GND	
2	PULSAR1	
3	VCC	
4	SIN/COS4L3	
5	SIN/COS4L4	U72
6	SIN/COS4L5	
7	SIN/COS4L6	
8	SIN/COS4L7	
9	SIN/COS4L8	
10	SIN/COS4L9	
11	SIN/COS3U0	
12	SIN/COS3U1	
13	SIN/COS3U2	
14	SIN/COS3U3	
15	SIN/COS3U4	U44
16	SIN/COS3U5	
17	SIN/COS3U6	
18	SIN/COS3U7	
19	SIN/COS3U8	
20	SIN/COS3U9	
21	FSCLOAD\	
22	FRSO\	
23		
24	EXPOF\`0	U17
25	EXPOF\`1	
26	EXPOF\`2	
27	EXPOF\`3	
28	VEE	
29	SIN/COS24	
30	VCC	
31	SIN/COS27	
32	GND	

DIN

P3C

1	GND	
2	SIN/COS10	
3	VCC	
4	A0C21	
5	A0C2\1	
6	A0C10	
7	A0C1\0	
8	SIN/COS11	
9	SIN/COS12	
10	A1C21	
11	A1C2\1	
12	A1C10	
13	A1C1\0	
14	SIN/COS13	
15	SIN/COS14	
16	A2C21	
17	A2C2\1	
18	A2C10	
19	A2C1\0	
20	SIN/COS15	
21	SIN/COS16	
22	A3C21	
23	A3C2\1	
24	A3C10	
25	A3C1\0	
26	SIN/COS17	
27	SIN/COS18	
28	VEE	
29	SIN/COS19	
30	VCC	
31		
32	GND	

DIN

P3B

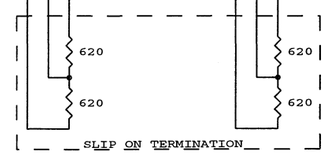
1	GND	
2	FRRW\	
3	VCC	
4	A0C30	
5	A0C3\0	
6	A0C11	
7	A0C1\1	
8	A0C00	
9	A0C0\0	
10	A1C30	
11	A1C3\0	
12	A1C11	
13	A1C1\1	
14	A1C00	
15	A1C0\0	
16	A2C30	
17	A2C3\0	
18	A2C11	
19	A2C1\1	
20	A2C00	
21	A2C0\0	
22	A3C30	
23	A3C3\0	
24	A3C11	
25	A3C1\1	
26	A3C00	
27	A3C0\0	
28	VEE	
29	FSSIB	
30	VCC	
31	FSSID	
32	GND	

DIN

P3A

1	GND	
2	FRLOAD\	
3	VCC	
4	A0C31	
5	A0C3\1	
6	A0C20	
7	A0C2\0	
8	A0C01	
9	A0C0\1	
10	A1C31	
11	A1C3\1	
12	A1C20	
13	A1C2\0	
14	A1C01	
15	A1C0\1	
16	A2C31	
17	A2C3\1	
18	A2C20	
19	A2C2\0	
20	A2C01	
21	A2C0\1	
22	A3C31	
23	A3C3\1	
24	A3C20	
25	A3C2\0	
26	A3C01	
27	A3C0\1	
28	VEE	
29	FSSIA	
30	VCC	
31	FSSIC	
32	GND	

DIN



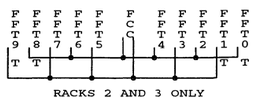
SLIP ON TERMINATION

FOR USE ONLY ON THE FOLLOWING CARDS:

RACK 2 FFT 0	RACK 3 FFT 0
RACK 2 FFT 1	RACK 3 FFT 1
RACK 2 FFT 8	RACK 3 FFT 8
RACK 2 FFT 9	RACK 3 FFT 9

RACKS 0 AND 1 DO NOT NEED THESE TERMINATIONS, SINCE THEY WERE REWIRED WITH THE FSTC BUFFER BOARDS.

THIS PROVIDES TERMINATIONS FOR THE TWO FSSI BUSSES AS DIAGRAMED BELOW:
T INDICATES A TERMINATION.



RACKS 2 AND 3 ONLY

DT[1..24] DT[1..24]

DB[1..24] DB[1..24]

BUSSES CORRESPONDING TO A CONNECTOR AND CABLE.

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: FFT CARD CONNECTOR

Size	Document Number	REV
C	56000L025 (RACKWIRE/L025D03.SCH)	

Date: July 23, 1996 Sheet 3 of 32

A[0..1] A[0..1]

B[0..1] B[0..1]

C[0..1] C[0..1]

D[0..1] D[0..1]

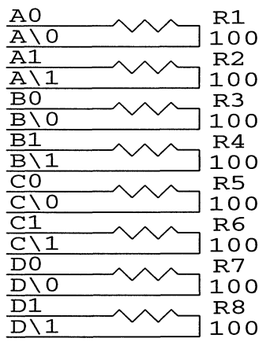
A\[0..1] A\[0..1]

B\[0..1] B\[0..1]

C\[0..1] C\[0..1]

D\[0..1] D\[0..1]

SLIP ON FIXTURE
ON FFT CARD CONNECTOR.



VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title 100 OHM TERMINATING RESISTORS		
Size A	Document Number 56000L025 (L025D04.SCH)	REV
Date: December 7, 1995	Sheet 4 of	

CRSI\B[0..4] — CRSI\B[0..4]

CRSTBB[0..4] — CRSTBB[0..4]

RAMCLKB[0..4] — RAMCLKB[0..4]

FRSIB[0..4] — FRSIB[0..4]

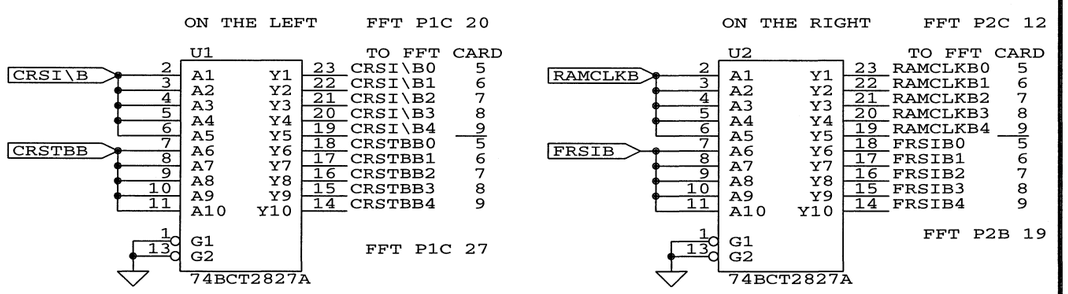
CRSI\A[0..4] — CRSI\A[0..4]

CRSTBA[0..4] — CRSTBA[0..4]

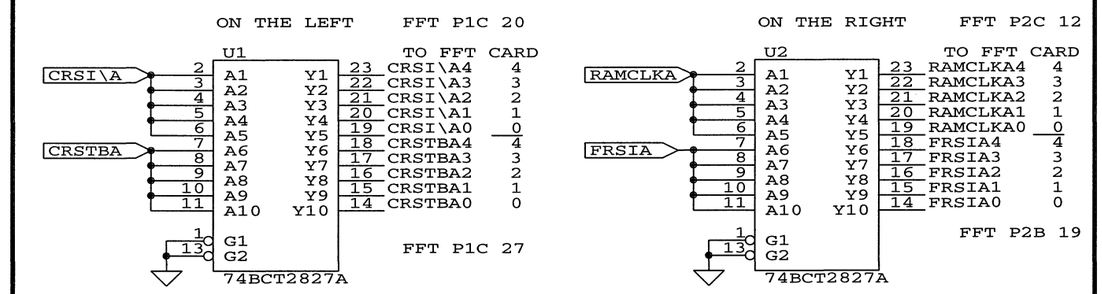
RAMCLKA[0..4] — RAMCLKA[0..4]

FRSIA[0..4] — FRSIA[0..4]

BACKPLANE BUFFER BOARD ON THE LEFT



BACKPLANE BUFFER BOARD ON THE RIGHT



USED ON FFT BIN BACKPLANE FOR BUFFERING
THE FOLLOWING SIGNALS,
FROM THE FCC TO FFT BOARDS:
CRSI\, CRSTB, FRSI, RAMCLK

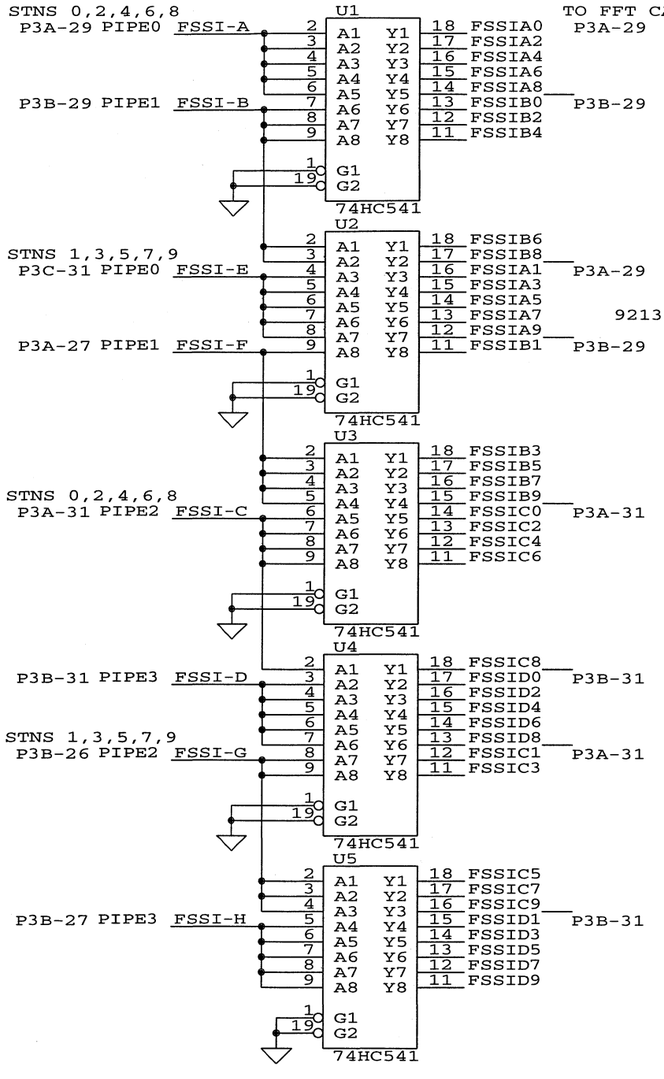
THESE BOARDS ARE BOLTED TO THE BACKPLANE.
THE WIRING IS REPEATED IN EACH RACK.

M:\RACKWIRE\L025\SCCS

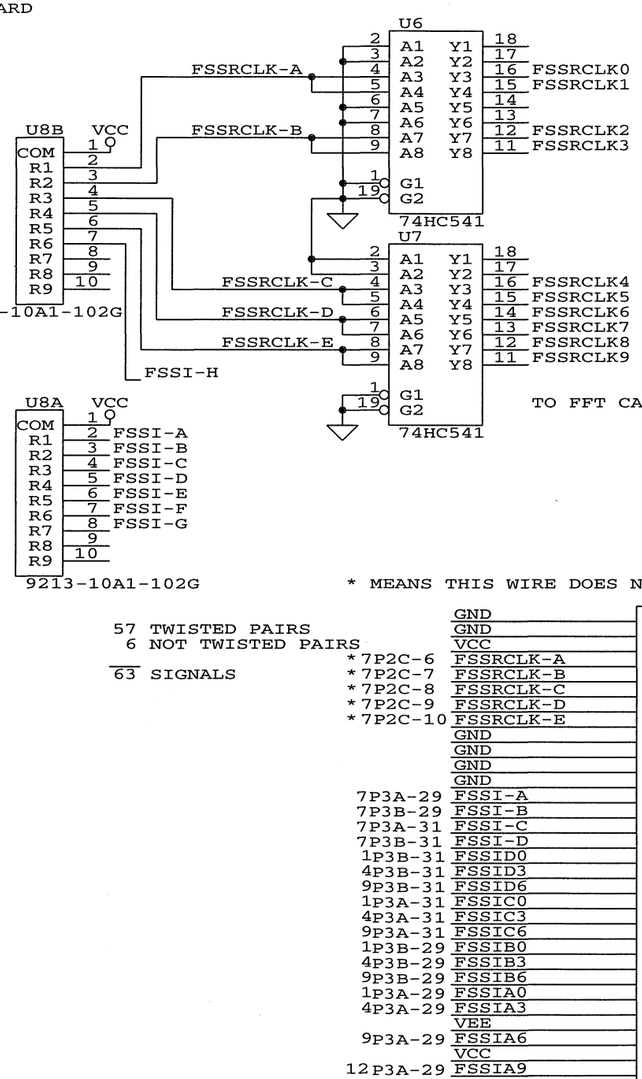
NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NM		
Title BACKPLANE BUFFER BOARD		
Size B	Document Number 56000L025 (L025D40.SCH)	REV
Date: February 9, 1995	Sheet of	

FROM FCC

NUMBER REPRESENTS FFT CARD
ABCD REPRESENT PIPELINES 0123

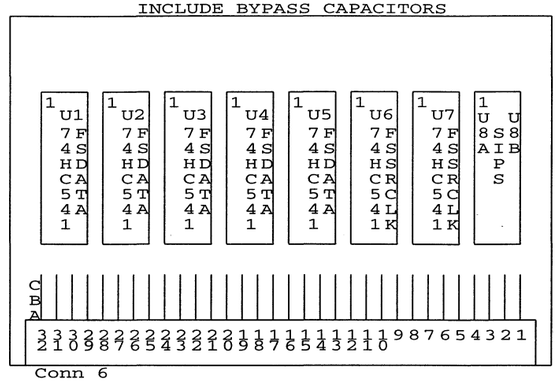


TO FFT CARD
P3A-29
P3B-29
P3A-29
P3B-29
P3A-31
P3B-31
P3A-31
P3B-31



TO FFT CARDS P2C-10

INCLUDE BYPASS CAPACITORS



* MEANS THIS WIRE DOES NOT HAVE TO BE A TWISTED PAIR, SINCE IT IS A SHORT RUN.

57 TWISTED PAIRS
6 NOT TWISTED PAIRS

63 SIGNALS

6P2A		6P2B		6P2C	
GND	1	GND	1	GND	1
GND	2	GND	2	GND	2
VCC	3	VCC	3	VCC	3
*7P2C-6 FSSRCLK-A	4	1P2C-10 FSSRCLK0	4	8P2C-10 FSSRCLK5	4
*7P2C-7 FSSRCLK-B	5	2P2C-10 FSSRCLK1	5	9P2C-10 FSSRCLK6	5
*7P2C-8 FSSRCLK-C	6	3P2C-10 FSSRCLK2	6	10P2C-10 FSSRCLK7	6
*7P2C-9 FSSRCLK-D	7	4P2C-10 FSSRCLK3	7	11P2C-10 FSSRCLK8	7
*7P2C-10 FSSRCLK-E	8	*5P2C-10 FSSRCLK4	8	12P2C-10 FSSRCLK9	8
GND	9	GND	9	GND	9
GND	10	GND	10	GND	10
GND	11	GND	11	GND	11
GND	12	GND	12	GND	12
7P3A-29 FSSI-A	13		13	7P3C-31 FSSI-E	13
7P3B-29 FSSI-B	14		14	7P3A-27 FSSI-F	14
7P3A-31 FSSI-C	15		15	7P3B-26 FSSI-G	15
7P3B-31 FSSI-D	16	12P3B-31 FSSID9	16	7P3B-27 FSSI-H	16
1P3B-31 FSSID0	17	2P3B-31 FSSID1	17	3P3B-31 FSSID2	17
4P3B-31 FSSID3	18	5P3B-31 FSSID4	18	8P3B-31 FSSID5	18
9P3B-31 FSSID6	19	10P3B-31 FSSID7	19	11P3B-31 FSSID8	19
1P3A-31 FSSIC0	20	2P3A-31 FSSIC1	20	3P3A-31 FSSIC2	20
4P3A-31 FSSIC3	21	5P3A-31 FSSIC4	21	8P3A-31 FSSIC5	21
9P3A-31 FSSIC6	22	10P3A-31 FSSIC7	22	11P3A-31 FSSIC8	22
1P3B-29 FSSIB0	23	2P3B-29 FSSIB1	23	3P3B-29 FSSIB2	23
4P3B-29 FSSIB3	24	5P3B-29 FSSIB4	24	8P3B-29 FSSIB5	24
9P3B-29 FSSIB6	25	10P3B-29 FSSIB7	25	11P3B-29 FSSIB8	25
1P3A-29 FSSIA0	26	2P3A-29 FSSIA1	26	3P3A-29 FSSIA2	26
4P3A-29 FSSIA3	27	5P3A-29 FSSIA4	27	8P3A-29 FSSIA5	27
VEE	28	VEE	28	VEE	28
9P3A-29 FSSIA6	29	10P3A-29 FSSIA7	29	11P3A-29 FSSIA8	29
VCC	30	VCC	30	VCC	30
12P3A-29 FSSIA9	31	12P3B-29 FSSIB9	31	12P3A-31 FSSIC9	31
GND	32	GND	32	GND	32
DIN		DIN		DIN	

SLOT	CARD
1	FFT 0
2	FFT 1
3	FFT 2
4	FFT 3
5	FFT 4
6	BUFFER BOARD & CABLES TO THE TOP OF FCC
7	FCC
8	FFT 5
9	FFT 6
10	FFT 7
11	FFT 8
12	FFT 9

SEE RACKWIRE/FSTC.TXT FOR IMPLEMENTATION STRATEGY.
TO BE MOUNTED ON THE CENTER DIN NEXT TO THE FCC

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
FSTC BUFFER BOARD

Size	Document Number	REV
B	56000L025 (RACKWIRE/L025D42.SCH)	

Date: September 11, 1995 Sheet 1 of 32

SLIP ON RESISTORS

CLOCK DISTRIBUTION SEPARATE DRAWING

100 OHM

L025D04.SCH 100 OHM

L025D04.SCH 100 OHM

L025D04.SCH 100 OHM

L025D04.SCH 100 AND 300 OHM

L025D44.SCH 100 OHM

L025D04.SCH 100 OHM

L025D04.SCH 100 OHM

L025D04.SCH 100 OHM

L025D04.SCH 100 AND 300 OHM

L025D44.SCH 100 AND 300 OHM

L025D44.SCH 100 AND 300 OHM

L025D44.SCH

SEE L025D07.SCH FOR CABLING BLOCK DIAGRAM

CARDS 0 THRU 4
5 FFT CARDS

CARDS 5 THRU 9
5 FFT CARDS

L025D46.SCH

L025D46.SCH

FSTC BUFFER BOARD
RACKS 0 AND 1 ONLY
SEE L025D42.SCH FOR SCHEMATIC

FFT CTRL CARD

FFT CTRL CARD

TO uP CARD

BACKPLANE BUFFER BOARDS

L025D40.SCH

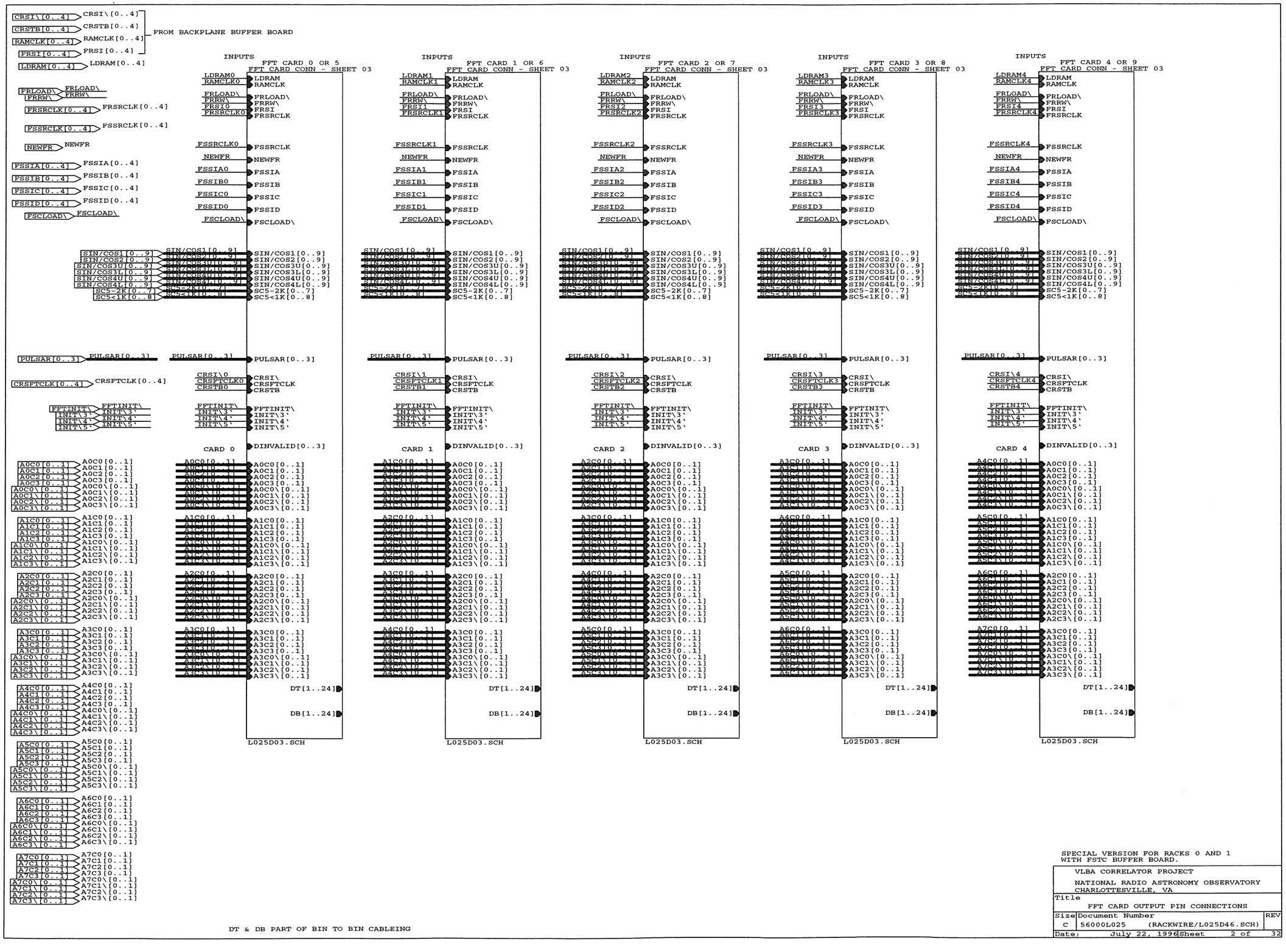
SLOT	CARD
1	FFT 0
2	FFT 1
3	FFT 2
4	FFT 3
5	FFT 4
6	FSTC BUFFER BOARD
7	FCC
8	FFT 5
9	FFT 6
10	FFT 7
11	FFT 8
12	FFT 9

SEE L025D01.SCH FOR RACKS 2 AND 3.
SEE L025D05 FOR CABLING TOP LEVEL

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: FFT BIN (RACKS 0 AND 1)

Size	Document Number	REV
C	56000L025 (RACKWIRE/L025D45.SCH)	
Date: July 23, 1996	Sheet 1 of 32	



SPECIAL VERSION FOR RACKS 0 AND 1
WITH FSTC BUFFER BOARD.

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
FFT CARD OUTPUT PIN CONNECTIONS

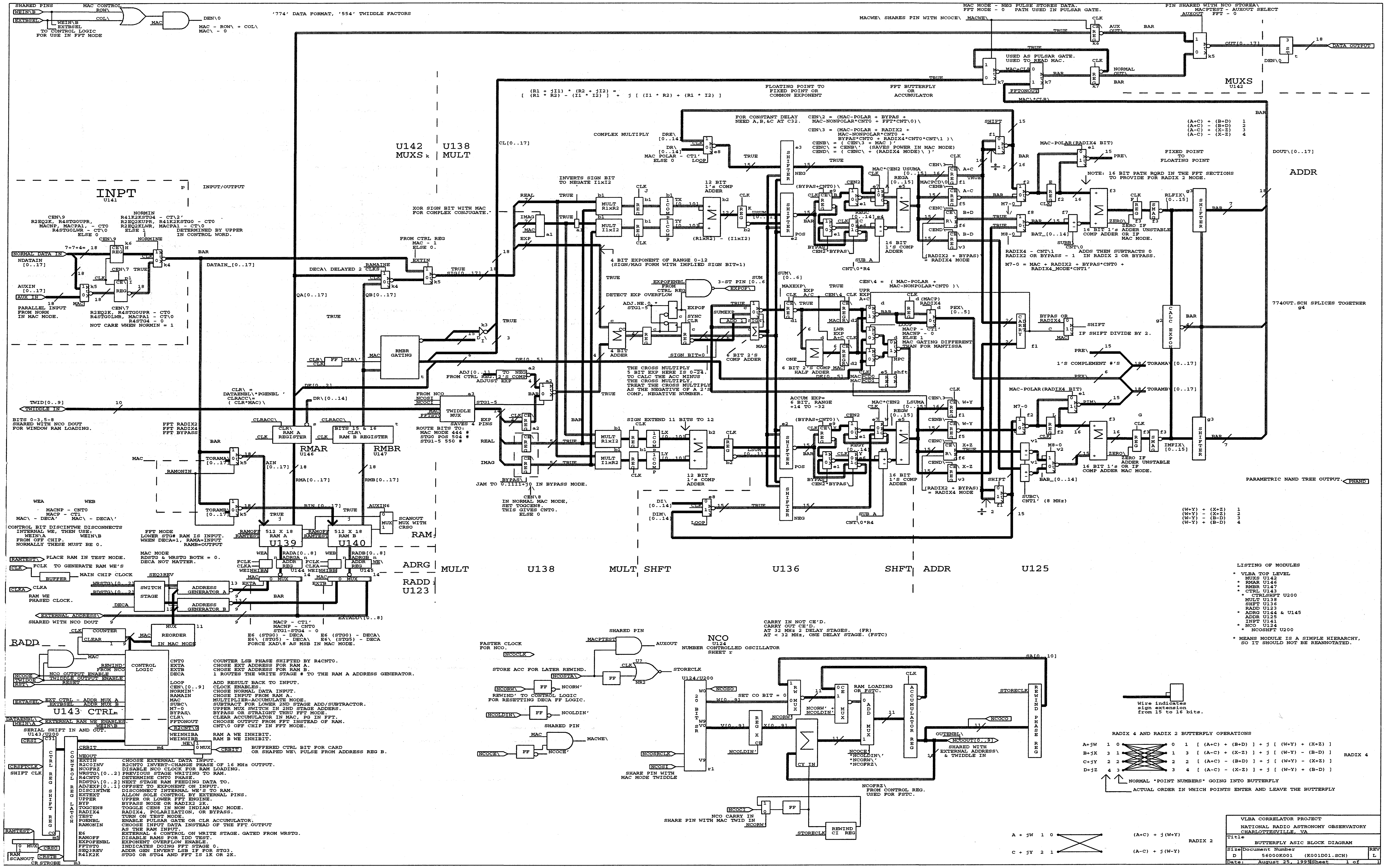
Size	Document Number	REV
C	56000L025 (RACKWIRE/L025D46.SCH)	

Date: July 22, 1996 Sheet 2 of 32

5 VLBA1 Gate Array

ASIC Block Diagram k001d01.sch

VLBA1 Pinout k028d03.blk


'774' DATA FORMAT, '554' TWIDDLE FACTORS
MAC MODE - NEG PULSE STORES DATA.
FFT MODE - 0 PATH USED IN PULSAR GATE.
MACWE\ SHARES PIN WITH NCOCE\
PIN SHARED WITH NCO STOREA\
MACPTEST - AUXOUT SELECT
AUXOUT FFT - 0
DATA OUTPUT
USED AS PULSAR GATE.
USED TO READ MAC.
MUXS
U142
(R1 + jI1) * (R2 + jI2) =
[(R1 * R2) - (I1 * I2)] + j [(I1 * R2) + (R1 * I2)]
FLOATING POINT TO
FIXED POINT OR
COMMON EXPONENT
FFT BUTTERFLY
OR
ACCUMULATOR
FOR CONSTANT DELAY
NEED A,B,&C AT C32.
COMPLEX MULTIPLY
(A+C) + (B+D) 1
(A+C) - (B+D) 2
(A-C) + (X-Z) 3
(A-C) - (X-Z) 4
U142 MUXS
U138 MULT
FIXED POINT
TO
FLOATING POINT
NOTE: 16 BIT PATH RQRD IN THE FFT SECTIONS
TO PROVIDE FOR RADIX 2 MODE.
ADDR
INPT
U141
INPUT/OUTPUT
INVERTS SIGN BIT
TO NEGATE I1xI2
XOR SIGN BIT WITH MAC
FOR COMPLEX CONJUGATE.
12 BIT
1's COMP
ADDER
4 BIT EXPONENT OF RANGE 0-12
(SIGN/MAG FORM WITH IMPLIED SIGN BIT=1)
DETECT EXP OVERFLOW
6 BIT 2'S
COMP ADDER
6 BIT 2'S COMP MAC
HALF ADDER
RADIX4 - CNT\1
RADIX2 OR BYPASS - 1 IN RADIX 2 OR BYPASS.
M7-0 = MAC + RADIX2 + BYPAS*CNT0 +
RADIX4_MODE*CNT1'
774OUT.SCH SPLICES TOGETHER
IF SHIFT DIVIDE BY 2.
1'S COMPLEMENT #'S
TORAMA\[0..17]
TORAMB\[0..17]
THE CROSS MULTIPLY
5 BIT EXP HERE IS 0-24.
TO CALC THE ACC MINUS
THE CROSS MULTIPLY,
TREAT THE CROSS MULTIPLY
AS THE NEGATIVE OF A 2'S
COMP, NEGATIVE NUMBER.
ACCUM EXP=
6 BIT, RANGE
+14 TO -32
TWIDDLE
MUX
SAVES 4 PINS
ROUTE BITS TO:
MAC MODE 444 #
STG0 POS 504 #
STG1-5 550 #
SIGN EXTEND 11 BITS TO 12
JAM TO 0.1111+j0 IN BYPASS MODE.
IN NORMAL MAC MODE,
SET TOGCEN8.
THIS GIVES CNT0.
ELSE 0
ZERO IF
ADDER UNSTABLE
OR IF
MAC MODE.
PARAMETRIC NAND TREE OUTPUT.
(W+Y) + (X+Z) 1
(W+Y) - (X+Z) 2
(W-Y) + (B-D) 3
(W-Y) - (B-D) 4
RMAR
U146
RMBR
U147
512 X 18
RAM A
U139
512 X 18
RAM B
U140
SCANOUT
MUX WITH
CRSO
RAM
ADRG
RADD
U123
MULT
U138
MULT SHFT
U136
SHFT ADDR
U125
LISTING OF MODULES
* VLBA TOP LEVEL
MUXS U142
* RMAR U146
* RMBR U147
* CTRL U143
* CTRLSHFT U200
MULT U138
SHFT U136
RADD U123
* ADRG U144 & U145
ADDR U125
INPT U141
* NCO U124
* NCOSHFT U200
* MEANS MODULE IS A SIMPLE HIERARCHY,
SO IT SHOULD NOT BE REANNOTATED.
CONTROL BIT DISCINTWE DISCONNECTS
INTERNAL WE, THEN USE:
WEIN\A WEIN\B
FROM OFF CHIP.
NORMALLY THESE MUST BE 0.
FFT MODE
LOWER STG# RAM IS INPUT.
WHEN DECA=1, RAMA=INPUT
RAMB=OUTPUT
MAC MODE
RDSTG & WRSTG BOTH = 0.
DECA NOT MATTER.
PLACE RAM IN TEST MODE.
TO GENERATE RAM WE'S
MAIN CHIP CLOCK
RAM WE
PHASED CLOCK.
SHARED WITH NCO DOUT
ADDRESS
GENERATOR A
ADDRESS
GENERATOR B
REORDER
IN MAC MODE
RADD
CONTROL
LOGIC
U143 CTRL
COUNTER LSB PHASE SHIFTED BY R4CNT0.
CHOSE EXT ADDRESS FOR RAM A.
CHOSE EXT ADDRESS FOR RAM B.
1 ROUTES THE WRITE STAGE # TO THE RAM A ADDRESS GENERATOR.
ADD RESULT BACK TO INPUT.
CLOCK ENABLES.
CHOSE NORMAL DATA INPUT.
CHOSE INPUT FROM RAM A.
MULTIPLIER-ACCUMULATE MODE.
SUBTRACT FOR LOWER 2ND STAGE ADD/SUBTRACTOR.
UPPER MUX SWITCH IN 2ND STAGE ADDERS.
BYPASS OR STRAIGHT THRU FFT MODE.
CLEAR ACCUMULATOR IN MAC, PG IN FFT.
CHOOSE OUTPUT FROM FFT INSTEAD OF RAM.
CNT\0 OFF CHIP IN FFT MODE.
RAM A WE INHIBIT.
RAM B WE INHIBIT.
BUFFERED CTRL BIT FOR CARD
OR SHAPED WE\ PULSE FROM ADDRESS REG B.
CHOOSE EXTERNAL DATA INPUT.
INVERT-CHANGE PHASE OF 16 MHz OUTPUT.
DISABLE NCO CLOCK FOR RAM LOADING.
PREVIOUS STAGE WRITING TO RAM.
DETERMINE CNT0 PHASE.
NEXT STAGE RAM FEEDING DATA TO.
OFFSET TO EXPONENT ON INPUT.
DISCONNECT INTERNAL WE'S TO RAM.
ALLOW SOLE CONTROL BY EXTERNAL PINS.
UPPER OR LOWER FFT ENGINE.
BYPASS MODE OR RADIX2 2K.
TOGGLE CEN8 IN NON INDIAN MAC MODE.
RADIX4, POLARIZATION, OR BYPASS.
TURN ON TEST MODE.
ENABLE PULSAR GATE OR CLR ACCUMULATOR.
CHOOSE INPUT DATA INSTEAD OF THE FFT OUTPUT
AS THE RAM INPUT.
EXTERNAL 6 CONTROL ON WRITE STAGE. GATED FROM WRSTG.
DISABLE RAMS FOR IDD TEST.
EXPONENT OVERFLOW ENABLE.
INDICATES DOING FFT STAGE 0.
ADDR GEN INVERT LSB IF FOR STG3.
STG0 OR STG4 AND FFT IS 1K OR 2K.
SERIAL SHIFT IN AND OUT.
U143/U200
SHIFT CLK
RAM SCANOUT
CR STROBE
FASTER CLOCK
FOR NCO.
STORE ACC FOR LATER REWIND.
REWIND' TO CONTROL LOGIC
FOR RESETTING DECA FF LOGIC.
SHARED PIN
NCO
U124
NUMBER CONTROLLED OSCILLATOR
CARRY IN NOT CE'D.
CARRY OUT CE'D.
AT 32 MHz 2 DELAY STAGES. (FR)
AT < 32 MHz, ONE DELAY STAGE. (FSTC)
SET CO BIT = 0
RAM LOADING
OR FSTC.
ACCUMULATOR REG
REWIND PHASE REG
SHARED WITH
EXTERNAL ADDRESS\
& TWIDDLE IN
SHARE PIN WITH
MAC MODE TWIDDLE
NCOFRZ\
FROM CONTROL REG.
USED FOR FSTC.
NCO CARRY IN
SHARE PIN WITH MAC TWID IN
REWIND
CI REG
Wire indicates
sign extension
from 15 to 16 bits.
RADIX 4 AND RADIX 2 BUTTERFLY OPERATIONS
A+jW 1 0 — 0 1 [(A+C) + (B+D)] + j [(W+Y) + (X+Z)]
B+jX 3 1 — 1 3 [(A-C) + (X-Z)] + j [(W-Y) - (B-D)]
C+jY 2 2 — 2 2 [(A+C) - (B+D)] + j [(W+Y) - (X+Z)]
D+jZ 4 3 — 3 4 [(A-C) - (X-Z)] + j [(W-Y) + (B-D)]
RADIX 4
NORMAL "POINT NUMBERS" GOING INTO BUTTERFLY
ACTUAL ORDER IN WHICH POINTS ENTER AND LEAVE THE BUTTERFLY
A + jW 1 0 — (A+C) + j(W+Y)
C + jY 2 1 — (A-C) + j(W-Y)
RADIX 2
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title
BUTTERFLY ASIC BLOCK DIAGRAM
Size D
Document Number
56000K001 (K001D01.SCH)
REV L
Date: August 25, 1995 Sheet 1 of 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	V	N4	A4	N6	N7	A8	CLKA	N9	A10	A11	N13	A14	G	A
B	A2	N2	N3	N5	A6	N8	FCLK	A9	N11	A12	A13	N15	A16	B
C	N0	A1	G	A3	A5	A7	G	N10	N12	N14	V	A15	N17	C
D	E1	A0	N1								N16	A17	O1	D
E	E3	E2	E0								O0	O2	O3	E
F	E6	E5	E4								O4	O5	O6	F
G	V	E7	G								V	G	O7	G
H	E8	NCD9	T0								PND	V	CLK	H
J	T1	T2	NCCK								O10	O8	RST	J
K	T3	T5	T8								O14	O11	O9	K
L	T6	R2C0	V	NCCI	NSCK	NCRW	T4	WEA	CRCK	RMTS	O17	O13	O12	L
M	T7	T9	NCOE	NCCE	NCSO	NCCO	G	EXB	EXOF	CRST	G	O16	O15	M
N	G	NCSI	TWOE	NCLD	NCST	V	DEBL	EXA	WEB	CRSI	CRSO	CRBT	V	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

VLBA1 ASIC

TOP VIEW

120 PIN PGA (121 PINS TOTAL)

LABEL	PIN NAMES
V	VCC
G	GROUND
N0-N17	NDATAIN[0..17]
A0-A17	AUXIN[0..17]
E0-E8	EXTADD\[0..8]
O0-O17	OUT[0..17]
T0-T9	TWID[0..9]
CLK	CLK
CLKA	CLKA
FCLK	FCLK
NCCK	NCOCLK
PNND	PNAND
RST	RST\
R2C0	R2CNT0
WEA	WEIN\A
WEB	WEIN\B
EXA	EXTASEL
EXB	EXTBSEL

LABEL	PIN NAMES
CRCK	CRSFTCLK
CRST	CRSTB
CRSI	CRSI
CRSO	CRSO
CRBT	CRBIT
RMTS	RAMTEST\
EXOF	EXPOF\
TWOE	TWIDOE
NCOE	NCOOE
NCD9	NCODOUT9
NCCI	NCOCI
NSCK	NCOSRCLK
NCRW	NCORW\
NCCE	NCOCE\
NCSO	NCOSO
NCCO	NCOCO
NCSI	NCOSI
NCLD	NCOLDIN\
NCST	NCOSTA\
DEBL	DATAENBL\

This drawing combines k028d01.blk and k028d02.blk onto one drawing.

	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	G	A14	N13	A11	A10	N9	CLKA	A8	N7	N6	A4	N4	V	A
B	A16	N15	A13	A12	N11	A9	FCLK	N8	A6	N5	N3	N2	A2	B
C	N17	A15	V	N14	N12	N10	G	A7	A5	A3	G	A1	N0	C
D	O1	A17	N16								N1	A0	E1	D
E	O3	O2	O0								E0	E2	E3	E
F	O6	O5	O4								E4	E5	E6	F
G	O7	G	V								G	E7	V	G
H	CLK	V	PND								T0	NCD9	E8	H
J	RST	O8	O10								NCCK	T2	T1	J
K	O9	O11	O14								T8	T5	T3	K
L	O12	O13	O17	RMTS	CRCK	WEA	T4	NCRW	NSCK	NCCI	V	R2C0	T6	L
M	O15	O16	G	CRST	EXOF	EXB	G	NCCO	NCSO	NCCE	NCOE	T9	T7	M
N	V	CRBT	CRSO	CRSI	WEB	EXA	DEBL	V	NCST	NCLD	TWOE	NCSI	G	N
	13	12	11	10	9	8	7	6	5	4	3	2	1	

VLBA1 ASIC

BOTTOM VIEW

120 PIN PGA (121 PINS TOTAL)

In m:/ga/sch/SCCS

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: VLBA1 PIN ASSIGNMENTS, 120 PIN PGA

Size	Document Number	REV
B	56000K028 (K028D03.BLK)	

Date: November 10, 1997 | Sheet 3 of 3

6 FFT Test Fixture Schematic and Block Diagram

FFT Test Fixture Top Level Schematic l015d37.sch

FFT Test Fixture Block Diagram l015d38.sch

TOP LEVEL
L015D01.SCH

CARD TO CARD CABLES
L015D19.SCH

CARD A

CARD A PINOUT
L015D14.SCH

CARD A SCH
L015D05.SCH

CARD A MUX PAL
L015D16.SCH

CARD A LAYOUT
Z011D01.LAY

CARD B

CARD B PINOUT
L015D11.SCH

CARD B SCH
L015D02.SCH

SEQUENCER
L015D06.SCH

CARD B RAMS & SR
L015D07.SCH

CARD B PAL SCH
L015D09.SCH

CARD B LAYOUT
Z011D02.LAY

SYSTEM TIMING
L015D17.SCH

STAGGERED CTR TIMING
L015D24.SCH

CLOCK DIST BOARD
L015D21.SCH

CK SIGNAL & DISTRIBUTION
L015D20.SCH

CARD C

CARD C HCB PINOUT
L015D08.SCH

CARD C HCB TOP
L015D12.SCH

HCB
L015D04.SCH

CARD C LAYOUT
Z011D03.LAY

CARD D

CARD D PINOUT
L015D13.SCH

CARD D SCH
L015D10.SCH

CARD D LAYOUT
Z011D04.LAY

BLOCK DIAGRAM

BLOCK DIAGRAM
L015D38.SCH

SUBSTITUTE FFT CARD

SUBFFT SCH
L015D22.SCH

SUBFFT LAYOUT
Z011D05.LAY

MISC

VCO
L015D15.SCH

LOGIC AN CABLE
L015D35.SCH

PNAND BOARD
L015D23.SCH

SOFTWARE

LDRAMS&LDMACCW
L015D03.SCH

SEQUENCER SW
L015D18.SCH

MAC SELF TEST SOFTWARE
L015D34.SCH

SUBROUTINE COMPSNAP
L015D36.SCH

SUBSTITUTE MAC CARD

SUBMAC SCH
L015D25.SCH

RAM/ROM
L015D26.SCH

DATA IN
L015D27.SCH

COMPARE
L015D28.SCH

SEQUENCER
L015D31.SCH

CONTROL PAL
L015D29.SCH

COMPARE PAL
L015D30.SCH

LAYOUT
Z011D06.LAY

TIMING
L015D32.SCH

SWITCH POSITION EXPLANATION
L015D33.SCH

EDIT IN j:/orcad/ffttfix
MASTERS IN m:/ffttfix/sch/SCCS

NATIONAL RADIO ASTRONOMY OBSERVATORY		
Title: FFT TEST FIXTURE TOP LEVEL MENU		
Size: A	Document Number: 56000L015 (L015D37.SCH)	REV:
Date: August 6, 1996	Sheet 37 of 37	

* INDICATES DIFF TTL SIGNAL
** INDICATES DIFF ECL SIGNAL INVERTED PINS NOT SHOWN

MACWE IN 4 CYCLE GAP AFTER FFT CYCLE.

FFT CARD INPUTS

FFT CARD OUTPUTS

C32ECL
C32ECL\

CCINIT

FCC

FFT CONTROL CARD

FFT CARD

TRIG TABLE INPUTS
8 SETS OF 32 MHz
INPUT SIGNALS
77 PINS

SIN/COS1[0..9]
SIN/COS2[0..9]
SIN/COS3[0..9]
SIN/COS4[0..9]
SIN/COS1[0..9]\
SIN/COS2[0..9]\
SIN/COS3[0..9]\
SIN/COS4[0..9]\
SC5=1K[0..7]
SC5=1K[0..8]

CONTROL REGISTER CONTROLS
SERIAL DATA IN. — CRSI\
REGISTER CLOCK. — CRSPTCLK
DOUBLE BUFFER STROBE. — CRSTB
3 PINS

NCO FSTC CONTROLS
SERIAL PARAMETER INPUTS — FSSIA, FSSRCLK, FSSIB
SERIAL PARAMETER CLOCK — FSSIC, FSSID

LOAD NEW FSTC PARAMETER STB. — FSCLOAD\
STORE PHASE. TIE HIGH — FSST\
REWIND PHASE. TIE HIGH — FSRW\
11 PINS

PARAMETER RAM LOAD AND CLOCK — LDRAM, RAMCLK
2 PINS

NCO FRINGE ROTATOR CONTROLS
LOAD NEW FRINGE PARAMETERS ENABLE. — FRLOAD\
REWIND FRINGE PHASE ENABLE. — FRRW\
FRINGE NCO SERIAL PARAMETER INPUT — FRSI
FRINGE NCO SERIAL PARAMETER CLOCK — FRSRCLK

NEWFR (NEW FRINGE) FOR SYNCHRONIZING THE STORE CYCLES. — NEWFR

PULSAR GATES. 4 PINS — PULSAR[0..3]
UPPER HALF OF PARAMETER RAM BANK SELECT. — UPRMEM

STAGGERED FFT TIMING SIGNALS
4 PINS — FFTINIT\, INIT\3', INIT\4', INIT\5'

DCOMM[0..7] *
SELECT FFTCTRL * DCOMM BUS & CTRL
STROBE *
MODE[0..1] *
ACK\IRQ FFTCTRL *

C32ECL
C32ECL\

MULTIPLEXED FFT
444 OUTPUT DATA
ECL DIFFERENTIAL DATA

DT[0..11] **
DB[0..11]

ROWS A & B CHANNELS 0 & 1 — E0V[0..11], E1V[0..11]
ROWS C & D CHANNELS 2 & 3 — E2V[0..11], E3V[0..11], E0H[0..11], E1H[0..11], E2H[0..11], E3H[0..11]

48 PINS

C32ECL
C32ECL\

MAC CARD

ASIC 0
MACWE
RAM BANK 0
RAM BANK 1
EXT ADR8
AUXOUT
EXT ADR[0..7]
ASIC 1
MACWE
RAM BANK 0
RAM BANK 1
EXT ADR8
AUXOUT
EXT ADR[0..7]

ROW, COL, ARRAY CHOSES ASIC
TO uP
REG
STAREAD

TFC
DOUT[0..17]

AFTER MACWE, NEED TO READ THE 32, 36 BIT #S. THEN MACWE'S ADDRESS CAN CHANGE FOR THE NEXT.

SINCE BANK SWITCH, CAN HAVE DUPLICATE MACWE'S FOR THE SAME MACWE ADDRESS.

TEST FIXTURE LOGIC

X 4

16 MHz OSC
8751
32K X 8 RAM
SHIFT REG — C01
64K X 4 RAM
SR LOAD
SHIFT REG — C00
64K X 4 RAM
262,144 BITS
LOAD RAMS — SEQUENCER BIT[3..17] — 8.192 ms

FFT CRSO\
XMULTCRSO
FRSO\

DOUT[0..17]

TFB

XMULT
CRSI
CR CLK
CR STB

CRD SEL\ TEST THAT INHIBITS CARD

TFB

C0[0..1]
C1[0..1]
C2[0..1]
C3[0..1]

EXTERNAL SOURCE 0 — ECL TO TTL
EXTERNAL SOURCE 2 — ECL TO TTL

DIFFERENTIAL ECL SYSTEM CLOCK
2
PAL
ADR\0
ADR\1
1 TO 4
REG
TTL TO DIFF ECL
A0C0[0..1] ... A3C0[0..1]
A0C1[0..1] ... A3C1[0..1]
A0C2[0..1] ... A3C2[0..1]
A0C3[0..1] ... A3C3[0..1]
**

FRONT PANEL SWITCH
DATA SOURCE
INT
EXT

TFA

TFA

FFT DATA INPUT SIGNALS
4 SETS OF 4 DIFFERENTIAL ECL INPUTS
64 PINS

TEST FAIL LED

RESET BY LED RESET BUTTON.

RESET
REG

TFC
HCB BUS & CTRL
DCOMM[0..7] *
SELECT uP *
STROBE *
MODE[0..1] *
ACK\IRQ uP *
PC INTERFACE

ADDRESS FOR MACWE
PCEA8
REG CE
EXT ADR8 BANK SWITCH
CLR POS
PCEA[0..7]
EXT ADR[0..7]
16 MHz
SEQ RESET\
EMACWE

TO MAC CARD MACWE
DINVALID[0..3]

MAC CARD CONTROL LOGIC — FFT CARD — FFT CTRL CARD

VCO
C32ECL
C32ECL\
RADIX 516 10 BIT COUNTER
ROM
SR LOAD
FFT CYCLE DATA
512+4 CLOCK CYCLES
16.125 usec
MACINIT\
MACWE\
CE'S

ECL FFTINIT
ECL FFTINIT\

FRONT PANEL SWITCH
INT
EXT
CLOCK SOURCE

8 BIT COUNTER
ROM
D
FRINGE CYCLE DATA
256 FFT CYCLES
4.128 ms

NEW FRINGE
DINVALID[0..3]

5 BIT COUNTER
D
INTEGRATION CYCLE DATA
32 FRINGE CYCLES
132.1 ms

8K x 8
CLK
CLR ACCUMULATOR

TFB

TEST FIXTURE LOGIC

C32
FROM uP STAREAD
REG
REG

ADR\0
ADR\1
INPUT MUX PROGRAM LINES
2 PINS

FFT CRSO\ CONTROL REGISTER SERIAL OUTPUT
1 PIN

FRSO\

EXPONENT OVERFLOW FLAGS
EXPOF\'[0..3]

LATCH X 4
TFD
LEDS
MASTER RESET
LED RESET BUTTON

TFB

SHORT TERM ACCUMULATOR STA READ
1 CYCLE IN 8

6 BIT ADDRESS FROM PC
CRD SEL\
ARRAY
ROW 1
ROW 0
COL 1
COL 0
LSB AUX OUT
EXT ADR[0..8]
INIT\

FIRST FFT CYCLE OF EVERY INTEGRATION CYCLE
WRITE ONCE PER FFT CYCLE
CLAC
MAC WE\

XMULT CRSI
CR CLK
CR STB

MAC CARD

C32
D C
STAREAD
C
REG
CARDSEL
ROW#
ROW DECODE
ROW\
COL DECODE
COL\
COL#
ARRAY
AUXOUT
D C
CLK
1 A
2
3 OE\
STAREAD

ROW\ 2 A
COL\ 3
1
NORM REG
AUX REG
MUX
3 ST
DOUT
CLK
18 BIT 2 TO 1 MUX AND REG
G MACCRSO SEL OE
OE\
ASIC
AUXOUT
CARDSEL\
COL MSB

TWO GROUPS OF 16 ASICS EACH ARE TRI-STATED TOGETHER ON THE CARD. ONE GROUP HAS ALL COLUMNS 0 & 1. THE OTHER GROUP HAS COLUMNS 2 & 3. THE COLUMN MSB THUS SELECTS BETWEEN THE TWO GROUPS AT THE CARD OUTPUT.

TFA, TFB, TFC, OR TFD SHOW WHICH TEST FIXTURE CARD CONTAINS THE NEARBY LOGIC.

NATIONAL RADIO ASTRONOMY OBSERVATORY		
Title: FFT TEST FIXTURE BLOCK DIAGRAM		
Size: C	Document Number: 56000L015 (L015D38.SCH)	REV
Date: February 5, 1998	Sheet 38 of	