VLBA Technical Report No. 46
THE VLBA CORRELATOR
DIGITAL FILTER
VOLUME 2 of 2

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February 1, 1999

firmanv2.doc Microsoft Word not under SCCS control

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(VOLUME II)

The 11 by 17 drawings in this volume can be plotted by invoking:
/corrdwgs/manuals/firman/plotfir, which is under SCCS control

This document can be printed without the placeholders by telling the print command to print pages 1,2,3,4,9,17,20,23

FIR Block Diagrams

EACH OUTPUT ROW
HOLDS A DUMP OF 215,040 COMPLEX #'S.

THE BUS IS AVAILABLE FOR BACK END OUTPUT EVERY 5TH 2 uSEC CYCLE.
READING 5 VALUES / 2 uSEC CYCLE WILL WORK FINE.

IF FIFO NOT EMPTY AT START
OF 2uSEC WINDOW, DISABLE WHOLE WINDOW.

430,080 COMPLEX FLOATING PT #/131 MS
IS REDUCED BY THE LTA TO A MAX OF
8 COMPLEX FLOATING POINT NUMBERS / FFT CYCLE
OR ONE COMPLEX # / 2.0156 uSEC

OR 3.969 MBYTES/SEC

LTA SENDS DATA
STORED IN EXTRA BASELINES

SNAPSHOT OF SELECTED RAM BANK
FOR XFER TO DRAM

FROM CLAC RAM

SNAPOE\
SNAPCE\

4 CYC DELAY FIFO

SLOEMPTY

10uSEC CLK

REG

EMPTY

E FIFO

HANDSHAKE LOGIC

TO BACKEND DATA

R0 I0 R2 I2 R1 I1 R3 I3

R4 I4 R6 I6 R5 I5 R7 I7

REG

R8 I8 R9 I9

WE\

REG

9

CE\ OE\ SNAPSHOT REG

MUX

ADRA

10

ADRB

ADRD

NEED TO BUNCH 8 uSEC
OF INPUT TO 2 uSEC
OF OUTPUT

OE\ FROM uP
uP WRITE

REG

COMPLEX NUMBER
EVERY 2 uSEC

RESULT

D[0..31]

32

FIRSI\

REAL THEN IMAG

NAND

OUTSTB

FIFO
32 X 64

8 MHz

RQSTSTB\

REQUESTS A COMPLEX NUMBER BE STROBED INTO FIFO
CLOCKS ADDRESS INTO LTA
CAUSES BUS FROM LTA TO NOT BE HIZ

32

R 29C327 FLOATING POINT CHIP S F

32

32

uP READ

REG

8 MHz CLOCK
WITH 1 CYCLE
MISSING/FFT CYCLE.

8 MHz

4 CYCLE DELAY FIFO

REG REG

ADRM

EACH 1Mx8 DRAM OUTLINED BY WIDE LINE.
20 M TOTAL RAM.

250 NS AVAILABLE FOR EACH R OR W.

VALIDITY DIVIDE
NUMERATOR FROM uP

16

1/X
TMC3210

16

SEE
L031D10

8 MHz
RAMS LOADED EVERY 131 MS
128 TAP WEIGHTS
1680 OF V

32

2Kx32

ADDRESS

11

16 MHz

uP 64 DEEP FIFO

TAP WEIGHT RAM ADDRESS GENERATION

TAP WEIGHT ADDRESS DE SEQUENCER

3

CLACENBL

7

CLAC RAM & MUX

SNAPCE\
SNAPOE\
CLAC INST TO 327

(TWI) TAP WEIGHT INDEX

DE COUNTER MODULUS FIFO

16 DEEP DELAY FIFO

4

7

TRI-STATE

11

beCOL9

beBANK

MUX

beADR9

LOADED EVERY 2 uSEC

DELAY

PULL-UP ON
4 MSB'S

UNLOAD AT
8 MHz

16 DEEP

8

BASELINE FIFO

CHANNEL FIFO

RESULT FIFO

8

3

11

RESULT

3

3 LSB'S

19-BIT ADDRESS TO LTA

8

BL IF LOADING VALIDITIES

8

19

MUX CONTROL BIT TELLING WHETHER TO THROW AWAY MSB OF BL OR RESULT ADDR

BLMSB

OUTBANK
R2,3,6,7

IMAG

21

RAM ADDRESS LOGIC

8 TO 1 MUX

10

BASELINE

8

210 IF LOADING VALIDITIES

210

29MA16

3 LSB'S

8

8

uP ADDRESS

20

REG

20

RAM WRITING

BL LIMITS FROM BACKEND

be ACCESS ADDRESS GENERATION SEE L031D07

REFRESH ROW COUNTER

9

ADR SELECT

ROW0 LTA RD/WR
COL LTA RD/WR
ROW1 LTA RD/WR
ROW 0 be RD
ROW 1 be RD
ROW u RD/WR
COL u RD/WR
ROW refresh

ASEL[0..2]

0 BLMSB=0
1
2 BLMSB=1
3 beBLMSB=0
4 beBLMSB=1
5
6
7

RSP RSF

BLP

LOCK=0

8 8

BL RS

LOCK FROM uP

RSP RSF

210

BLP

LOCK=1

8 8

BL RS

COUNTER

RD

3

MODULUS LSB'S

R D

TWI

4

STOPLOOP MSB

R D

LTA BASELINE FIFO

COUNTER MODULUS FIFO

DRAM BASELINE FIFO

REG

BASELINE
0-209 PLUS
EXTRAS FOR VALIDITY

MICROPROCESSOR LOAD

87C51

PROGRAM #

STOPLOOP

SEQUENCER

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

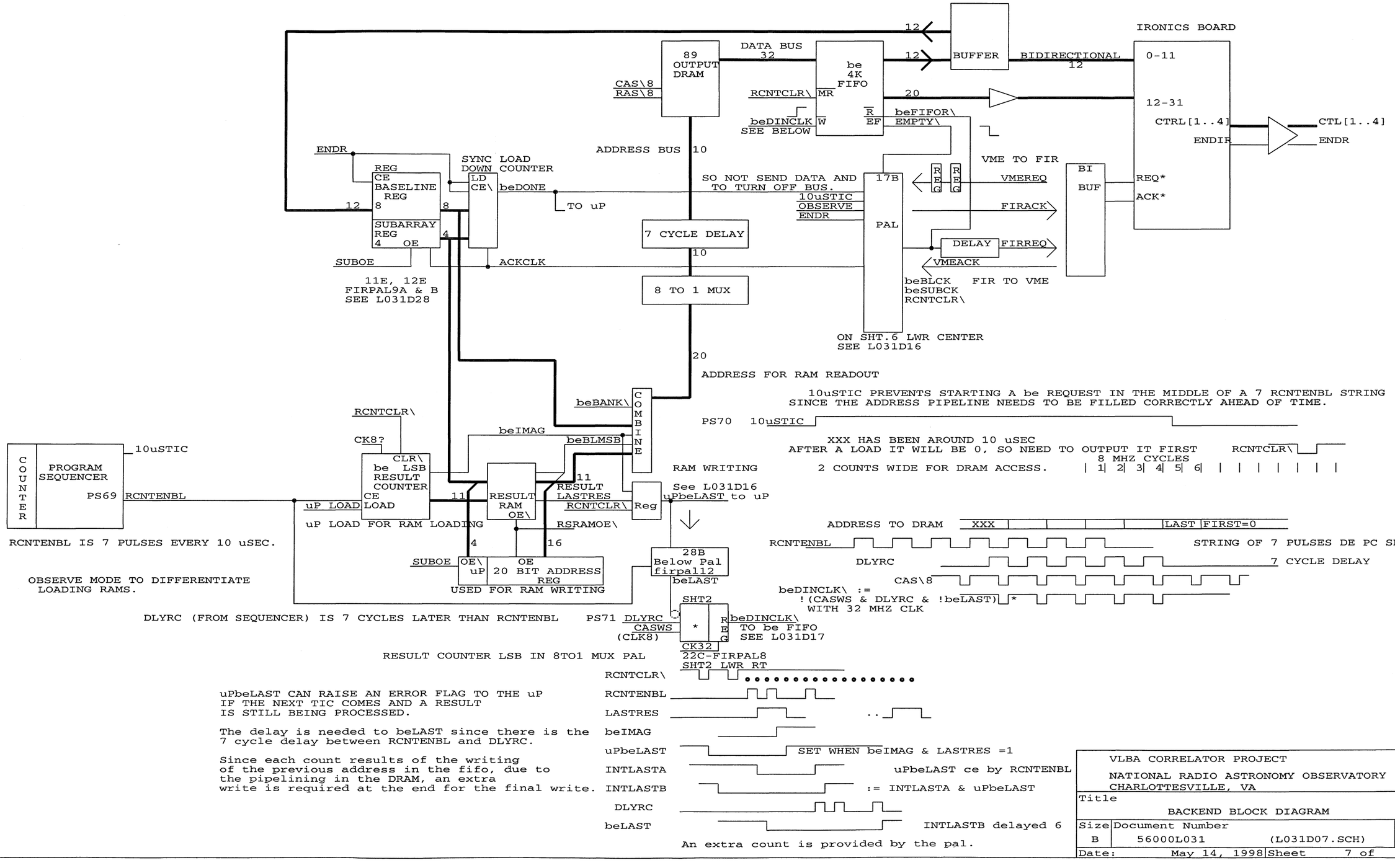
Title

TOP LEVEL FIR BLOCK DIAGRAM

Size	Document Number	REV
B	56000L031 (L031D25.SCH)	

Date: August 4, 1995 Sheet 25 of

RESET FIFO AT BEGINNINGING OF BASELINE WHEN !10uSTIC.
FIFO CAN HOLD WHOLE BASELINE, SO NOT NEED TO WORRY ABOUT FIFO OVERFLOW.



VLBA CORRELATOR PROJECT	
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA	
Title	BACKEND BLOCK DIAGRAM
Size: B	Document Number: 56000L031 (L031D07.SCH) REV:
Date: May 14, 1998	Sheet 7 of 41

FFT CYCLE = 16.125 uSEC
= 8, 2 uSEC CYCLES
SOFTWARE CYCLE IS 5 2uSEC CYCLES

SW 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8

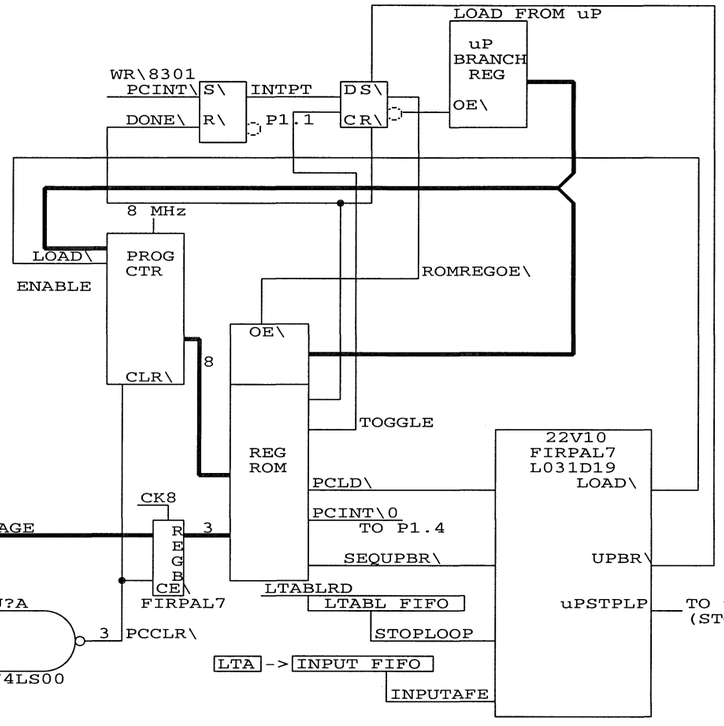
FFT

HENCE SW STEP DOES NOT REPEAT ON AN FFT BASIS

VALIDITIES ARE GOOD FOR A DUMP TIME.
SEQUENCER NEEDS TO SWITCH TO LOAD AND NORMALIZE VALIDITY MODE.

TO HAVE THE uP CONTROL THE SEQUENCER:
* LOAD THE uP REGISTERS WITH THE BRANCH ADDRESS & PAGE
* ON NEWPAGE AND PCCLR, CAPTURE REG CAUSES A PROGRAM IDLE LOOP
* A PCINT CAUSES THE BRANCHING TO THE uP REG ADDRESS SERVICE ROUTINE, AT THE APPROPRIATE SPOT, AS SPECIFIED BY TOGGLE.
* P1.1 TELLS THE uP THE SERVICE ROUTINE HAS BEEN COMPLETED.
* THE PC GOES BACK TO THE IDLE LOOP SPECIFIED BY THE SEQUENCER INSTRUCTION.

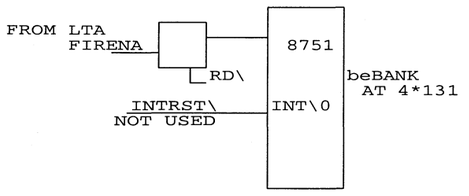
8 MHz
WO 4 CYCLE GAP → TO 29C327

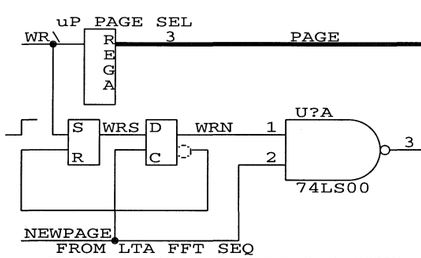


SEQUPBR\ ALLOWS THE SEQUENCER TO BRANCH TO THE ADDRESS IN THE UP BRANCH REG. TOGGLE WILL RESET IT AGAIN.

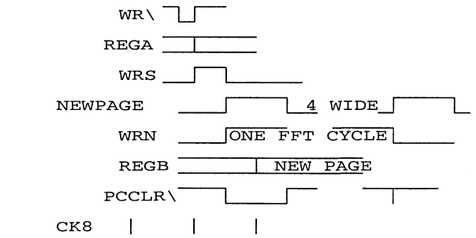
IF PCLD\ AND SEQUPBR\ OCCUR AT THE SAME TIME, CHECK THE INPUTOR & STOPLOOP SIGNALS

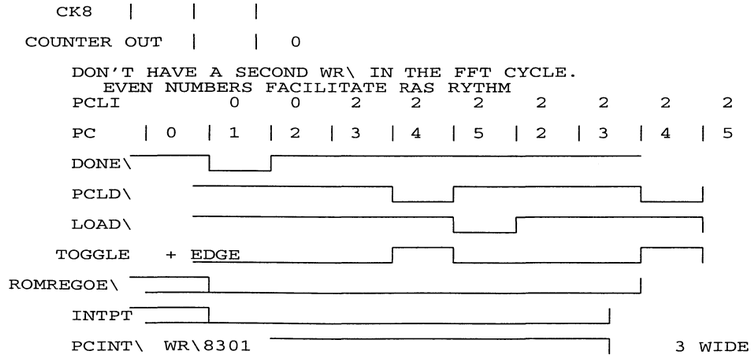
EVERY 131 MS





NEWPAGE FROM LTA FFT SEQ SINCE IT CONTROLS THE PC REG ROM.

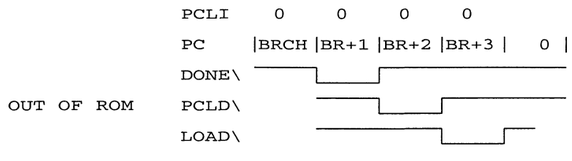




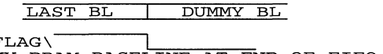
ON PCINT\, GO TO BRANCH ROUTINE BRCH IN BRANCH REG.
WHEN DONE BACK TO 0.

PCINT IDLE LOOP TIMING

MINIMUM LENGTH BRANCH

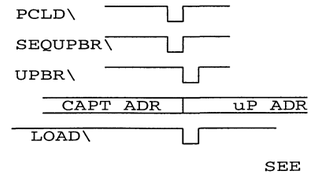


| JUST PAST START OF PROGRAM LOOP



EMPTY FLAG\
ON DUMMY DRAM BASELINE AT END OF FIFO
NEEDS TO BE WITHIN THE 10 uSEC PROGRAM CYCLE.

THE LAST BASELINE WILL SPAN MANY PROGRAM LOOPS.



SEE /FIRASM/SEQ.TXT

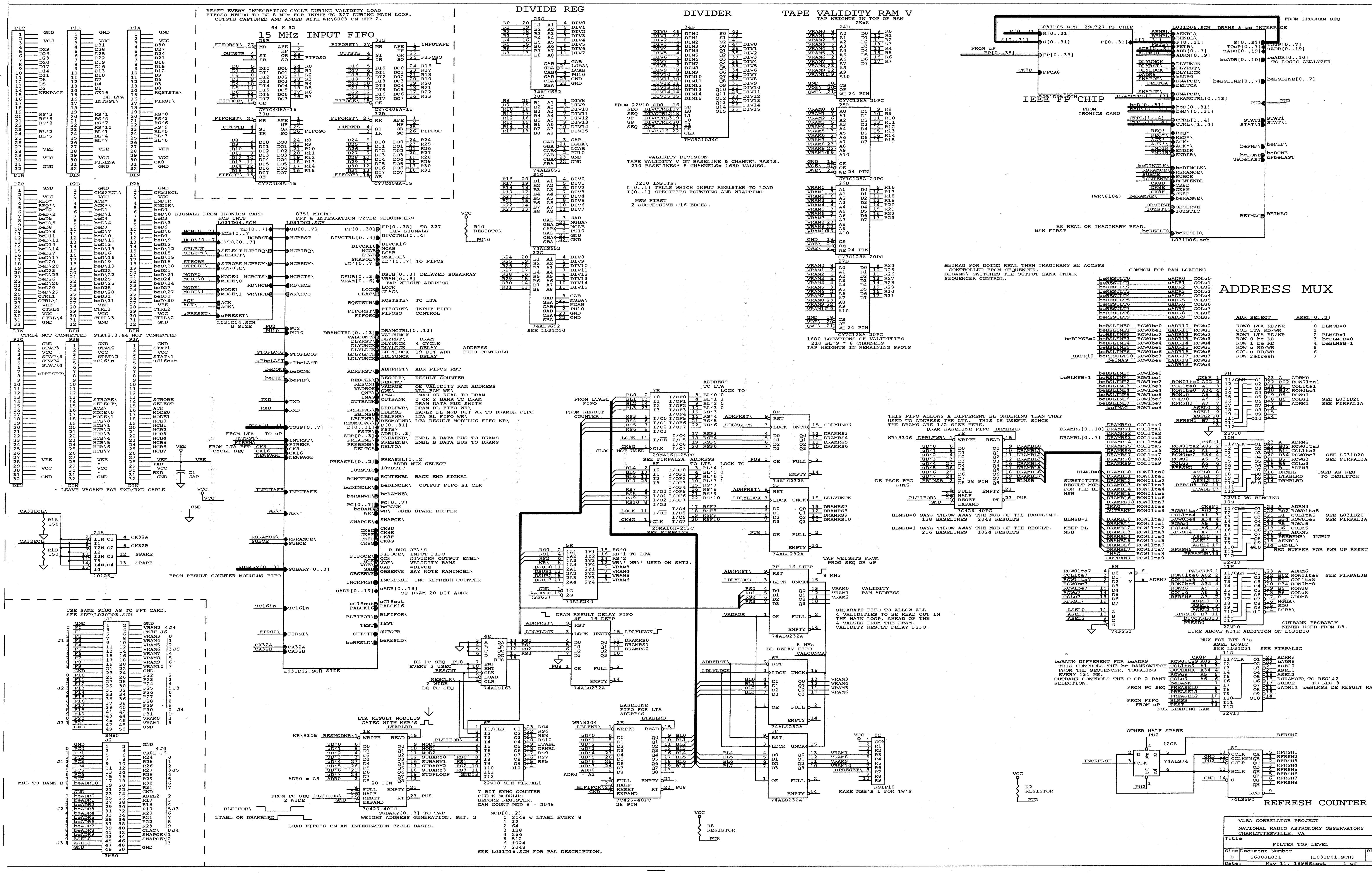
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: FIR SEQUENCER BLOCK DIAGRAM

Size	Document Number	REV
B	56000L031 (L031D09.SCH)	

Date: July 25, 1996 Sheet 9 of 41

2 FIR Schematics and Layout


DIVIDE REG
DIVIDER
TAPE VALIDITY RAM V
15 MHz INPUT FIFO
IEEE FP CHIP
ADDRESS MUX
REFRESH COUNTER
RESET EVERY INTEGRATION CYCLE DURING VALIDITY LOAD
FIFOSO NEEDS TO BE 8 MHz FOR INPUT TO 327 DURING MAIN LOOP.
OUTSTB CAPTURED AND ANDED WITH WR\8003 ON SHT 2.
VALIDITY DIVISION
TAPE VALIDITY V ON BASELINE & CHANNEL BASIS.
210 BASELINES* 8 CHANNELS= 1680 VALUES.
1680 LOCATIONS OF VALIDITIES
210 BL'S * 8 CHANNELS
TAP WEIGHTS IN REMAINING SPOTS
BEIMAG FOR DOING REAL THEN IMAGINARY BE ACCESS
CONTROLLED FROM SEQUENCER.
BEBANK\ SWITCHES THE OUTPUT BANK UNDER
SEQUENCER CONTROL.
THIS FIFO ALLOWS A DIFFERENT BL ORDERING THAN THAT
USED TO ADDRESS THE LTA. THIS IS USEFUL SINCE
THE DRAMS ARE 1/2 SIZE HERE.
BLMSB=0 SAYS THROW AWAY THE MSB OF THE BASELINE.
128 BASELINES 2048 RESULTS
BLMSB=1 SAYS THROW AWAY THE MSB OF THE RESULT.
256 BASELINES 1024 RESULTS
SEPARATE FIFO TO ALLOW ALL
4 VALIDITIES TO BE READ OUT IN
THE MAIN LOOP, AHEAD OF THE
4 VALUES FROM THE DRAM.
VALIDITY RESULT DELAY FIFO
* LEAVE VACANT FOR TXD/RXD CABLE
USE SAME PLUG AS TO FFT CARD.
SEE SDT\L020D03.SCH
FROM RESULT COUNTER MODULUS FIFO
LOAD FIFO'S ON AN INTEGRATION CYCLE BASIS.
7 BIT SYNC COUNTER
CHECK MODULUS
BEFORE REGISTER.
CAN COUNT MOD 8 - 2048
SEE L031D15.SCH FOR PAL DESCRIPTION.
MAKE MSB'S 1 FOR TW'S
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title
FILTER TOP LEVEL
Size D
Document Number 560001031 (L031D01.SCH)
REV
Date: May 11, 1998
Sheet 1 of 5

STOPLOOP LOAD SIGNAL TO LTABL FIFO

beBANK TOGGLES EVERY 4 x 131 MS.

INTEGRATION CYCLE RESET FROM LTA

WR\8003 STROBES INTO INPUT FIFO

WRITING TO DRAM OR FP MODE

WRITTEN BY WR\8302 WITH PAGE

32 BIT PATH FOR READING DRAM

F BUS VIA CROSS BAR LOGIC FROM SHT6

A4,3 AND A6,5 SPECIFIY THE ADDRESS AT THE CROSSBAR EACH TO 4 CHIPS FOR FANOUT

SELECTION	ADDRESS
0	0000000 8000
1	0101000 8028
2	1010000 8050
3	1111000 8078

MISCELLANEOUS READS COULD READ TWICE TO MAKE SYNCHRONOUS

32 BIT PATH FOR WRITING TO DRAM OR FP CHIP MODE VIA INPUT FIFO

uP 24 BIT DRAM ADDRESS REG ALSED TO READ AND WRITE THE RESULT RAM ON SHT. 7 STRAIGHT THRU ON READ. STORES ON WRITE

uP DRAM 20 BIT ADDR

uP SELECTS PAGE

DELAY SIGNAL TO INHIBIT WRITING INTO THE BACKEND FIFO. de 21B13

NEWPAGE BUFFERED SIGNAL FROM LTA SEQ

MEMOE\ = (A'\15*RD + PSEN)\ 32K x 8 RAM
B TO A IF READ AND UPPER MEMORY (8000-FFFF).

ONLY ENABLE WHEN NEEDED TO REDUCE ELECTRICAL NOISE.

DIV SIGNALS

BACKEND CONTROL

LTA BL FIFO WR\
LTA RESULT MODULUS FIFO WR\
DRAM BASELINE FIFO

WRITE RESULT RAM

LOAD BACKEND RESULT COUNTER DE uP
RESET THE BASELINE AND MODULUS FIFOS

ADDRESS SELECT MUX ADDRESS

TO LOGIC ANALYZER

PROGRAM COUNTER

F SINCE PHASED CLK FOR DRAMS

SEQ BRANCH REG

REGA FROM uP

FROM PC ROM PCINT DONE

PCINT\ TO INTERRUPT PC SEQUENCE

DE 22V10 uPBR\

TO DIVIDE CHIP

FP[0..38] CONFIGURES THE 29C327 CHIPS.

FP33	(ENI\) 0
FP34	(OE8\) 0
FP35	(FSEL) 1
FP36	(RM0) 0
FP37	(RM1) 0
FP38	(RM2) 0
DIVCTRL3	(I0) 1
DIVCTRL4	(I1) 1

SIGNALS FROM LTA'S FFT SEQ

RESISTOR FOR IF DEGENERATE LTA FROM LTA

DETERMINE CAS SHAPE

W/O 4 CYCLE GAP

NOTE: NOT BI-DIREC

TO INPUT FIFO 025022

IN PARALLEL WITH INPUT FIFO LOAD CLAC AND TW RAMS IN PARALLEL

NEED CLACENBL\ FOR WRITING CLAC FOR EACH TW IN EACH SUBARRAY LOAD WHEN LOADING TAP WEIGHTS

TAP WEIGHT

FROM FIFO WITH RESULT COUNTER MODULUS. LOADED BY uP

DELAY FOR TIME IN LTA.

TO 5E ON SHT. 1 TRI-STATE BUFFER WITH VRAM

SAME CTRL AS ON D06 4 CYCLE DELAY THRU 327

TSEL OF 0010 FOR CLAC FORCES 0 ELSE STRAIGHT THRU

VRAM IS THE ADDRESS BUS TO THE VALIDITY RAM. IT IS TRI-STATED WITH THE VALIDITY ADDRESS ON SHT. 1

SNAPOE\ IS ALWAYS 1 LATER THAN A SNAPCE\ FOR RAM BANK 7 SEE L031D39 FOR EXPLANATION

CLAC FP9 DLY	TW RAM DLY
SUBAUNCK 245 12 NS	245 12 NS
VRAM[3..5]\ 232 31 NS	232 31 NS
7C123 12 NS	F399 4U 3 NS
22V10 15 NS	46 NS OF 125
327 5U 19 NS	
89 NS OF 125	

SEE L031D19.SCH

ATOB=/(A15*(RD+PSEN))
/MEMOE= /(/A15*RD + PSEN)

be FIFO HF\ INPUT
ONLY USE ON PAGE 1 (SEE L031D27)

SEE L031D08 FOR TIMING

CASWR\ FROM FFT SEQ ROM

MAIN ADDRESS SELECT MUX CONTROL

MAIN RESULT COUNTER CLR\
MAIN RESULT COUNTER CE

APPROXIMATELY SYNCHRONOUS WITH CLOCK TO FP CHIP. SINCE ONE GATE DELAY.

TOGGLE CLK REG THAT DETERMINES PC BRANCH ADR.
DONE\ THE PC INTERRUPT BY uP IS DONE
INC REFRESH EVERY 10 uS
BASELINE AND MOD FIFO RESETS(2 WIDE)

29C327 CONTROL

DIRECT INPUT

CLOCK TO UNLOAD THE VALIDITY RAM FROM PROGRAM LOGIC CHANNEL 232 FIFO. 8 MHZ FOR PROGRAM LOGIC 7-31 NS DELAY

NO PROBLEM SINCE RAM ACCESS TIME C8A ALLOWS SLOWER RAM

CK8? ALLOWS EXTRA HT AT DESTINATION REGISTER

TO 24E-1 045058

TO SHT6

TO INPUT 408 FIFO SHIFT OUT TO 327 R BUS AT 8 MHz

PREVENTS BUS CONTENTION DRAM 4 CYCLE DLY

CK8? ALLOWS EXTRA HT AT DESTINATION REGISTER

19 BIT ADR DELAY

ADR FIFOS RESET

8 MHz FOR STRAIGHT THRU 327 TO be MODE

SEPARATE CAS'S FOR STARTUP AND END
SEE L031D08 FOR DRAM TIMING
SEE L031D17 FOR PAL DESCRIPTION

PS80-PS87 ARE BRANCH ADDRESS

SEQ BRANCH TO uP SPECIFIED ADDRESS.
TEST DE uP
PCLD\ LOADS PROGRAM COUNTER
OE\ TO DIVIDE CHIP

UNGATED uP READ STB
DIVIDER OUT REG CLK GEN
PRESE00. SD0 STARTS DIV
DIVCTRL1 L0, DIVIDER MODE SEL
DIVCTRL2 L1, DIVIDER MODE SEL
uPINT\0 INT uP TO LOAD FIFO'S

COUNT TO 245
245 SU 18 NS
F163 OUT 11 NS
ALS244 10 NS
39 NS

93 AVAIL FOR RASCK8

NOTE THIS RUNS OFF OF DIFFERENT CLOCK. IT MUST BE FASTER THAN THE OTHER PC COUNTER PROMS.

NOR OUT
UNBUFFERED CK8
245 OUT
OR OUT

RS RAM ADDRESS.

BACK END CONTROL SIGNALS

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

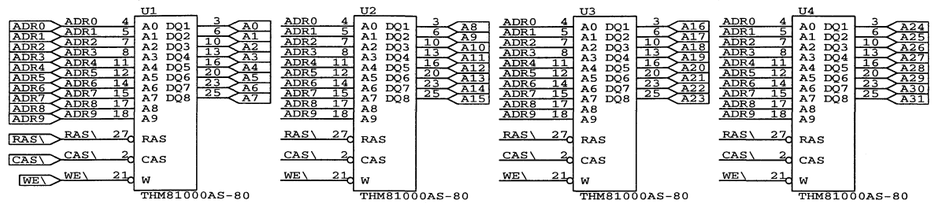
Title
FIR 8751 AND SEQUENCERS

Size	Document Number	REV
D	56000L031 (L031D02.SCH)	

Date: November 19, 1997 Sheet 2 of 5

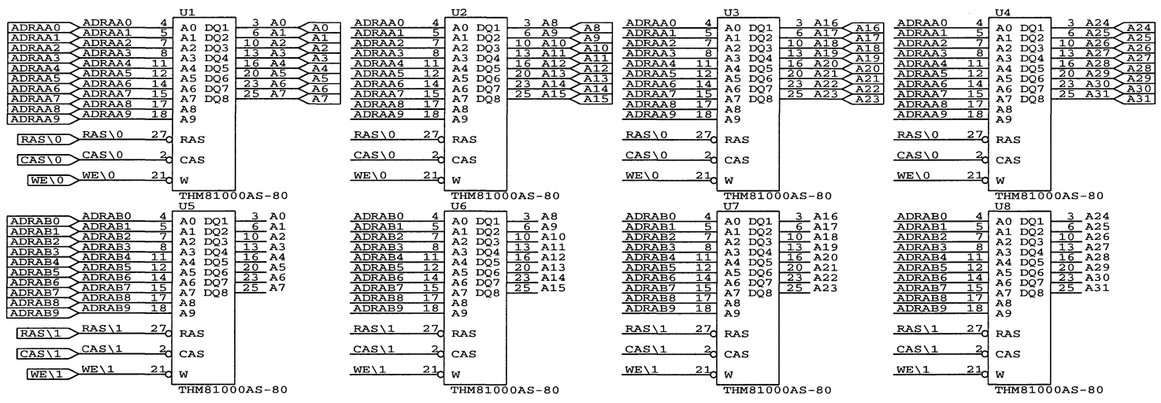
FOUR DRAM PC BOARD

HAVE BOARD FLUSH WITH ENDS OF CONNECTORS.
THE CONNECTORS ARE SPACED CLOSER TOGETHER THAN ON THE LTA.

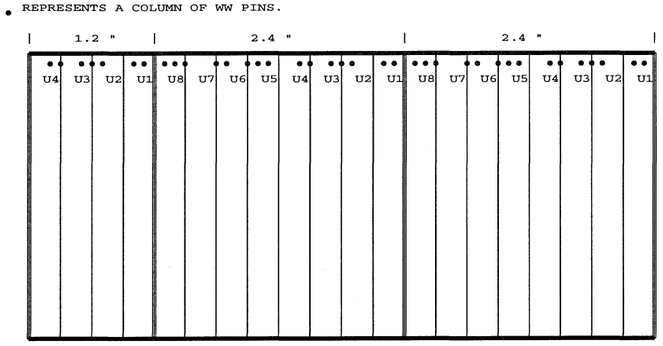


EIGHT DRAM PC BOARD

HAVE BOARD FLUSH WITH ENDS OF CONNECTORS.
THE CONNECTORS ARE SPACED CLOSER TOGETHER THAN ON THE LTA.



• REPRESENTS A COLUMN OF WW PINS.



2 OF THESE BOARDS WILL BE END TO END AS SHOWN

ELIMINATING THE VERTICAL GROUND BUSSES WILL FACILITATE ROUTING THE A[0..31] BUS ON THE TOP SIDE OF THE BOARD

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: FIR DRAM PC BOARD SCHEMATICS

Size	Document Number	REV
C	56000L031 (L031D03.SCH)	

Date: July 25, 1996 Sheet 3 of

HCB TARGET INTERFACE

HCB DATA BUS

HCB[0..7]
HCB\[0..7]

FLOATS TO NOT-SELECTED

VCC
R3 330
R4 150
R5 330

INPUTS FROM HCB

2B 75173
SELECT
SELECT\
STROBE
STROBE\
MODE0
MODE\0
MODE1
MODE\1
PU13
B0 B0 B1 B1 B2 B2 B3 B3 OE OE
O0 O1 O2 O3

2C 16L8 SEE FIRPAL11
SDATARDY BUSY\ SELECT STROBE MODE0 MODE1 uPRESET\
I1 I2 I3 I4 I5 I6 I7 I8 I9 I10
O1 O2 O3 O4 O5 O6 O7 O8
ACK RCVENA\ BUSENA OEA\ ACKA\ WRB\ RESET IRQ\

4A 2A 1A 75ALS171
BUSENA RCVENA\ PU13 BUS0 BUS1 BUS2 BUS3 BUS4 BUS5 BUS6 BUS7
CDE RE 1DE 1D 1R 2DE 2D 2R 3DE 3D 3R
1A 2A 3A 3B
HCB0 HCB\0 HCB1 HCB\1 HCB2 HCB\2 HCB3 HCB\3 HCB4 HCB\4 HCB5 HCB\5 HCB6 HCB\6 HCB7 HCB\7
ACK ACK\

OUTPUT TO HCB

3B 2952
BUS0 BUS1 BUS2 BUS3 BUS4 BUS5 BUS6 BUS7
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
uD0 uD1 uD2 uD3 uD4 uD5 uD6 uD7
OE-A OE-B WR-B WR-A WENB WENA

uD[0..7]
DATA BUS TO/FROM TARGET

DATA FROM MASTER IS READY (LOW TRUE) HCBRDY\
CLEAR TO SEND DATA TO MASTER (LOW TRUE) HCBCTS\

PU13
WRA\
ACKA\
WRB\
ACKB\
3AB 74ALS74 RDYA
3AA 74ALS74 RDYB\
S D Q C R

MASTER RESETS TARGET HCBRST
MASTER INTERUPTS TARGET HCBIRQ\
WR\HCB (WR\8007) TARGET WRITES DATA TO MASTER
RD\HCB (RD\8007) TARGET READS DATA FROM MASTER

VCC
R13 4.7K
PU13

SELECT	STROBE	MODE1	MODE0	FUNCTION	ACK	RCVENA\	BUSENA	OEA	ACKA\	WRB\	RESET	IRQ\
0	X	0	0	ALLOW TARGET TO ASSERT ATTENTION	SDATARDY\	1	0	1	1	1	0	1
0	X	0	1	IDLE	1	1	0	1	1	1	0	1
0	X	1	0	IDLE	1	1	0	1	1	1	0	1
0	X	1	1	IDLE	1	1	0	1	1	1	0	1
1	__	0	0	MSTR SENDS IRQ & 1st BYTE TO TARGET	1	0	0	1	STROBE\	STROBE\	0	STROBE\
1	__	0	1	MSTR WR SUBSEQUENT BYTES TO TARGET	BUSY\	0	0	1	STROBE\	STROBE\	0	1
1	__	1	0	MASTER READS FROM TARGET	SDATARDY\	1	STROBE	STROBE\	STROBE\	1	0	1
1	__	1	1	MASTER RESETS TARGET (HARD RESET)	1	1	0	1	STROBE\	1	STROBE	1

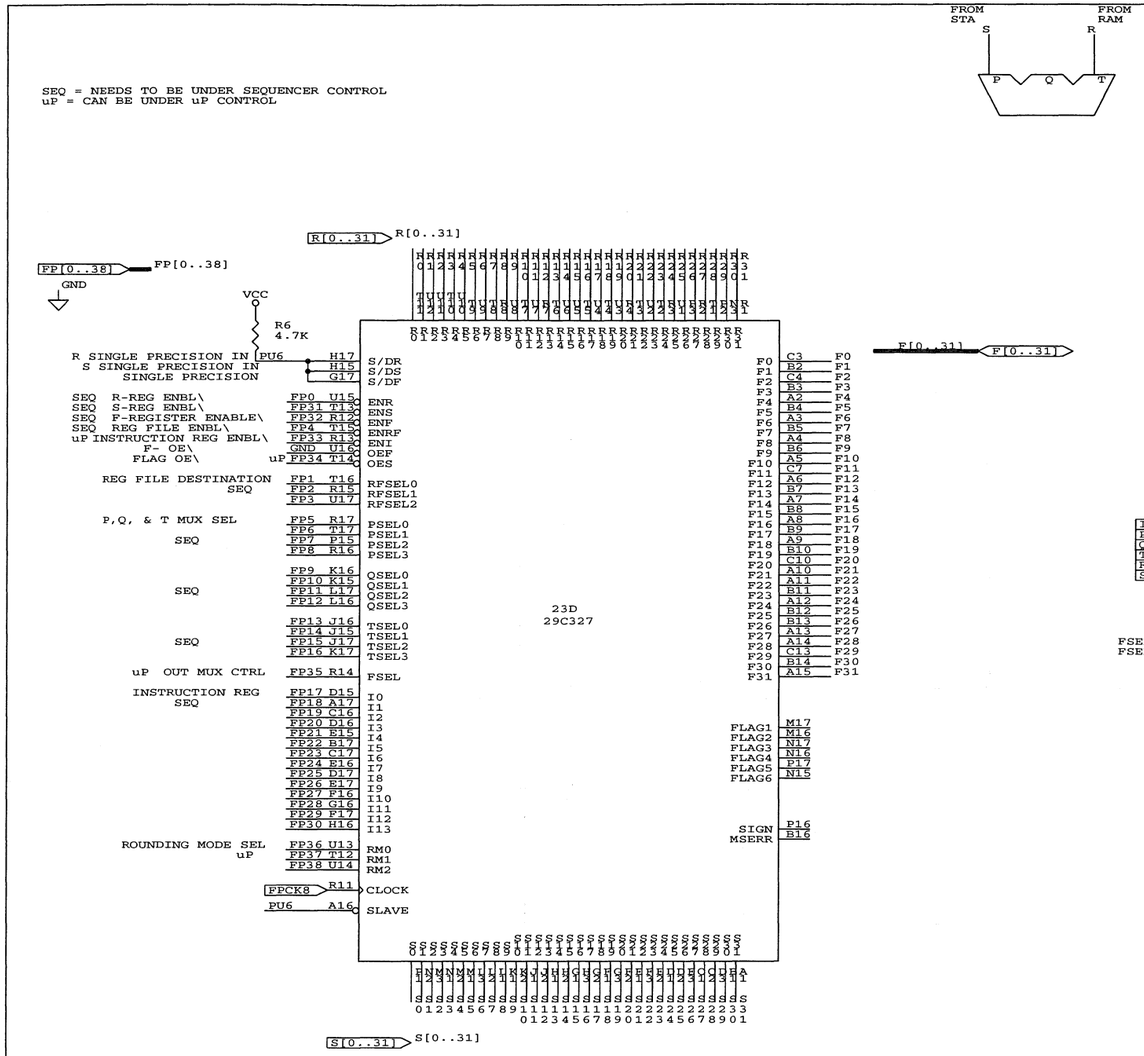
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

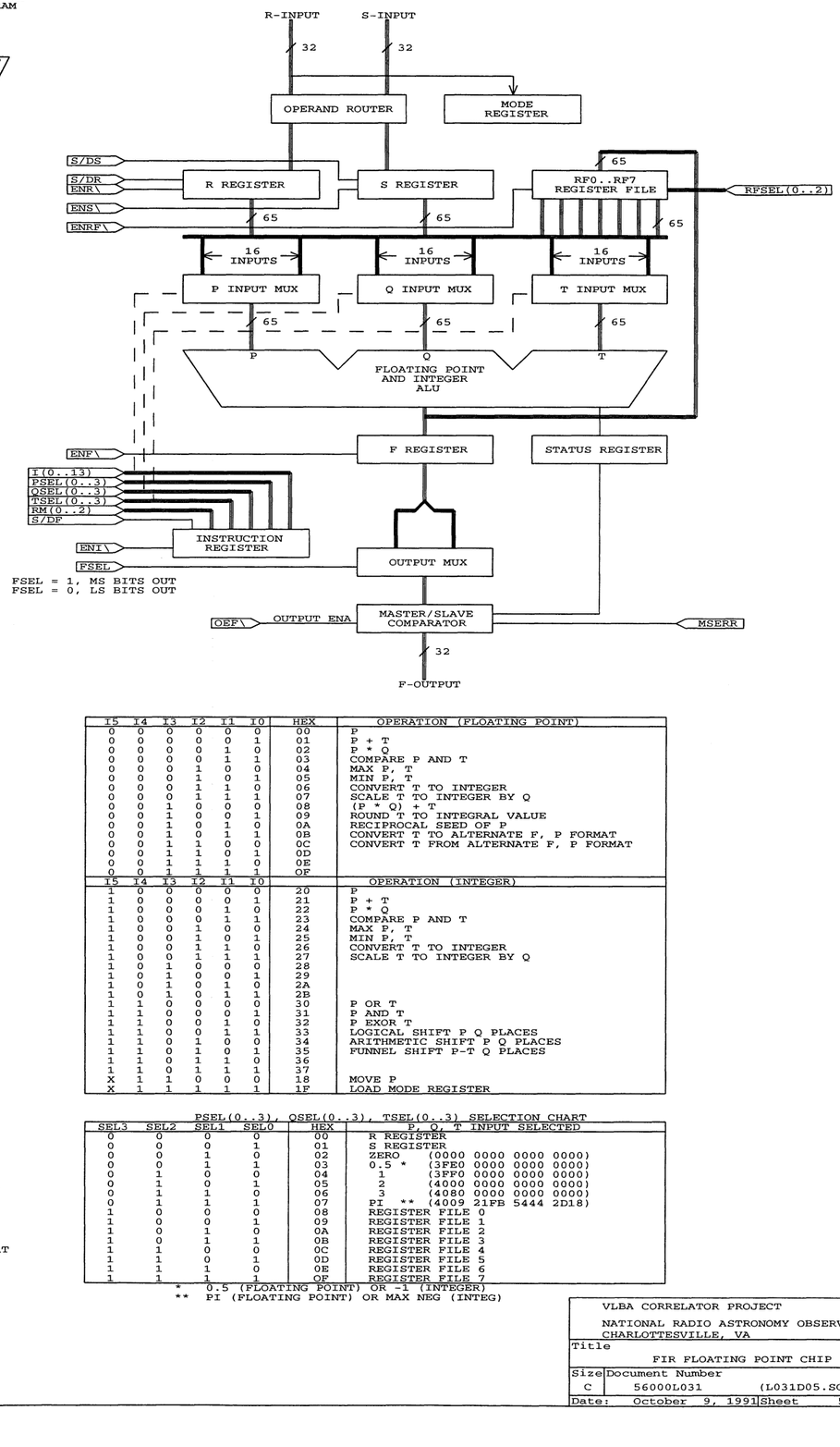
Title: FIR HCB TARGET INTERFACE

Size	Document Number	REV
B	56000L031 (L031D04.SCH)	

Date: April 6, 1992 Sheet 4 of 5

SEQ = NEEDS TO BE UNDER SEQUENCER CONTROL
uP = CAN BE UNDER uP CONTROL





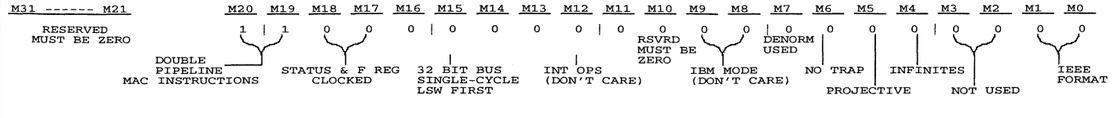
I5	I4	I3	I2	I1	I0	HEX	OPERATION (FLOATING POINT)
0	0	0	0	0	0	00	P
0	0	0	0	0	1	01	P + T
0	0	0	0	1	0	02	P * Q
0	0	0	0	1	1	03	COMPARE P AND T
0	0	0	1	0	0	04	MAX P, T
0	0	0	1	0	1	05	MIN P, T
0	0	0	1	1	0	06	CONVERT T TO INTEGER
0	0	0	1	1	1	07	SCALE T TO INTEGER BY Q
0	0	1	0	0	0	08	(P * Q) + T
0	0	1	0	0	1	09	ROUND T TO INTEGRAL VALUE
0	0	1	0	1	0	0A	RECIPROCAL SEED OF P
0	0	1	0	1	1	0B	CONVERT T TO ALTERNATE F, P FORMAT
0	0	1	1	0	0	0C	CONVERT T FROM ALTERNATE F, P FORMAT
0	0	1	1	0	1	0D	
0	0	1	1	1	0	0E	
0	0	1	1	1	1	0F	
I5	I4	I3	I2	I1	I0		OPERATION (INTEGER)
1	0	0	0	0	0	20	P
1	0	0	0	0	1	21	P + T
1	0	0	0	1	0	22	P * Q
1	0	0	0	1	1	23	COMPARE P AND T
1	0	0	1	0	0	24	MAX P, T
1	0	0	1	0	1	25	MIN P, T
1	0	0	1	1	0	26	CONVERT T TO INTEGER
1	0	0	1	1	1	27	SCALE T TO INTEGER BY Q
1	0	1	0	0	0	28	
1	0	1	0	0	1	29	
1	0	1	0	1	0	2A	
1	0	1	0	1	1	2B	
1	1	0	0	0	0	30	P OR T
1	1	0	0	0	1	31	P AND T
1	1	0	0	1	0	32	P EXOR T
1	1	0	0	1	1	33	LOGICAL SHIFT P Q PLACES
1	1	0	1	0	0	34	ARITHMETIC SHIFT P Q PLACES
1	1	0	1	0	1	35	FUNNEL SHIFT P-T Q PLACES
1	1	0	1	1	0	36	
1	1	0	1	1	1	37	
X	1	0	0	0	1	18	MOVE P
X	1	1	1	1	1	1F	LOAD MODE REGISTER

PSEL(0..3), QSEL(0..3), TSEL(0..3) SELECTION CHART

SEL3	SEL2	SEL1	SEL0	HEX	P, Q, T INPUT SELECTED
0	0	0	0	00	R REGISTER
0	0	0	1	01	S REGISTER
0	0	1	0	02	ZERO (0000 0000 0000 0000)
0	0	1	1	03	0.5 * (3FE0 0000 0000 0000)
0	1	0	0	04	1 (3FF0 0000 0000 0000)
0	1	0	1	05	2 (4000 0000 0000 0000)
0	1	1	0	06	3 (4080 0000 0000 0000)
0	1	1	1	07	PI ** (4009 21FB 5444 2D18)
1	0	0	0	08	REGISTER FILE 0
1	0	0	1	09	REGISTER FILE 1
1	0	1	0	0A	REGISTER FILE 2
1	0	1	1	0B	REGISTER FILE 3
1	1	0	0	0C	REGISTER FILE 4
1	1	0	1	0D	REGISTER FILE 5
1	1	1	0	0E	REGISTER FILE 6
1	1	1	1	0F	REGISTER FILE 7

* 0.5 (FLOATING POINT) OR -1 (INTEGER)
** PI (FLOATING POINT) OR MAX NEG (INTEG)

MODE WORD FOR FIR: 00 18 00 00



VLBA CORRELATOR PROJECT	
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA	
Title	FIR FLOATING POINT CHIP
Size: C	Document Number: 56000L031 (L031D05.SCH) REV:
Date: October 9, 1991	Sheet 5 of 5

29C327 TO DRAM CROSSBAR

SENBL\ ENABLES OUTPUT TO S BUS.

FTOA\ — A[0..31] / B[0..31] — DRAMS

F[0..31] / S[0..31] — A[0..31] / B[0..31] — FTOA

29C327: ADR[0..31] ADR[0..3], FSTBL\ FSTBL

S[0..31] TOuP[0..7] TOuP[0..7]

A4,3 AND A6,5 SPECIFIY THE ADDRESS AT THE CROSSBAR EACH TO 4 CHIPS FOR FANOUT

SELECTION	ADDRESS
0	0000000 8000
1	0101000 8028
2	1010000 8050
3	1111000 8078

BENBL\	AENBL\	A	B	S
0	0	HIZ	HIZ	F
F TO B	0	1	HIZ	F	A
F TO A	1	0	F	HIZ	B
F TO S	1	1	HIZ	HIZ	F

SEE FIRPAL4A.ABL
SEE L031D22 FOR DESCRIPTION

26E 27E 28E 29E 30E 31E — 29MA16R-25PC

FROM 22V10, SO =1 IF NO CLK TO PREVENT XBAR TO DRAM BUS CONTENTION

AENBL\ = FTOA\

BENBL\ = FTOA

R7 4.7K PU7

VCC GND

BACKEND SNAPSHOT REGISTER

TAKES A SNAPSHOT OF THE SELECTED RAM BANK OUTPUT FOR THE BACKEND. ANCILLARY FUNCTION IS TO PROTECT THE 327 FROM POSSIBLE BUS CONTENTION.

SEE L031D08 FOR DRAM TIMING
SEE L031D14 FOR DRAM ADDRESS TIMING

EXTRA STAGE OF DELAY IN 13 AND 57 ADDRESS SO ROW AND COLUMN LINE UP CORRECTLY. SEE L031D14 FOR EXPLANATION.

ON SHT 6

beADR9 COMES FROM SEPARATE MUX FOR THE OUTPUT BUFFER BITS 0 THRU 8 ARE DERIVED AS ABOVE.

REGISTER TAKES UP DIFFERENCE DELAYS FROM DIFFERENT ADDRESS SOURCES.

SEE L031D11.SCH FOR RAM LOADING SOFTWARE

CLR\ TIMING
163 OUT 11 NS
7C122 RAM 25 NS
7C199 RAM 35 NS
ALS00 11 NS
ALS02 12 NS
163 CLR\ SU 12 NS
106 NS 125 AVAIL

DIFFERENT BIT 9, SINCE BANK SWITCHED DIFFERENTLY IN THE MAIN SECTION, THE BANK BIT CHOSES 0 OR 2, ETC. HERE IT CHOSES WHETHER THE be OR FIR USES THE BANK.

USE FOR 4*125NS DELAY

FROM 8 TO 1 MUX

PS15

SEE FIRPAL5
SEE L031D18 FOR PAL DESC

DELTA0 = 0
DELTA1 = 1

ADDRESS CHANGES EVERY 1 uSEC.

THE LARGEST DUMP IS 105 BASELINES * 2048 RESULTS = 214,016 ADDRESSES.
THIS IS 214 mS, WHICH IS BEYOND THE REFRESH RATE. HOWEVER, THE REFRESHES CAN BE DONE IN THE 1 IN 5, 2 uSEC REST, SINCE, THE DRAMS ARE NOT USED THEN, EXCEPT FOR BACKEND ACCESS. A REFRESH COUNTER CAN KEEP TRACK OF THE CURRENT ROW OF THE 512 TO BE REFRESHED. REFRESH REQUIRES 512 ACCESSES EVERY 8 MS. ONE ROW REFRESH/ 10 uSEC, REFRESHES ALL 512 ROWS (A0-A8) IN 5.12 MS.

TELL uP LAST RESULT OF BL

FIR ACKNOWLEDGES DATA FROM VME
ENDR' AND STATUS BIT TO VME FOR UNKNOWN PURPOSE
1 = DATA FROM THE FIR TO THE VME

BACKEND FIFO OUTPUT CLOCK

CLOCK BL, SUB REG AND COUNTER
RESULT COUNTER CLEAR\

FIR REQUESTS TO SEND DATA TO VME

22V10 W0 RINGING
SEE L031D16.SCH FOR PAL DESCRIPTION & HANDSHAKE TIMING.
SEE L031D07 FOR be BLOCK DIAGRAM

SEE FIRPAL6B

DONE WITH COUNT OF ACK'S

SEE FIRPAL9A.ABL
SEE L031D28.SCH FOR PAL DESCRIPTION

COULD GET RID OF CHIP IF NEED BE.

DETERMINES 8 BIT BUS DIRECTION
ENDR 1 = VME TO FIR

CTL1 SIGNAL XFER RQST
NO CURRENT DESTINATION

CTL2

CTL3

TO uP TO SEE IF VME STILL READING FIFO.

beSUB[0..2] IS THE SUBARRAY FOR THAT BASELINE.

4K FIFO CAN HOLD A WHOLE BASELINE'S OF CPX RESULTS.

SEE L031D17 FOR TIMING

VMEACK'' WAS DLYRC. SIGNAL ADDED 3/17/93

VMEREQ'' VMEREQ ASYCH TO SYNC

6 CNT DLY

SO SAME PIPELINING

31 NS DLY

FOR STRAIGHT THRU MODE SEE L031D27

STATUS NOT PRESENTLY USED

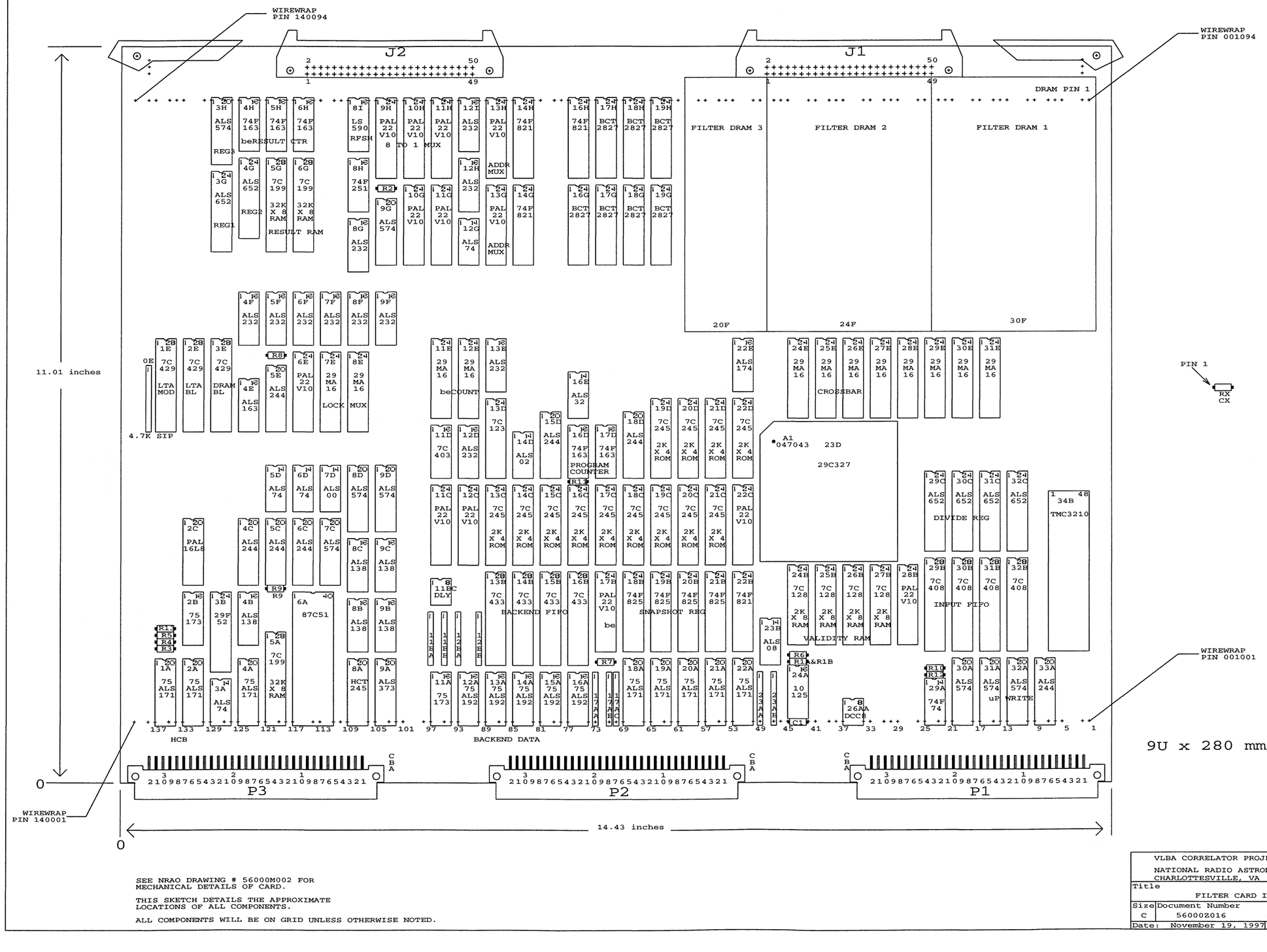
THE RAMS ARE LOADED VIA THE uADR[0..19] BUS
THIS IS THE uP DELIVERABLE ADDRESS.
THE RAMS CAN BE READ BACK TO THE uP VIA THIS AS WELL.
NOTE THE 4 MSB'S ARE WIRED RED TO PROVIDE THE SUBARRAY

TO uP ADDRESS REGISTER FOR LOADING RAM.

ALSO TO ADDRESS MUX

beLMSB TELLS WHETHER TO THROW AWAY THE RESULT OR BL MSB. FOR THAT BASELINE. 0 = 2048 RESULTS/BL.
beLMSB TO SHT. 1 PAL 11G VIA uADR11.

Title	VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA FIR DRAMS AND CROSSBAR
Size	D
Document Number	56000L031 (L031D06.SCH)
REV	
Date:	July 25, 1996
Sheet	6 of 41



SEE NRAO DRAWING # 56000M002 FOR MECHANICAL DETAILS OF CARD.

THIS SKETCH DETAILS THE APPROXIMATE LOCATIONS OF ALL COMPONENTS.

ALL COMPONENTS WILL BE ON GRID UNLESS OTHERWISE NOTED.

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: FILTER CARD IC LAYOUT

Size	Document Number	REV
C	56000Z016 (Z016D01.LAY)	

Date: November 19, 1997 Sheet 1 of 4

3 Ironics Transition Module Schematics

MATING CONNECTOR FOR CABLE
FROM IRONICS IV-3272

J3C (DIN)

1	IOBUS31
2	IOBUS30
3	IOBUS29
4	IOBUS28
5	IOBUS27
6	IOBUS26
7	IOBUS25
8	IOBUS24
9	IOBUS23
10	IOBUS22
11	IOBUS21
12	IOBUS20
13	IOBUS19
14	IOBUS18
15	IOBUS17
16	IOBUS16
17	iCTRL7
18	iCTRL6
19	iCTRL5
20	iCTRL4
21	iCTRL3
22	iCTRL2
23	iCTRL1
24	iCTRL0
25	iSTATUS7
26	iSTATUS6
27	iSTATUS5
28	iSTATUS4
29	iSTATUS3
30	iSTATUS2
31	iSTATUS1
32	iSTATUS0

J3A (DIN)

1	IOBUS15
2	IOBUS14
3	IOBUS13
4	IOBUS12
5	IOBUS11
6	IOBUS10
7	IOBUS9
8	IOBUS8
9	IOBUS7
10	IOBUS6
11	IOBUS5
12	IOBUS4
13	IOBUS3
14	IOBUS2
15	IOBUS1
16	IOBUS0
17	iREQ*
18	iACK*
19	
20	
21	
22	
23	iENDIR
24	
25	
26	
27	
28	
29	
30	
31	
32	

GNDS FOR TWISTED PAIRS

PU1

4A, 2B, 2C, 2D, 2E, 4F, 3A, 3B, 3C, 3D, 3E — 75ALS170

4A	C 2	C	1DIR 1A	1D 1B	13 ENDIR	14 ENDIR\					
	C 5	IOBUS31 4	2DIR 2A	2D 2B	10 beD31	11 beD\31					
	C 7	IOBUS30 6	3DIR 3A	3D 3B	8 beD30	9 beD\30					
2B	C 2	IOBUS29 1	1DIR 1A	1D 1B	13 beD29	14 beD\29					
	C 5	IOBUS28 4	2DIR 2A	2D 2B	10 beD28	11 beD\28					
	C 7	IOBUS27 6	3DIR 3A	3D 3B	8 beD27	9 beD\27					
2C	C 2	IOBUS26 1	1DIR 1A	1D 1B	13 beD26	14 beD\26					
	C 5	IOBUS25 4	2DIR 2A	2D 2B	10 beD25	11 beD\25					
	C 7	IOBUS24 6	3DIR 3A	3D 3B	8 beD24	9 beD\24					
2D	A 2	IOBUS23 1	1DIR 1A	1D 1B	13 beD23	14 beD\23					
	A 5	IOBUS22 4	2DIR 2A	2D 2B	10 beD22	11 beD\22					
	A 7	IOBUS21 6	3DIR 3A	3D 3B	8 beD21	9 beD\21					
2E	A 2	IOBUS20 1	1DIR 1A	1D 1B	13 beD20	14 beD\20					
	A 5	IOBUS19 4	2DIR 2A	2D 2B	10 beD19	11 beD\19					
	A 7	IOBUS18 6	3DIR 3A	3D 3B	8 beD18	9 beD\18					
4F	B 2	IOBUS17 1	1DIR 1A	1D 1B	13 beD17	14 beD\17					
	B 5	IOBUS16 4	2DIR 2A	2D 2B	10 beD16	11 beD\16					
	B 7	IOBUS15 6	3DIR 3A	3D 3B	8 beD15	9 beD\15					
3A	B 2	IOBUS14 1	1DIR 1A	1D 1B	13 beD14	14 beD\14					
	B 5	IOBUS13 4	2DIR 2A	2D 2B	10 beD13	11 beD\13					
	B 7	IOBUS12 6	3DIR 3A	3D 3B	8 beD12	9 beD\12					
3B	A 2	IOBUS11 1	1DIR 1A	1D 1B	13 beD11	14 beD\11					
	A 5	IOBUS10 4	2DIR 2A	2D 2B	10 beD10	11 beD\10					
	A 7	IOBUS9 6	3DIR 3A	3D 3B	8 beD9	9 beD\9					
3C	A 2	IOBUS8 1	1DIR 1A	1D 1B	13 beD8	14 beD\8					
	A 5	IOBUS7 4	2DIR 2A	2D 2B	10 beD7	11 beD\7					
	A 7	IOBUS6 6	3DIR 3A	3D 3B	8 beD6	9 beD\6					
3D	B 2	IOBUS5 1	1DIR 1A	1D 1B	13 beD5	14 beD\5					
	B 5	IOBUS4 4	2DIR 2A	2D 2B	10 beD4	11 beD\4					
	B 7	IOBUS3 6	3DIR 3A	3D 3B	8 beD3	9 beD\3					
3E	B 2	IOBUS2 1	1DIR 1A	1D 1B	13 beD2	14 beD\2					
	B 5	IOBUS1 4	2DIR 2A	2D 2B	10 beD1	11 beD\1					
	B 7	IOBUS0 6	3DIR 3A	3D 3B	8 beD0	9 beD\0					

VCC= PIN 12
GND= PIN 3

A SIZE SHEET
L044D02.SCH TERMINATIONS

beD[0..31] — beD[0..31]
beD\[0..31] — beD\[0..31]
REQ* — REQ*
REQ*\ — REQ*\
ACK* — ACK*
ACK*\ — ACK*\
ENDIR — ENDIR
ENDIR\ — ENDIR\
CTRL[1..4] — CTRL[1..4]
CTRL\[1..4] — CTRL\[1..4]
STAT[1..4] — STAT[1..4]
STAT\[1..4] — STAT\[1..4]

RN1, RN2, PU1

L044D02.SCH

J1 (3M50)

beD15	1	2	beD\15
beD14	3	4	beD\14
beD13	5	6	beD\13
beD12	7	8	beD\12
beD11	9	10	beD\11
beD10	11	12	beD\10
beD9	13	14	beD\9
beD8	15	16	beD\8
beD7	17	18	beD\7
beD6	19	20	beD\6
beD5	21	22	beD\5
beD4	23	24	beD\4
beD3	25	26	beD\3
beD2	27	28	beD\2
beD1	29	30	beD\1
beD0	31	32	beD\0
REQ*	33	34	REQ*\
	35	36	
ACK*	37	38	ACK*\
	39	40	
ENDIR	41	42	ENDIR\
	43	44	
	45	46	
	47	48	
	49	50	

J2 (3M50)

beD31	1	2	beD\31
beD30	3	4	beD\30
beD29	5	6	beD\29
beD28	7	8	beD\28
beD27	9	10	beD\27
beD26	11	12	beD\26
beD25	13	14	beD\25
beD24	15	16	beD\24
beD23	17	18	beD\23
beD22	19	20	beD\22
beD21	21	22	beD\21
beD20	23	24	beD\20
beD19	25	26	beD\19
beD18	27	28	beD\18
beD17	29	30	beD\17
beD16	31	32	beD\16
	33	34	
CTRL4	35	36	CTRL\4
CTRL3	37	38	CTRL\3
CTRL2	39	40	CTRL\2
CTRL1	41	42	CTRL\1
STAT4	43	44	STAT\4
STAT3	45	46	STAT\3
STAT2	47	48	STAT\2
STAT1	49	50	STAT\1

iENDIR — 2FA (74LS08) — 1CA (74LS86) — PU12

0= OUT FROM VME
1= IN TO VME

1F: IN OUT — MDLDL-TTL-20
1E: IN OUT — MDLDL-TTL-22

1CB (74LS86) — A
1CC (74LS86) — B
1CD (74LS86) — C

1=xmit

PU1 — 1A (75ALS171)

VCC= PIN 16
GND= PINS 4 & 5

17	CDE		
18	RE		
2	1DE	1A	19
3	1D	1B	20
1	1R		
7	2DE	2A	14 REQ*
8	2D	2B	15 REQ*\
6	2R		
10	3DE	3A	12 ACK*
11	3D	3B	13 ACK*\
9	3R		

NOTE:
ALWAYS RECEIVING,
(EVEN WHEN TRANSMITTING)

iREQ* — RN1 — 1B (74AS757)
iACK* — RN2

18	1Y1	1A1	2
16	1Y2	1A2	4
14	1Y3	1A3	6
12	1Y4	1A4	8
9	2Y1	2A1	11
7	2Y2	2A2	13
5	2Y3	2A3	15
3	2Y4	2A4	17
	1G		1
	2G		19

1D (75172)

iCTRL4	1	I0	B0 2 CTRL4
			B0 3 CTRL\4
iCTRL3	7	I1	B1 6 CTRL3
			B1 5 CTRL\3
iCTRL2	9	I2	B2 10 CTRL2
			B2 11 CTRL\2
iCTRL1	15	I3	B3 14 CTRL1
			B3 13 CTRL\1
PU1	4	OE	
	12	OE	

4G (75173)

iSTATUS4	3	O0	B0 2 STAT4
			B0 1 STAT\4
iSTATUS3	5	O1	B1 6 STAT3
			B1 7 STAT\3
iSTATUS2	11	O2	B2 10 STAT2
			B2 9 STAT\2
iSTATUS1	13	O3	B3 14 STAT1
			B3 15 STAT\1
		OE	4 PU1
		OE	12

A SIZE SHEET
L044D03.SCH IC LAYOUT

L044D03.SCH

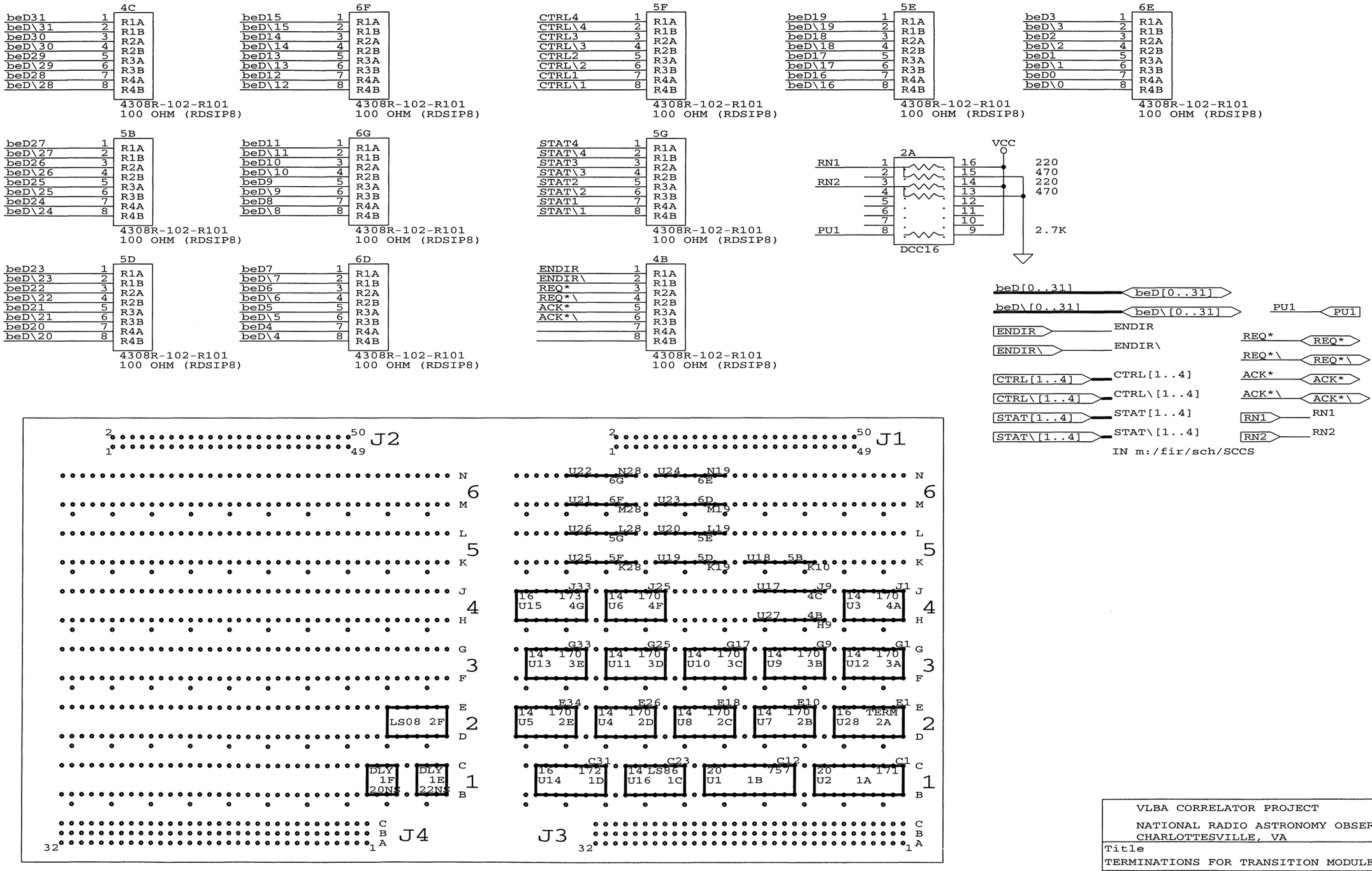
IN m:/fir/sch/SCCS

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: TRANSITION MODULE FOR IRONICS IV-3272

Size	Document Number	REV
B	56000L044 (L044D01.SCH)	

Date: January 21, 1998 | Sheet 1 of 3



VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

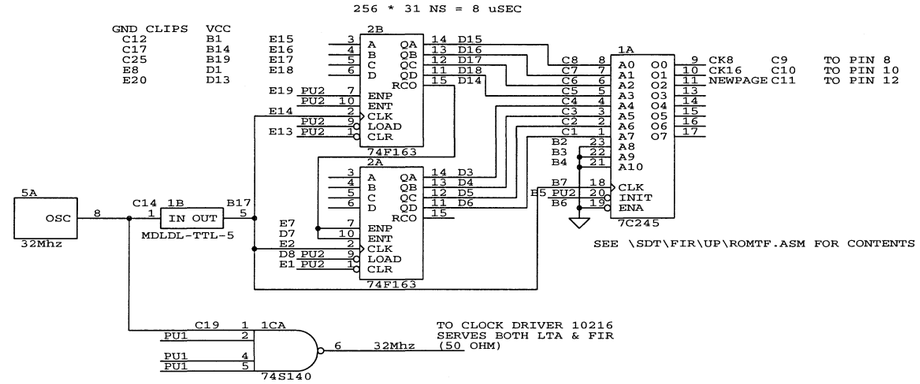
Title
TERMINATIONS FOR TRANSITION MODULE (IV-3272)

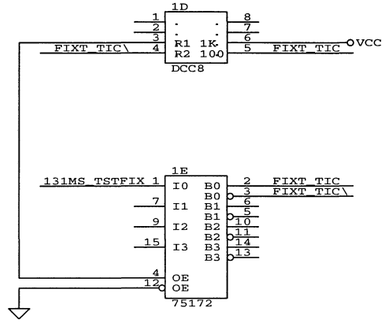
Size	Document Number	REV
B	56000L044 (L044D02.SCH)	

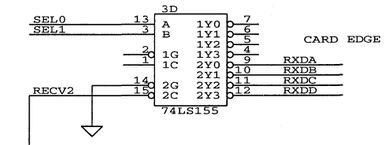
Date: May 15, 1998 Sheet 2 of 3

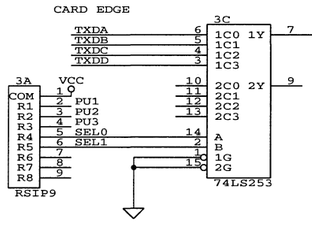
4 LTA/FIR Test Fixture Schematics

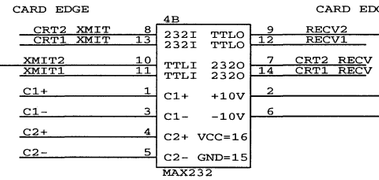
LTA/FIR TEST FIXTURE
CONTROL LOGIC

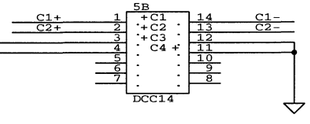


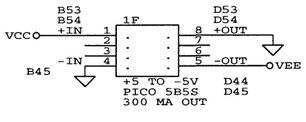


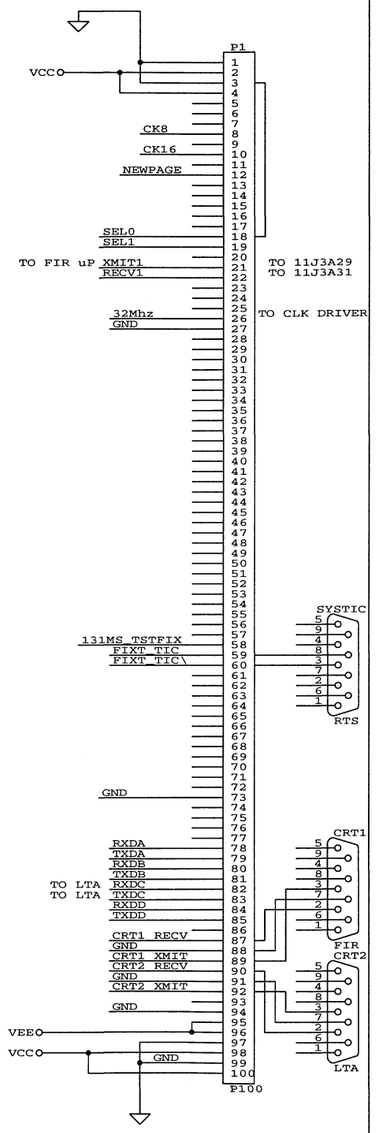






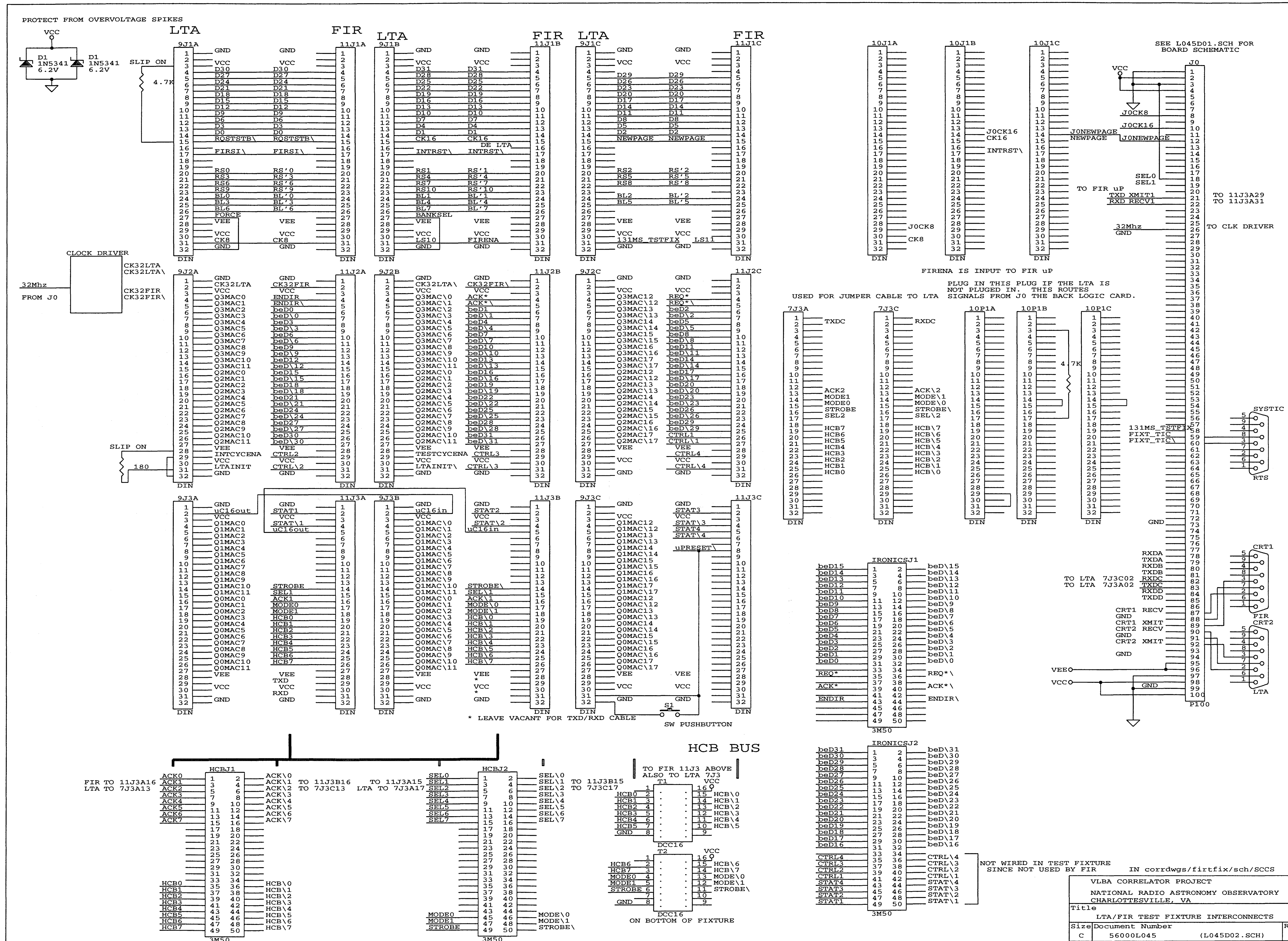






IN corrdwgs/firtfix/sch/SCCS

NATIONAL RADIO ASTRONOMY OBSERVATORY		
VLBA CORRELATOR		
Title: TEST FIXTURE CONTROL LOGIC 1		
Size: C	Document Number: L045D01.SCH	REV: A
Date: May 20, 1998	Sheet 1 of 1	


PROTECT FROM OVERVOLTAGE SPIKES
VCC
D1 1N5341 6.2V
D1 1N5341 6.2V
SLIP ON
4.7K
LTA
FIR
9J1A
11J1A
GND VCC D30 D27 D24 D21 D18 D15 D12 D9 D6 D3 D0 RQSTSTB\ FIRSI\ RS0 RS3 RS6 RS9 BL0 BL3 BL6 FORCE VEE VCC CK8 GND
GND VCC D30 D27 D24 D21 D18 D15 D12 D9 D6 D3 D0 RQSTSTB\ FIRSI\ RS'0 RS'3 RS'6 RS'9 BL'0 BL'3 BL'6 VEE VCC CK8 GND
9J1B
11J1B
GND VCC D31 D28 D25 D22 D19 D16 D13 D10 D7 D4 D1 CK16 INTRST\ RS1 RS4 RS7 RS10 BL1 BL4 BL7 BANKSEL VEE VCC LS10 GND
GND VCC D31 D28 D25 D22 D19 D16 D13 D10 D7 D4 D1 CK16 DE LTA INTRST\ RS'1 RS'4 RS'7 RS'10 BL'1 BL'4 BL'7 VEE VCC FIRENA GND
9J1C
11J1C
GND VCC D29 D26 D23 D20 D17 D14 D11 D8 D5 D2 NEWPAGE RS2 RS5 RS8 BL2 BL5 VEE VCC 131MS_TSTFIX GND
GND VCC D29 D26 D23 D20 D17 D14 D11 D8 D5 D2 NEWPAGE RS'2 RS'5 RS'8 BL'2 BL'5 VEE VCC LS11 GND
DIN
CLOCK DRIVER
32Mhz
FROM J0
CK32LTA
CK32LTA\
CK32FIR
CK32FIR\
9J2A
11J2A
GND CK32LTA VCC Q3MAC0 Q3MAC1 Q3MAC2 Q3MAC3 Q3MAC4 Q3MAC5 Q3MAC6 Q3MAC7 Q3MAC8 Q3MAC9 Q3MAC10 Q3MAC11 Q2MAC0 Q2MAC1 Q2MAC2 Q2MAC3 Q2MAC4 Q2MAC5 Q2MAC6 Q2MAC7 Q2MAC8 Q2MAC9 Q2MAC10 Q2MAC11 VEE INTCYCENA VCC LTAINIT GND
GND CK32FIR VCC ENDIR ENDIR\ beD0 beD\0 beD3 beD\3 beD6 beD\6 beD9 beD\9 beD12 beD\12 beD15 beD\15 beD18 beD\18 beD21 beD\21 beD24 beD\24 beD27 beD\27 beD30 beD\30 VEE CTRL2 VCC CTRL\2 GND
SLIP ON
180
9J2B
11J2B
GND CK32LTA\ VCC Q3MAC\0 Q3MAC\1 Q3MAC\2 Q3MAC\3 Q3MAC\4 Q3MAC\5 Q3MAC\6 Q3MAC\7 Q3MAC\8 Q3MAC\9 Q3MAC\10 Q3MAC\11 Q2MAC\0 Q2MAC\1 Q2MAC\2 Q2MAC\3 Q2MAC\4 Q2MAC\5 Q2MAC\6 Q2MAC\7 Q2MAC\8 Q2MAC\9 Q2MAC\10 Q2MAC\11 VEE TESTCYCENA VCC LTAINIT\ GND
GND CK32FIR\ VCC ACK* ACK*\ beD1 beD\1 beD4 beD\4 beD7 beD\7 beD10 beD\10 beD13 beD\13 beD16 beD\16 beD19 beD\19 beD22 beD\22 beD25 beD\25 beD28 beD\28 beD31 beD\31 VEE CTRL3 VCC CTRL\3 GND
9J2C
11J2C
GND VCC Q3MAC12 Q3MAC\12 Q3MAC13 Q3MAC\13 Q3MAC14 Q3MAC\14 Q3MAC15 Q3MAC\15 Q3MAC16 Q3MAC\16 Q3MAC17 Q3MAC\17 Q2MAC12 Q2MAC\12 Q2MAC13 Q2MAC\13 Q2MAC14 Q2MAC\14 Q2MAC15 Q2MAC\15 Q2MAC16 Q2MAC\16 Q2MAC17 Q2MAC\17 VEE VCC GND
GND VCC REQ* REQ*\ beD2 beD\2 beD5 beD\5 beD8 beD\8 beD11 beD\11 beD14 beD\14 beD17 beD\17 beD20 beD\20 beD23 beD\23 beD26 beD\26 beD29 beD\29 CTRL1 CTRL\1 VEE CTRL4 VCC CTRL\4 GND
9J3A
11J3A
GND uC16out VCC Q1MAC0 Q1MAC1 Q1MAC2 Q1MAC3 Q1MAC4 Q1MAC5 Q1MAC6 Q1MAC7 Q1MAC8 Q1MAC9 Q1MAC10 Q1MAC11 Q0MAC0 Q0MAC1 Q0MAC2 Q0MAC3 Q0MAC4 Q0MAC5 Q0MAC6 Q0MAC7 Q0MAC8 Q0MAC9 Q0MAC10 Q0MAC11 VEE VCC GND
GND STAT1 VCC STAT\1 uC16out STROBE SEL1 ACK1 MODE0 MODE1 HCB0 HCB1 HCB2 HCB3 HCB4 HCB5 HCB6 HCB7 VEE TXD VCC RXD GND
9J3B
11J3B
GND uC16in VCC Q1MAC\0 Q1MAC\1 Q1MAC\2 Q1MAC\3 Q1MAC\4 Q1MAC\5 Q1MAC\6 Q1MAC\7 Q1MAC\8 Q1MAC\9 Q1MAC\10 Q1MAC\11 Q0MAC\0 Q0MAC\1 Q0MAC\2 Q0MAC\3 Q0MAC\4 Q0MAC\5 Q0MAC\6 Q0MAC\7 Q0MAC\8 Q0MAC\9 Q0MAC\10 Q0MAC\11 VEE VCC GND
GND STAT2 VCC STAT\2 uC16in STROBE\ SEL\1 ACK\1 MODE\0 MODE\1 HCB\0 HCB\1 HCB\2 HCB\3 HCB\4 HCB\5 HCB\6 HCB\7 VEE * VCC * GND
9J3C
11J3C
GND VCC Q1MAC12 Q1MAC\12 Q1MAC13 Q1MAC\13 Q1MAC14 Q1MAC\14 Q1MAC15 Q1MAC\15 Q1MAC16 Q1MAC\16 Q1MAC17 Q1MAC\17 Q0MAC12 Q0MAC\12 Q0MAC13 Q0MAC\13 Q0MAC14 Q0MAC\14 Q0MAC15 Q0MAC\15 Q0MAC16 Q0MAC\16 Q0MAC17 Q0MAC\17 VEE VCC GND
GND STAT3 VCC STAT\3 STAT4 STAT\4 uPRESET\ VEE VCC GND
* LEAVE VACANT FOR TXD/RXD CABLE
S1
SW PUSHBUTTON
10J1A
J0CK8
CK8
10J1B
J0CK16
CK16
INTRST\
10J1C
J0NEWPAGE
NEWPAGE
FIRENA IS INPUT TO FIR uP
SEE L045D01.SCH FOR BOARD SCHEMATIC
J0
VCC
J0CK8
J0CK16
J0NEWPAGE
SEL0
SEL1
TO FIR uP
TXD XMIT1
RXD RECV1
TO 11J3A29
TO 11J3A31
32Mhz
GND
TO CLK DRIVER
PLUG IN THIS PLUG IF THE LTA IS NOT PLUGED IN. THIS ROUTES SIGNALS FROM J0 THE BACK LOGIC CARD.
USED FOR JUMPER CABLE TO LTA
7J3A
TXDC ACK2 MODE1 MODE0 STROBE SEL2 HCB7 HCB6 HCB5 HCB4 HCB3 HCB2 HCB1 HCB0
7J3C
RXDC ACK\2 MODE\1 MODE\0 STROBE\ SEL\2 HCB\7 HCB\6 HCB\5 HCB\4 HCB\3 HCB\2 HCB\1 HCB\0
10P1A
10P1B
4.7K
10P1C
SYSTIC
131MS_TSTFIX
FIXT_TIC
FIXT_TIC\
RTS
GND
RXDA TXDA RXDB TXDB RXDC TXDC RXDD TXDD
TO LTA 7J3C02
TO LTA 7J3A02
CRT1 RECV
GND
CRT1 XMIT
CRT2 RECV
GND
CRT2 XMIT
GND
CRT1
FIR
CRT2
LTA
VEE
VCC
GND
P100
IRONICSJ1
beD15 beD14 beD13 beD12 beD11 beD10 beD9 beD8 beD7 beD6 beD5 beD4 beD3 beD2 beD1 beD0 REQ* ACK* ENDIR
beD\15 beD\14 beD\13 beD\12 beD\11 beD\10 beD\9 beD\8 beD\7 beD\6 beD\5 beD\4 beD\3 beD\2 beD\1 beD\0 REQ*\ ACK*\ ENDIR\
3M50
IRONICSJ2
beD31 beD30 beD29 beD28 beD27 beD26 beD25 beD24 beD23 beD22 beD21 beD20 beD19 beD18 beD17 beD16 CTRL4 CTRL3 CTRL2 CTRL1 STAT4 STAT3 STAT2 STAT1
beD\31 beD\30 beD\29 beD\28 beD\27 beD\26 beD\25 beD\24 beD\23 beD\22 beD\21 beD\20 beD\19 beD\18 beD\17 beD\16 CTRL\4 CTRL\3 CTRL\2 CTRL\1 STAT\4 STAT\3 STAT\2 STAT\1
NOT WIRED IN TEST FIXTURE SINCE NOT USED BY FIR
HCBJ1
FIR TO 11J3A16
LTA TO 7J3A13
ACK0 ACK1 ACK2 ACK3 ACK4 ACK5 ACK6 ACK7
ACK\0 ACK\1 ACK\2 ACK\3 ACK\4 ACK\5 ACK\6 ACK\7
TO 11J3B16
TO 7J3C13
HCB0 HCB1 HCB2 HCB3 HCB4 HCB5 HCB6 HCB7
HCB\0 HCB\1 HCB\2 HCB\3 HCB\4 HCB\5 HCB\6 HCB\7
HCBJ2
TO 11J3A15
LTA TO 7J3A17
SEL0 SEL1 SEL2 SEL3 SEL4 SEL5 SEL6 SEL7
SEL\0 SEL\1 SEL\2 SEL\3 SEL\4 SEL\5 SEL\6 SEL\7
TO 11J3B15
TO 7J3C17
MODE0 MODE1 STROBE
MODE\0 MODE\1 STROBE\
HCB BUS
TO FIR 11J3 ABOVE
ALSO TO LTA 7J3
T1
VCC
HCB0 HCB1 HCB2 HCB3 HCB4 HCB5 GND
HCB\0 HCB\1 HCB\2 HCB\3 HCB\4 HCB\5
DCC16
T2
VCC
HCB6 HCB7 MODE0 MODE1 STROBE GND
HCB\6 HCB\7 MODE\0 MODE\1 STROBE\
DCC16
ON BOTTOM OF FIXTURE
IN corrdwgs/firtfix/sch/SCCS
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title
LTA/FIR TEST FIXTURE INTERCONNECTS
Size Document Number REV
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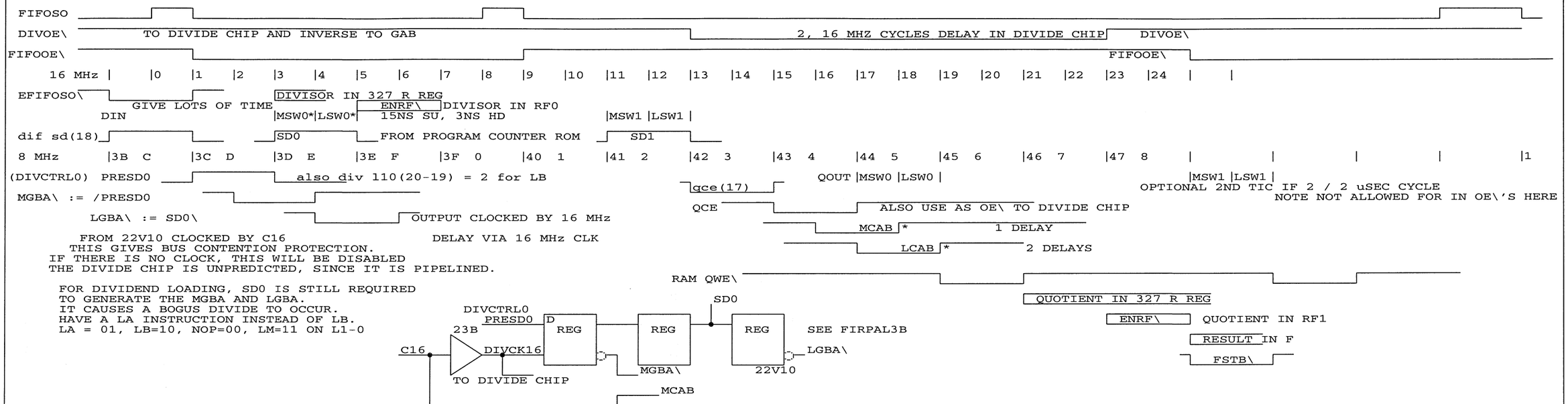
5 FIR Timing Charts and Diagrams

HAVE MODE REGISTER AND A REGISTOR INITIALLY LOADED
BASED ON 2 VALIDITIES AVAILABLE EVERY 2 uSEC

THIS SECOND TIC WILL READ THE DUPLICATE VALUE IF 1 VALIDITY / 2 uSEC.

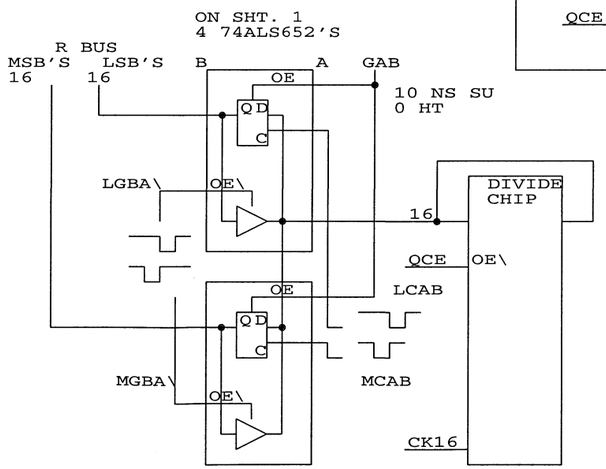


FROM 22V10 CLOCKED BY C16
THIS GIVES BUS CONTENTION PROTECTION.
IF THERE IS NO CLOCK, THIS WILL BE DISABLED
THE DIVIDE CHIP IS UNPREDICTED, SINCE IT IS PIPELINED.

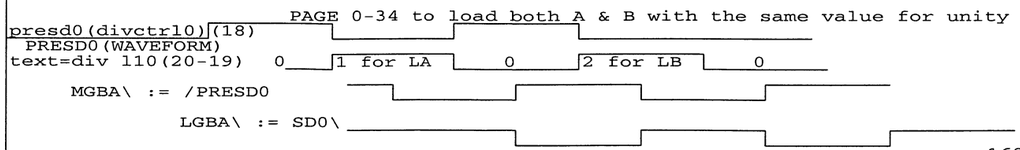
FOR DIVIDEND LOADING, SD0 IS STILL REQUIRED
TO GENERATE THE MGBA AND LGBA.
IT CAUSES A BOGUS DIVIDE TO OCCUR.
HAVE A LA INSTRUCTION INSTEAD OF LB.
LA = 01, LB=10, NOP=00, LM=11 ON L1-0

NEED MCAB NOT TO BE > 5 NS AFTER CK16

QUOTIENT IN 327 R REG
ENRF\ QUOTIENT IN RF1
RESULT IN F
FSTB\



PAGE 0-34 to load both A & B with the same value for unity divide output



Divides started by ST0 are needless.

For non normalized mode (Page 3), have no LA's present.
It will then use the LA from Page 0-34.

1680 VALIDITES = 210 BASELINES OF 8 CHANNELS
uP RESETS ADDRESS FIFO'S
ALSO 4, 131 MS CYCLES WORTH OF VALIDITIES GET STORED IN THE
BACKEND BUFFER, FOR READING EACH BANKSWITCH.
THE BACKEND HAS ACCESS TO ALL VALIDITES INPUT.

TO PROCESS VALIDITIES

HAVE THE uP:

LOCK BASELINE TO LTA TO 210.
LOAD LTA BASELINE FIFO WITH 0 TO 209
LOAD MODULUS FIFO WITH 0 210 TIMES (SEE L031D15)
(THIS GIVES MODULUS 2048 WITH LTABL EVERY 8. DRBL AT 0 AND 1680)
LOAD DRAM BASELINE FIFO WITH THE be BUFFER DESTINATION BASELINE.
(THIS WILL CYCLE 0,1,2,3 EVERY 4*131MS CYCLES)
WRITE BRANCH REG WITH LOAD VALIDITY ROUTINE
WRITE PCINT\
WRITE BRANCH REG WITH EXIT ROUTINE

HAVE THE PC SEQUENCER:
RESET THE INPUT FIFO
GIVE A RESCNT & RESCLR\ TO CLR COUNTER & READ ALL 3 ADR FIFO'S
CLOCK ADDRESS INTO DELAY FIFOS
SEND A RQSTSTB\ TO THE LTA FOR A VALIDITY TO PRIME THE FIFO
WAIT 2 uSEC (16 INSTRUCTIONS)
THIS ALLOWS THE LTA'S 2uSEC LOOP TO BE AN ARBITRARY
PHASE OFFSET FROM MY 2 uSEC LOOP.
* GIVE A RESCNT
CLOCK ADDRESS INTO DELAY FIFOS
GIVE A RQSTSTB\
2 uSEC LOOP READ THE INPUT FIFO
CLOCK INTO 327
DO VALCUNCK & LDLYUNCK TO RECALL PREVIOUS VALUE
DO THE ABOVE DIVIDE AND STORE THE RESULT IN RAM
STORE THE 327 VALUE IN THE be BUFFER
IF DRAMBL FIFO NOT EMPTY
LOOP BACK TO *

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
DIVIDER TIMING

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lower case means actual value in prom before reg
nc = not clocked in 327

PAGE 2 ->| PAGE 1 ->|

	AF	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75
instruction	r*r0+s	dummy	f=r	f=r	f=r	f=r	f=r*r4	f=r*r4	f=r*r5	f=r*r5	f=r*r6	f=r*r6	f=r*r7	f=r*r7	f=r	f=r	f=r	r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r0+s	
R INPUT	TW7			VAL0	VAL1	VAL2	VAL3	RE0	IM0	RE1	IM1	RE2	IM2	RE3	IM3	RIN	HiZ	HiZ	TW0	TW1	TW2	TW3	TW4
R REG							R4=VAL0	R5=VAL1	R6=VAL2	R7=VAL3	R0 =RE0 *VAL0	R1 =IM0 *VAL0	R2 =RE1 *VAL1	R3 =IM1 *VAL1	R4 =RE2 *VAL2	R5 =IM2 *VAL2	R6 =RE3 *VAL3	R7 =IM3 *VAL3					
rfsel(24-26)(number) & enrf\(27)	(waveform)			4	5	6	7	0	1	2	3	4	5	6	7								
oemuxg\-ba		1-3none	0-2 ram	0-2 ram	0-2 ram	0-2 ram	0-0fifo	0-0fifo	0-0fifo	0-0fifo	0-0fifo	0-0fifo	0-0fifo	0-0fifo	0-0fifo	1-0	1-2	0-2 ram	0-2 ram	0-2 ram	0-2 ram	0-2 ram	0-2
efifoso\(68) #, FIFOSO	(waveform)	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
vadroe(65)		0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
evalunck\(62)		1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1						
fstb(16)		CAPTURE	VAL0																				
rqststb\(66)																							
rescnt(57)																							
													clacenbl\(3)										
tw(0-2)																		tw0	tw1	tw2	tw3	tw4	tw5
SUBARRAY FROM DELAY FIFO																							

ok to go ram to fifo

INITIALLY:
LOAD A BASELINE, DRAM BASELINE, MODULUS AND SUBARRAY
LOAD VALIDITY RAMS

VAL0 0 0 0000000
VAL1 0 1 0000000
VAL2 0 2 0000000
VAL3 0 3 0000000

60	DUMMY INSTRUCTION	FOLLOWING LAST MAC	BC T15*R7+ACCi28
61	VAL0	STRAIGHT THRU	BD T11*R7+ACCi29
62	VAL1	STRAIGHT THRU	BE T7*R7+ACCi30
63	VAL2	STRAIGHT THRU	BF T3*R7+ACCi31
64	VAL3	STRAIGHT THRU	61 R4=VAL0
65	RE0	RE0*R4	62 R5=VAL1
66	IM0	IM0*R4	63 R6=VAL2
67	RE1	RE1*R5	64 R7=VAL3
68	IM1	IM1*R5	65 R0=RE0*VAL0
69	RE2	RE2*R6	66 R1=IM0*VAL0
6A	IM2	IM2*R6	67 R2=RE1*VAL1
6B	RE3	RE3*R7	68 R3=IM1*VAL1
6C	IM3	IM3*R7	69 R4=RE2*VAL2
6D	R IN	STRAIGHT THRU	6A R5=IM2*VAL2
6E	S IN	STRAIGHT THRU	6B R6=RE3*VAL3
			6C R7=IM3*VAL3
	FILTER 32 RESULTS		OUTPUT =
70	T0	ACCr0	T0*R0+0	6D R IN
71	T28	ACCr1	T28*R0+ACCr1	6E S IN
72	T24	ACCr2	T24*R0+ACCr2	
73	T20	ACCr3	T20*R0+ACCr3	
74	T16	ACCr4	T16*R0+ACCr4	70 T0*R0+0
75	T12	ACCr5	T12*R0+ACCr5	71 T28*R0+ACCr1
76	T8	ACCr6	T8*R0+ACCr6	72 T24*R0+ACCr2
77	T4	ACCr7	T4*R0+ACCr7	73 T20*R0+ACCr3
78	T0	ACCi0	T0*R1+0	74 T16*R0+ACCr4
79	T28	ACCi1	T28*R1+ACCi1	75 T12*R0+ACCr5
7A	T24	ACCi2	T24*R1+ACCi2	76 T8*R0+ACCr6
7B	T20	ACCi3	T20*R1+ACCi3	77 T4*R0+ACCr7
7C	T16	ACCi4	T16*R1+ACCi4	78 T0*R1+0
7D	T12	ACCi5	T12*R1+ACCi5	79 T28*R1+ACCi1
7E	T8	ACCi6	T8*R1+ACCi6	8A T24*R1+ACCi2
7F	T4	ACCi7	T4*R1+ACCi7	8B T20*R1+ACCi3
				8C
				8D
				8E
				8F

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
MAIN LOOP INITIALIZATION TIMING

Size	Document Number	REV
B	56000L031 (L031D12.SCH)	

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RR = READ ROW
RC = READ COLUMN DATA AVAILABLE
WR = WRITE ROW
WC = WRITE COLUMN DATA WRITTEN
* = 8TO1 MUX OUTPUT

ALL WRITE ADDRESSES ARE DELAYED READ ADDRESSES
THE MUX HAS SWITCHED READ AND WRITE.

NOTE 13 EQUALS 02 DELAYED BY ONE CLOCK CYCLE.
NOTE 57 EQUALS 46 DELAYED BY ONE CLOCK CYCLE.

89 ADDRESS IS 57 ADDRESS DELAYED ONE CLOCK CYCLE

WHERE THE NUMBER IS THE DESTINATION DRAM BANK.

preasel
0 row lta
1 col lta
7 row rfsh
2 row be
6 col be

SINGLE LTA ADDRESS FOR A COMPLEX LTA VALUE RECEIVED

THE SIGNALS IMAG AND OUTBANK SPECIFY WHICH QUADRANT IN THE RAM THE DATA GOES TO.

```
                        vadroe(65)                                                  SNAPOE\(WE\8)
                         rcntenbl(69)          DRAM BANK                             EESNAPOE(from CLAC ram when TW=7)
                          preasel(8-10)     MEMORY ADDRESS                            dlyrc(71)
                           deltoa(15)       ACCESSES                                   10ustic(70)
                            8TO1 PROM  0   1     4     5     8                         1clacenbl\(3)
                            MUX  ADDR  2   3     6     7     9  we\                    11tw(0-2)
                        0020       5E                               precas\            110prebaenbl\(11-12)
                        0160*be0   5F                            40 85410              1103SNAPCE\ FOR SNAP OF 0
                        0020*be0 60 *be0 2uSEC PAUSE          11 11111 1101103XEESNAPCE\(from CLAC ram for snap of 0)
                        1160*be1 61 *be0 be0                  11 11111 1101103XXCLACP\ FROM FIRPAL10
                        1020*be1 62 *be1 be0                  11 11111 1101103XX1CLAC\(from CLAC ram to clac 0)
                        1160*be2 63 *be1 be1                  11 11111 1101103XX1XTW(0-2)
                        1020*be2 64 *be2 be1 be0              11 11111 1101103XX1X0rescnt(57)
                        0160*be3 65 *be2 be2 be0 be0          11 11111 1101103XX1X00
                        0020*be3 66 *be3 be2 be1 be0 be0      11 01111 1111103XX1X00
                        0160*be4 67 *be3 be3 be1 be1 be0      11 11111 1101103XX1X00
                        0020*be4 68 *be4 be3 be2 be1 be1      11 01111 1111103XX1X00
                        0160*be5 69 *be4 be4 be2 be2 be1      11 11111 1101103XX1X00
                        0020*be5 6A *be5 be4 be3 be2 be2      11 01111 1111103XX1X00
                        0160*be6 6B *be5 be5 be3 be3 be2      11 11111 1101103XX1X00
                        0070*be6 6C *be6 be5 be4 be3 be3      11 01111 1111103XX1X00   89
                        0070*RFR 6D *be6 be6 be4 be4 be3      11 11111 1101103XX1X00   DATA
        DATA            0000*RFR 6E *RFR be6 be5 be4 be4      11 01111 1111103XX1X00
         IN             0010*RR0 6F *RFR RFR be5 be5 be4      11 11111 1101101XX1X00
                        0000*RC0 70 *RR0 RFR be6 be5 be5      11 01110 1111001XX1X00
        RReal0          0010*RR2 71 *RC0 RR1 be6 be6 be5      11 11101 1101011X01000
        RReal1          0001*RC2 72 *RR2 RC1 RFR be6 be6      11 01110 1111021X10110 DATA SNAPSHOT IS OF Wreal OR Wimag 0 THRU 7
        RReal2          0011*RR4 73 *RC2 RR3 RFR RFR be6      11 11101 1101032X11120 THE NUMBER IS SPECIFIED BASED ON SUBARRAY.
        RReal3  OUT     0001*RC4 74  WR0 RC3 *RR4 RFR RFR     10 11010 1101042X11130
        RReal4  WReal0  0011*RR6 75  WC0 WR1 *RC4 RR5 RFR     11 10101 1101052011140       RFR=REFRESH ADDRESS
        RReal5  WReal1  0000*RC6 76  WR2 WC1 *RR6 RC5         10 11010 1101062111150 NORMALLY THE ADDRESS MUX THROWS EVERY
        RReal6  WReal2  0010*RR0 77  WC2 WR3 *RC6 RR7         11 10101 1100071111160 4 CYCLES.  FOR be ACCESS, AT THE END OF
        RReal7  WReal3  0000*RC0 78 *RR0 WC3 WR4 RC7          01 11010 1000001111170 THE 2 USEC PAUSE, LEAVE ADR MUX IN THE
        RImag0  WReal4  0010*RR2 79 *RC0 RR1 WC4 WR5          11 10101 1100011101000 0 POSITION.
        RImag1  WReal5  0001*RC2 7A *RR2 RC1 WR6 WC5          01 11010 1100021110110
        RImag2  WReal6  0011*RR4 7B *RC2 RR3 WC6 WR7          11 10101 1100032111120
        RImag3  WReal7  0001*RC4 7C  WR0 RC3 *RR4 WC7 WR7     10 01010 1100042111130
        RImag4  WImag0  0011*RR6 7D  WC0 WR1 *RC4 RR5 WC7     11 10101 0100052011141 REAL DATA SNAPSHOT
        RImag5  WImag1  0000*RC6 7E  WR2 WC1 *RR6 RC5         10 11010 1100062111150
        RImag6  WImag2  0010*RR0 7F  WC2 WR3 *RC6 RR7         11 10101 1100071111160
        RImag7  WImag3  0000*RC0 80 *RR0 WC3 WR4 RC7          01 11010 1000001111170
        RReal0  WImag4  0010*RR2 81 *RC0 RR1 WC4 WR5          11 10101 1100011101000
        RReal1  WImag5  0001*RC2 82 *RR2 RC1 WR6 WC5          01 11010 1100021110110
        RReal2  WImag6  0011*RR4 83 *RC2 RR3 WC6 WR7          11 10101 1100032111120
        RReal3  WImag7  0001*RC4 84  WR0 RC3 *RR4 WC7 WR7     10 01010 1100042111130
        RReal4  WReal0  0011*RR6 85  WC0 WR1 *RC4 RR5 WC7     11 10101 0100052011140 IMAG DATA SNAPSHOT
        RReal5  WReal1  0000*RC6 86  WR2 WC1 *RR6 RC5         10 11010 1100062111150
        RReal6  WReal2  0010*RR0 87  WC2 WR3 *RC6 RR7         11 10101 1100071111160
        RReal7  WReal3  0000*RC0 88 *RR0 WC3 WR4 RC7          01 11010 1000001111170
        RImag0  WReal4  0010*RR2 89 *RC0 RR1 WC4 WR5          11 10101 1100011101000
        RImag1  WReal5  0001*RC2 8A *RR2 RC1 WR6 WC5          01 11010 1100021110110
        RImag2  WReal6  0011*RR4 8B *RC2 RR3 WC6 WR7          11 10101 1100032111120
        RImag3  WReal7  0001*RC4 8C  WR0 RC3 *RR4 WC7 WR7     10 01010 1100042111130
        RImag4  WImag0  0011*RR6 8D  WC0 WR1 *RC4 RR5 WC7     11 10101 0100052011141 REAL DATA SNAPSHOT
        RImag5  WImag1  0000*RC6 8E  WR2 WC1 *RR6 RC5         10 11010 1100062111150
        RImag6  WImag2  0010*RR0 8F  WC2 WR3 *RC6 RR7         11 10101 1100071111160
        RImag7  WImag3  0000*RC0 90 *RR0 WC3 WR4 RC7          01 11010 1000001111170
        RReal0  WImag4  0010*RR2 91 *RC0 RR1 WC4 WR5          11 10101 1100011101000
        RReal1  WImag5  0001*RC2 92 *RR2 RC1 WR6 WC5          01 11010 1100021110110
        RReal2  WImag6  0011*RR4 93 *RC2 RR3 WC6 WR7          11 10101 1100032111120
        RReal3  WImag7  0001*RC4 94  WR0 RC3 *RR4 WC7 WR7     10 01010 1100042111130
        RReal4  WReal0  0011*RR6 95  WC0 WR1 *RC4 RR5 WC7     11 10101 0100052011140 IMAG DATA SNAPSHOT
        RReal5  WReal1  0000*RC6 96  WR2 WC1 *RR6 RC5         10 11010 1100062111150
        RReal6  WReal2  0010*RR0 97  WC2 WR3 *RC6 RR7         11 10101 1100071111160
        RReal7  WReal3  0000*RC0 98 *RR0 WC3 WR4 RC7          01 11010 1000001111170
        RImag0  WReal4  0010*RR2 99 *RC0 RR1 WC4 WR5          11 10101 1100011101000
        RImag1  WReal5  0001*RC2 9A *RR2 RC1 WR6 WC5          01 11010 1100021110110
        RImag2  WReal6  0011*RR4 9B *RC2 RR3 WC6 WR7          11 10101 1100032111120
        RImag3  WReal7  0001*RC4 9C  WR0 RC3 *RR4 WC7 WR7     10 01010 1100042111130
        RImag4  WImag0  0011*RR6 9D  WC0 WR1 *RC4 RR5 WC7     11 10101 0100052011141
        RImag5  WImag1  0000*RC6 9E  WR2 WC1 *RR6 RC5         10 11010 1100062111150
        RImag6  WImag2  0010*RR0 9F  WC2 WR3 *RC6 RR7         11 10101 1100071111160
        RImag7  WImag3  0000*RC0 A0 *RR0 WC3 WR4 RC7          01 11010 1000001111170
        RReal0  WImag4  0010*RR2 A1 *RC0 RR1 WC4 WR5          11 10101 1100011101000
        RReal1  WImag5  0001*RC2 A2 *RR2 RC1 WR6 WC5          01 11010 1100021110110
        RReal2  WImag6  0011*RR4 A3 *RC2 RR3 WC6 WR7          11 10101 1100032111120
        RReal3  WImag7  0001*RC4 A4  WR0 RC3 *RR4 WC7 WR7     10 01010 1100042111130
        RReal4  WReal0  0011*RR6 A5  WC0 WR1 *RC4 RR5 WC7     11 10101 0100052011140
        RReal5  WReal1  0000*RC6 A6  WR2 WC1 *RR6 RC5         10 11010 1100062111150
        RReal6  WReal2  0010*RR0 A7  WC2 WR3 *RC6 RR7         11 10101 1100071111160
        RReal7  WReal3  0000*RC0 A8 *RR0 WC3 WR4 RC7          01 11010 1000001111170
        RImag0  WReal4  0010*RR2 A9 *RC0 RR1 WC4 WR5          11 10101 1100011101000
        RImag1  WReal5  0001*RC2 AA *RR2 RC1 WR6 WC5          01 11010 1100021110110
        RImag2  WReal6  0011*RR4 AB *RC2 RR3 WC6 WR7          11 10101 1100032111120DRAMBL(DERIVED FROM RESCNT WHEN RESULT COUNT = 4)
        RImag3  WReal7  0001*RC4 AC  WR0 RC3 *RR4 WC7 WR7     10 01010 11010421111300DRAMBLRD
        RImag4  WImag0  0011*RR6 AD  WC0 WR1 *RC4 RR5 WC7     11 10101 010105201114100              ALSO SEE L031D32
        RImag5  WImag1  0020*RC6 AE  WR2 WC1 *RR6 RC5         10 11010 110106211115010LAST USE OF OLD BASELINE IF RESULT 4
        RImag6  WImag2  0160*be0 AF  WC2 WR3 *RC6 RR7         11 10101 110107111116001BASELINE HIZ IF RESULT 4
        RImag7  WImag3  0020*be0 B0      WC3 WR4 RC7          01 11011 100110111117000NEW BASELINE IF RESULT 4
                WImag4  1160*be1 B1          WC4 WR5          11 10111 11011011X1X00sequpbr\(14)
                WImag5  1020*be1 B2          WR6 WC5          01 11011 11011011X1X0011loop to 66 VIA PCLI
                WImag6  1160*be2 B3          WC6 WR7          11 10111 11011031X1X0000    IF NOT STOPLOOP
                WImag7  1020*be2 B4              WC7 WR7      11 01111 11011031X1X0011
                        0160*be3 B5                  WC7      11 11111 0101103XX1X0011
                        0020*be3 B6 *be3 be2 be1 be0 be0      11 01111 1111103XX1X0011
                        0160*be4 B7 *be3 be3 be1 be1 be0      11 11111 1101103XX1X0011     IF STOPLOOP CONTINUE
                        0020*be4 B8 *be4 be3 be2 be1 be1      11 01111 1111103XX1X00 pcld\(13)
                        0160*be5 B9 *be4 be4 be2 be2 be1      11 11111 1101103XX1X00
                        0020*be5 BA *be5 be4 be3 be2 be2      11 01111 1111103XX1X00
                        0160*be6 BB *be5 be5 be3 be3 be2      11 11111 1101103XX1X00
                        0070*be6 BC *be6 be5 be4 be3 be3      11 01111 1111103XX1X00
                        0070*RFR BD *be6 be6 be4 be4 be3      11 11111 1101103XX1X000
                        0020*RFR BE *RFR be6 be5 be4 be4      11 01111 1111103XX1X000
                        0060*be0 BF *RFR RFR be5 be5 be4      11 11111 1101101XX1X000
                        0020*be0 C0      RFR be6 be6 be5      11 01111 1111101XX1X001    FOR PAGE 1 - THE MAIN LOOP, WE IDLE IN C0-C15
                        1060*be1 C1          be6 be6 be5      11 11111 1101101XX1X001    THIS GIVES A CONTINUOUS BACKEND CLOCK AND REFRESH.
                        1020*be1 C2          RFR RFR be6      11 01111 1111101XX1X001    THUS IF A TIC WITH A SMALL AMOUNT OF DATA FOLLOWS
                        1060*be2 C3          RFR RFR be6      11 11111 1101103XX1X001    A TIC WITH A LARGE AMOUNT OF DATA,
                        1020*be2 C4                  RFR      11 11111 1101103XX1X001    THE BACKEND WILL STILL BE ABLE TO MOVE ALL THE DATA.
                        0060*be3 C5                  RFR      11 11111 1100103XX1X001
                        0020*be3 C6 *be3 be2 be1 be0 be0      11 01111 1100103XX1X001
                        0060*be4 C7 *be3 be3 be1 be1 be0      11 11111 1100103XX1X001
                        0020*be4 C8 *be4 be3 be2 be1 be1      11 01111 1100103XX1X001incrfrsh(60)
                        0060*be5 C9 *be4 be4 be2 be2 be1      11 11111 1100103XX1X0011
                        0020*be5 CA *be5 be4 be3 be2 be2      11 01111 1100103XX1X001
                        0060*be6 CB *be5 be5 be3 be3 be2      11 11111 1100103XX1X001
                        0070*be6 CC *be6 be5 be4 be3 be3      11 01111 1101103XX1X001
                        0070*RFR CD *be6 be6 be4 be4 be3      11 11111 1101103XX1X001
                        0020*RFR CE *RFR be6 be5 be4 be4      11 01111 1101103XX1X001
                        0160*be0 CF *RFR RFR be5 be5 be4      11 11111 1101101XX1X001
                        0020*be0 D0      RFR be6 be6 be5      11 01111 1101101XX1X001
                        1160*be1 D1          be6 be6 be5      11 11111 1101101XX1X001
                        1020*be1 D2          RFR RFR be6      11 01111 1101101XX1X001
                        1160*be2 D3          RFR RFR be6      11 11111 1101103XX1X001
                        1020*be2 D4                  RFR      11 11111 1101103XX1X001
                        0160*be3 D5                  RFR      11 11111 1101103XX1X001
                        0020*be3 D6 *be3 be2 be1 be0 be0      11 01111 1111103XX1X001
                        0160*be4 D7 *be3 be3 be1 be1 be0      11 11111 1101103XX1X001
                        0020*be4 D8 *be4 be3 be2 be1 be1      11 01111 1111103XX1X001incrfrsh(60)
                        0160*be5 D9 *be4 be4 be2 be2 be1      11 11111 1101103XX1X0011
                        0020*be5 DA *be5 be4 be3 be2 be2      11 01111 1111103XX1X001
                        0160*be6 DB *be5 be5 be3 be3 be2      11 11111 1101103XX1X001
                        0070*be6 DC *be6 be5 be4 be3 be3      11 01111 1111103XX1X001
                        0070*RFR DD *be6 be6 be4 be4 be3      11 11111 1101103XX1X001
                        0020*RFR DE *RFR be6 be5 be4 be4      11 01111 1111103XX1X001
                        0060*be0 DF *RFR RFR be5 be5 be4      11 11111 1101101XX1 001
                        vadroe(65)                                               CLACP\
                         rcntenbl(69)          DRAM BANK          precas\            uPINT\0(21)
                          preasel(8-10)     MEMORY ADDRESS        85410SNAPOE\(WE\8)
                           deltoa(15)       ACCESSES           we\   EESNAPOE(from CLAC ram when TW=7)
                            8TO1 PROM  0   1     4     5     8 40     dlyrc(71)
                            MUX  ADDR  2   3     6     7     9         10ustic(70)
                                                                        clacenbl\(3)
                                                                         tw(0-2)
                                                                          prebaenbl\(11-12)
                                                                           SNAPCE\ FOR SNAP OF 0
                                                                            EESNAPCE\(from CLAC ram for snap of 0)
                                                                             CLAC\(from CLAC ram to clac 0) CLAC is one later since the MAC instruction has one less pipeline
                                                                              TW(0-2)                        in the T register path.
                                                                               rescnt(57)
```

```
 vadroe(65)                                                   uPINT\0(21)
  rcntenbl(69)          DRAM BANK          precas\
   preasel(8-10)     MEMORY ADDRESS        85410SNAPOE\(WE\8)
    deltoa(15)       ACCESSES           we\     EESNAPOE(from CLAC ram when TW=7)
     8TO1 PROM  0   1     4     5     8 40       dlyrc(71)
     MUX  ADDR  2   3     6     7     9           10ustic(70)
                                                   clacenbl\(3)
                                                    tw(0-2)
                                                     prebaenbl\(11-12)
                                                      SNAPCE\ FOR SNAP OF 0
                                                       EESNAPCE\(from CLAC ram for snap of 0)
                                                        CLAC\(from CLAC ram to clac 0)
                                                         TW(0-2)
                                                          rescnt(57)
 0000*RC0 C0 *RR0 RFR be6 be5 be5 1101110 1111001XXX0011
 0010*RR2 C1 *RC0 RR1 be6 be6 be5 1111101 1101011X0X0011
 0001*RC2 C2 *RR2 RC1 RFR be6 be6 1101110 1111021X101011
 0011*RR4 C3 *RC2 RR3 RFR RFR be6 1111101 1101032X112011
 0001*RC4 C4  WR0 RC3 *RR4 RFR RFR 1111010 1101042X113001
 0011*RR6 C5  WC0 WR1 *RC4 RR5 RFR 1110101 11010520114011
 0000*RC6 C6  WR2 WC1 *RR6 RC5     1111010 11010621115011  \ TO IDLE LOOP VIA PCLI
```

SECTION AS ON PAGE 2 FOR VALIDITY FILTERING
WE DO NOT WANT THE VALIDITY IDLE LOOP TO CLOCK THE BACKEND,
SINCE IT WILL BE IMMEDIATELY FOLLOWED BY THE MAIN LOOP.

% MEANS A CHANGED VALUE

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: DRAM ADDRESSING		
Size: C	Document Number: 56000L031 (L031D14.SCH)	REV
Date: May 14, 1993	Sheet 14 of	

SUBARRAY 0 IS A 32 TAP FILTER * MEANS READY TO OUTPUT
SUBARRAY 1 IS A 10 TAP FILTER, ONLY 5 RAMS USED

SUBARRAY 0	SUBARRAY 1	RAM0	RAM1	RAM2	RAM3	RAM4	RAM5	RAM6	RAM7
INPUT 0	INPUT0								
INPUT 1		SUB1IN0	1T0						
INPUT 2		SUB0IN0	T0						
INPUT 3		SUB0IN1	T1						
INPUT 4	INPUT1	SUB0IN2	T2						
INPUT 5		SUB0IN3	T3						
INPUT 6		SUB1IN1	1T1						
INPUT 7		SUB0IN4	T4	T0					
INPUT 8	INPUT2	SUB0IN5	T5	T1					
INPUT 9		SUB0IN6	T6	T2					
INPUT 10		SUB0IN7	T7	T3					
INPUT 11		SUB1IN2	1T2	1T0					
INPUT 12	INPUT3	SUB0IN8	T8	T4	T0				
INPUT 13		SUB0IN9	T9	T5	T1				
INPUT 14		SUB0IN10	T10	T6	T2				
INPUT 15		SUB0IN11	T11	T7	T3				
INPUT 16	INPUT4	SUB1IN3	1T3	1T1					
INPUT 17		SUB0IN12	T12	T8	T4	T0			
INPUT 18		SUB0IN13	T13	T9	T5	T1			
INPUT 19		SUB0IN14	T14	T10	T6	T2			
INPUT 20	INPUT5	SUB0IN15	T15	T11	T7	T3			
INPUT 21		SUB1IN4	1T4	1T2	1T0				
INPUT 22		SUB0IN16	T16	T12	T8	T4	T0		
INPUT 23		SUB0IN17	T17	T13	T9	T5	T1		
INPUT 24	INPUT6	SUB0IN18	T18	T14	T10	T6	T2		
INPUT 25		SUB0IN19	T19	T15	T11	T7	T3		
INPUT 26		SUB1IN5	1T5	1T3	1T1				
INPUT 27		SUB0IN20	T20	T16	T12	T8	T4	T0	
INPUT 28	INPUT7	SUB0IN21	T21	T17	T13	T9	T5	T1	
INPUT 29		SUB0IN22	T22	T18	T14	T10	T6	T2	
INPUT 30		SUB0IN23	T23	T19	T15	T11	T7	T3	
INPUT 31		SUB1IN6	1T6	1T4	1T2	1T0			
INPUT 32	INPUT8	SUB0IN24	T24	T20	T16	T12	T8	T4	T0
INPUT 33		SUB0IN25	T25	T21	T17	T13	T9	T5	T1
INPUT 34		SUB0IN26	T26	T22	T18	T14	T10	T6	T2
INPUT 35		SUB0IN27	T27	T23	T19	T15	T11	T7	T3
INPUT 36	INPUT9	SUB1IN7	1T7	1T5	1T3	1T1			
INPUT 37		SUB0IN28	T28	T24	T20	T16	T12	T8	T4 T0
INPUT 38		SUB0IN29	T29	T25	T21	T17	T13	T9	T5 T1
INPUT 39		SUB0IN30	T30	T26	T22	T18	T14	T10	T6 T2
INPUT 40	INPUT10	SUB0IN31	*T31	T27	T23	T19	T15	T11	T7 T3
INPUT 41		SUB1IN8	1T8	1T6	1T4	1T2	1T0		
INPUT 42		SUB0IN32	T0	T28	T24	T20	T16	T12	T8 T4
INPUT 43		SUB0IN33	T1	T29	T25	T21	T17	T13	T9 T5
	INPUT11	SUB0IN34	T2	T30	T26	T22	T18	T14	T10 T6
		SUB0IN35	T3	*T31	T27	T23	T19	T15	T11 T7
		SUB1IN9	*1T9	1T7	1T5	1T3	1T1		
		SUB0IN36	T4	T0	T28	T24	T20	T16	T12 T8
		SUB0IN37	T5	T1	T29	T25	T21	T17	T13 T9
		SUB0IN38	T6	T2	T30	T26	T22	T18	T14 T10
		SUB0IN39	T7	T3	*T31	T27	T23	T19	T15 T11
		SUB1IN10	1T0	1T8	1T6	1T4	1T2		
		SUB0IN40	T8	T4	T0	T28	T24	T20	T16 T12
		SUB0IN41	T9	T5	T1	T29	T25	T21	T17 T13
		SUB0IN42	T10	T6	T2	T30	T26	T22	T18 T14
		SUB0IN43	T11	T7	T3	*T31	T27	T23	T19 T15
		SUB1IN11	1T1	*1T9	1T7	1T5	1T3		
				T8	T4	T0	T28	T24	T20 T16
				T9	T5	T1	T29	T25	T21 T17
				T10	T6	T2	T30	T26	T22 T18
				T11	T7	T3	*T31	T27	T23 T19
				1T0	1T8	1T6	1T4		
					T8	T4	T0	T28	T24 T20
					T9	T5	T1	T29	T25 T21
					T10	T6	T2	T30	T26 T22
					T11	T7	T3	*T31	T27 T23
				1T1	*1T9	1T7	1T5		
						T8	T4	T0	T28 T24
						T9	T5	T1	T29 T25
						T10	T6	T2	T30 T26
						T11	T7	T3	*T31 T27
					1T0	1T8	1T6		
						T8	T4	T0	T28 T24
						T9	T5	T1	T29 T25
						T10	T6	T2	T30 T26
						T11	T7	T3	*T31 T27
					1T1	*1T9	1T7		
							T8	T4	T0 T28
							T9	T5	T1 T29
							T10	T6	T2 T30
							T11	T7	T3 *T31
						1T0	1T8		
								T8	T4 T0
								T9	T5 T1
								T10	T6 T2
								T11	T7 T3
						1T1	*1T9		
									T8 T4
									T9 T5
									T10 T6
									T11 T7
									T8
									T9
									T10
									T11

A BASELINE = 8 CHANNELS * 256 SPECTRAL POINTS * 8 BYTES = 16384 BYTES.
IN 131 MS., AT 4 MBYES/SEC, 32 BASELINES CAN BE OUTPUT.

EXAMPLE:
SUBARRAY 0 25 BASELINES EVERY 131 MS USING FILTER

SUBARRAY 1 70 BASELINES EVERY 1.31 SEC

DO 25 OF 0 AND 7 OF 1, EACH CYCLE
SUBARRAY 0 VALUES GO THROUGH FILTER, EVENTUALLY GETTING TO OUTPUT RAM.
SUBARRAY 1 VALUES GO DIRECTLY TO OUTPUT RAM.

OUTPUT RAM HOLDS ALL 210 BASELINES

SUBARRAY 0'S PORTION UPDATED EVERY 131 MS.
SUBARRAY 1'S PORTION UPDATED EVERY 1.31 SEC

NEED TO BANKSWITCH ON A SUBARRAY BASIS!

CHUCK CAN ONLY GIVE OUT VALUES ON THE 2 uSEC BOUNDARIES. THEREFORE IT IT GOOD TO BUFFER HIM VIA AN EXTRA MEMORY.

FOR DIFFERENT DUMP RATES,
FOR THE DIFFERENT SUBARRAYS,
JUST INTERSPERSE THE POINTS
AT WHATEVER RATE THEY COME OUT.

IF ONE SUBARRAY IS HUGE, WITH A LOW DUMP RATE, WHILE THE OTHER IS SMALL WITH A FAST DUMP RATE, THE SMALL ONE HAS PRIORITY. THUS THE HUGE ONE WILL HAVE TO COME IN SECTIONS BETWEEN THE SMALL ONE.

SUBARRAYS ALLOWED IN STORING DATA IN 8 RAMS.
IF 32 TAP FILTERS, WANT TO OUTPUT EACH AFTER 32 DUMPS.
IF X TAP FILTERS, WANT TO OUTPUT EACH AFTER X DUMPS.
WHEN IT IS TIME TO OUTPUT, A SUBARRAY, HAVE THAT DUMP BE COPIED IN PARALLEL TO THE OUTPUT RAM. THE OUTPUT RAM WILL THEN BE READ TO THE BACKEND.

RAMS USED * DUTY CYCLE = # TAP WEIGHTS
WHERE RAMS USED CAN BE 1 TO 8
DUTY CYCLE IS AN INTEGER VALUE
THUS # TAP WEIGHTS CAN BE:

DUTY CYCLE \ RAMS USED	0	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0
1	0	1	2	3	4	5	6	7	8
2	0	2	4	6	8	10	12	14	16
3	0	3	6	9	12	15	18	21	24
4	0	4	8	12	16	20	24	28	32
5	0	5	10	15	20	25	30	35	40
6	0	6	12	18	24	30	36	42	48
7	0	7	14	21	28	35	42	49	56
8	0	8	16	24	32	40	48	56	64

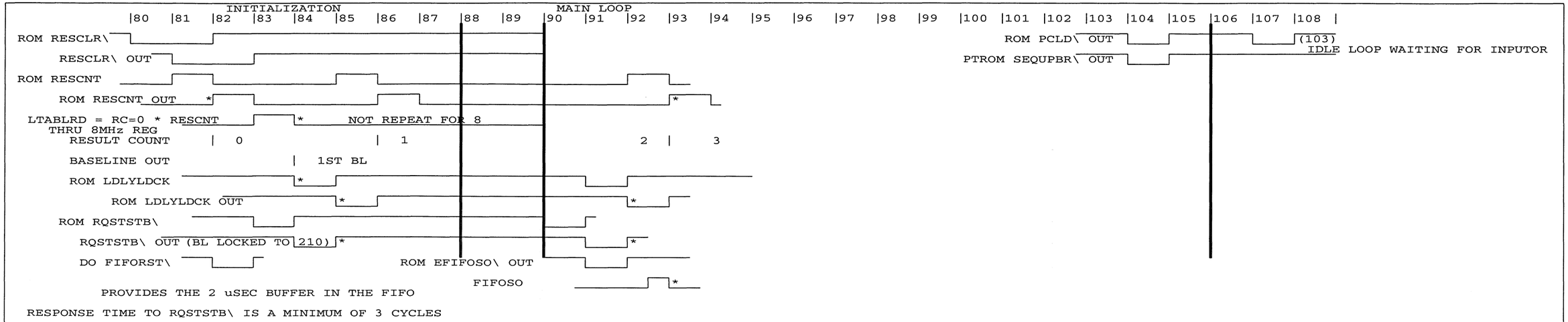
DUTY CYCLE

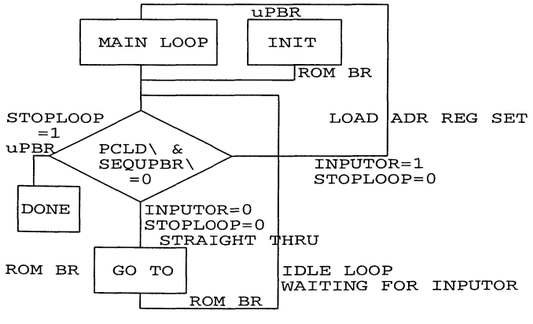
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: FIR SUBARRAY TIMING

Size	Document Number	REV
B	56000L031 (L031D23.SCH)	

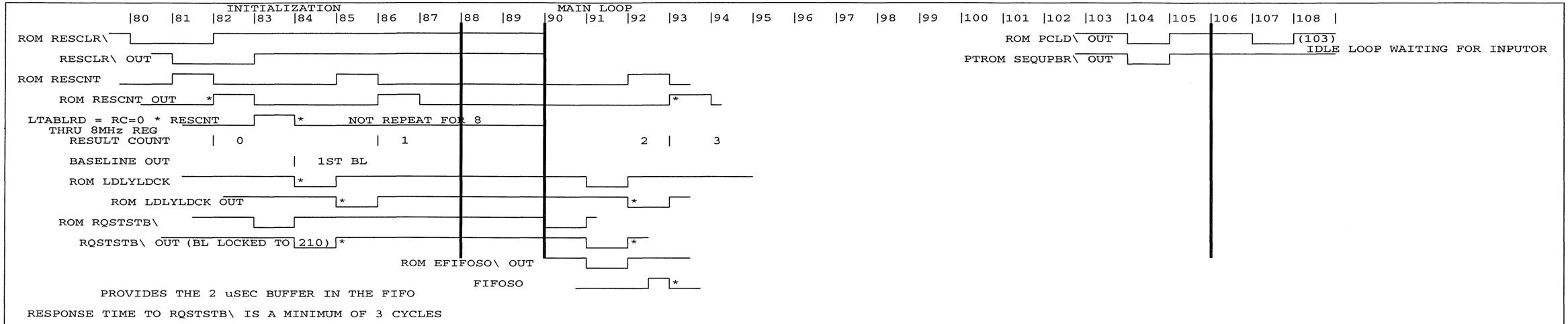
Date: July 25, 1996 Sheet 23 of 41





STOPLOOP FROM LTABL FIFO

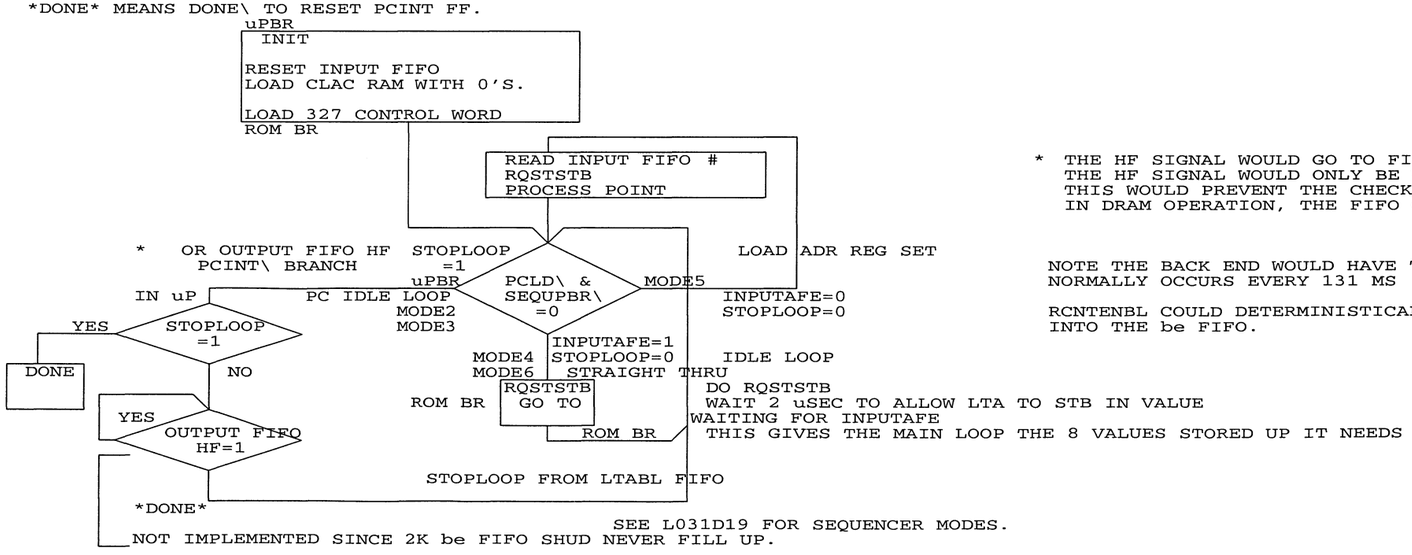
VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: VALIDITY LOOP TIMING		
Size: B	Document Number: 56000L031 (L031D26.SCH)	REV:
Date: July 3, 1991	Sheet 26 of	



DOES NOT USE DRAMS

INPUT AFE = 0 WHEN > 8 VALUES IN FIFO

DONE MEANS DONE\ TO RESET PCINT FF.



* THE HF SIGNAL WOULD GO TO FIRPAL7. FIRPAL7 ALSO HAS THE PAGE #.
THE HF SIGNAL WOULD ONLY BE USED ON PAGE 1, WHICH WOULD HAVE THE STRAIGHT THRU MODE.
THIS WOULD PREVENT THE CHECKING OF HF DURING DRAM USE OPERATION.
IN DRAM OPERATION, THE FIFO COULD NORMALLY BECOME FULL IN 2 K MODE.

NOTE THE BACK END WOULD HAVE TO NOT EXPECT THE BANK SWITCHING THAT NORMALLY OCCURS EVERY 131 MS

RCNTENBL COULD DETERMINISTICALLY CLOCK THE SNAPSHOT REGISTER OUTPUT INTO THE be FIFO.

IN INIT, PRIME INPUT FIFO WITH ONE DUMMY POINT.
THIS MAKES AFE TOGGLE AFTER 8 POINTS.
RCNTENBL AFTER A DELAY CAUSES beDINCLK TO STOBE THE DATA INTO THE be FIFO.

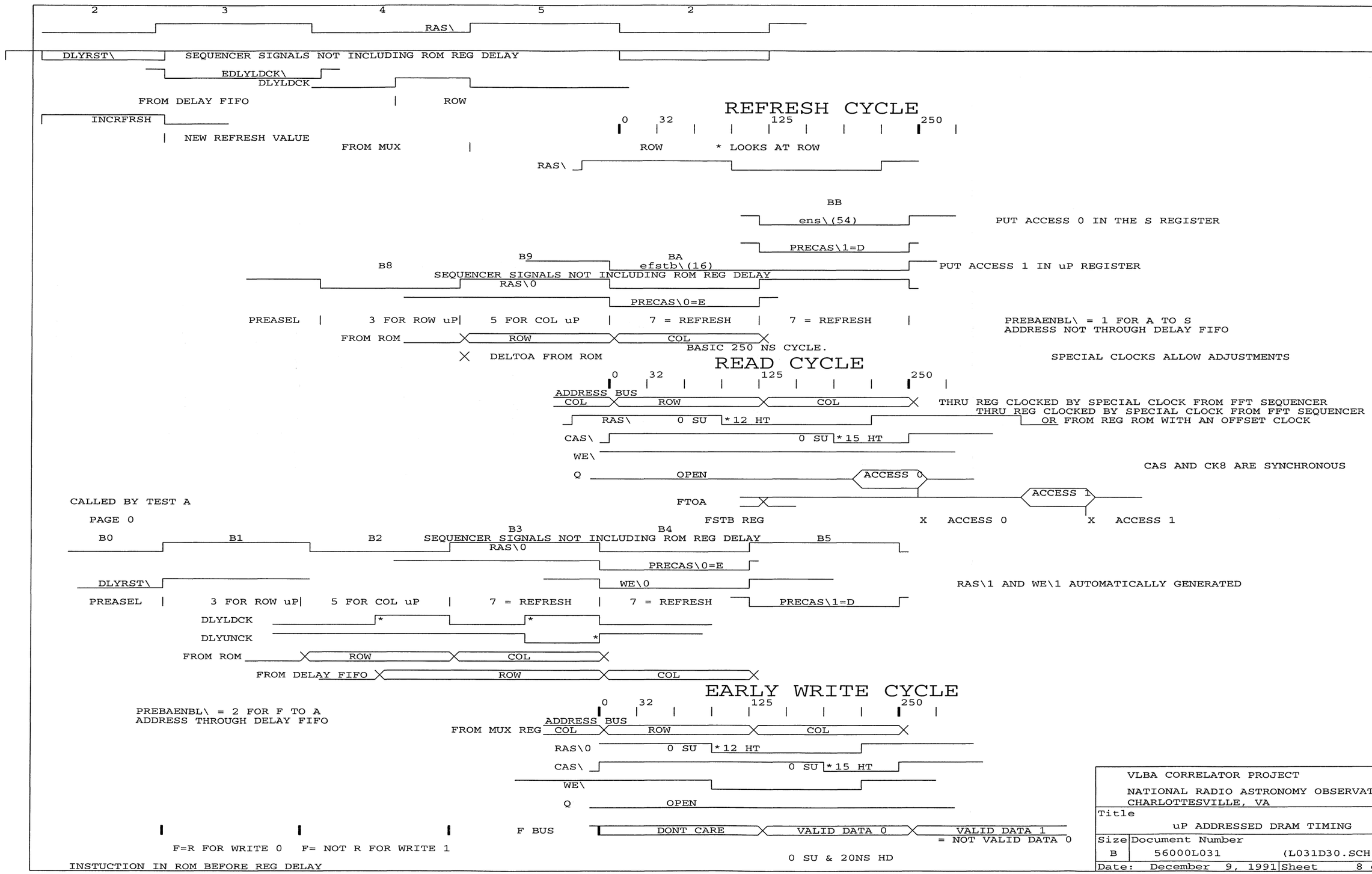
VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
MAIN LOOP TIMING

Size	Document Number	REV
B	56000L031 (L031D27.SCH)	

Date: October 23, 1991 Sheet 27 of



VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title

uP ADDRESSED DRAM TIMING

Size	Document Number	REV
B	56000L031 (L031D30.SCH)	

Date: December 9, 1991 | Sheet 8 of

lower case means actual value in prom before reg
nc = not clocked in 327

	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F	80	81	82	
instruction	f=r	r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r1+s	r*r1+s	r*r1+s	r*r1+s	r*r1+s	r*r1+s	r*r1+s	r*r1+s	r*r2+s	r*r2+s	r*r2+s	r*r2+s
R INPUT	HiZ	HiZ	TW0	TW1	TW2	TW3	TW4	TW5	TW6	TW7	TW0	TW1	TW2	TW3	TW4	TW5	TW6	TW7	TW0	TW1	
S-INPUT	XX	XX	XX	ACCr0	ACCr1	ACCr2	ACCr3	ACCr4	ACCr5	ACCr6	ACCr7	ACCi0	ACCi1	ACCi2	ACCi3	ACCi4	ACCi5	ACCi6	ACCi7	ACCr0	ACCr1

1 LESS PIPELINE STAGE IN 327

fstb\(16) — X

oemuxg\-ba | 1-2 | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram |

8TO1 MUX OUT (SEE 08) | RESULT 0 REAL | RESULT 0 IMAGINARY | RESULT 1 REAL

rqststb\(66) — *

rescnt(57) — res4 | MUST BE AFTER rqststb\ AND ldlyldck(75) | * | res5 | PLACEMENT BASED ON DRMBL (SEE SHT. 8)

ldlyldck(75) — * | LTABLRD | IF RESULT 0 — * | *

tw(0-2) | tw0 | tw1 | tw2 | tw3 | tw4 | tw5 | tw6 | tw7 | tw0 | tw1 | tw2 | tw3 | tw4 | tw5 | tw6 | tw7 | tw0 | tw1 | tw2 |

subaunck(4) — * | ---NEXT SUBARRAY

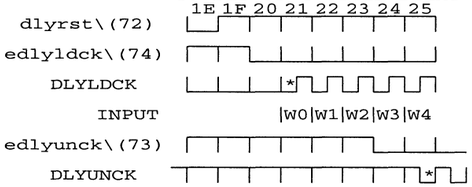
ldlyunck(76) — * | 1ST ONE FOR DELAYED RESULT TO DRAMS SEE 08

INITIALLY:
LOAD A BASELINE, DRAM BASELINE, MODULUS AND SUBARRAY
LOAD VALIDITY RAMS

efifoso\(68)=1
vadroe(65)=0
edlyunck\(73)=0
edlyldck\(74)=0
dlyrst\(72)=1

START BY CALLING NEWPAGE FOR PAGE 1
STARTS AT 0. HAVE LOOPS ALWAYS IN 2uSEC INCREMENTS.
IDLE LOOP WHEN DONE, AT END OF TIC'S WORK.

TO SET UP 4 CYCLE DELAY



2 uSEC CYCLES NO DRAM WRITES

	20	30	40	50	60	70	80	90	A0	B0
ENTER HERE 1E	PRE0	PRE1	PRE2	PRE3	INIT	0	1	2	3	
evalunck\(62)					RRRR					
rqststb\(66)	RQ	RQ	RQ	RQ	(at 6) RQ	RQ	RQ	RQ		
ldlyldck(75)	W	W	W	W	W (at 0)	W	W	W		
subaunck(4)	GETS A DELAY OF 4			W = A FIFO WRITE	R	R	R	R		
ldlyunck(76)	GETS A DELAY OF 4		res0	R = A FIFO READ	(at E) R	res1 R	res2 R	res3 R		

rescnt(57) 01	res0 C	res1 C	res2 C	res3 C	res4*	(at D) C	res5 C	res6 C	res7 C	res8

4 BEHIND RESCNT

RESET THE RESULT COUNTER
resclr\(56) 00

res8	...	res0	res1	res2	res3	res4*

at end of baseline res1023 res0 causes STOPLOOP to be read from MOD FIFO.
STOPLOOP is pipelined (see L031D19) for an extra pass
res0 res1 res2 res3 res4* to C0 then idle loop.

adrfrst\(79) 01 RESET THE DELAY FIFO'S
fiforst\(67) 01 RESET THE INPUT FIFO

Note when doing validities, there was no DRAMBL at the STOPLOOP, since only 1680 of the 2048 baseline was completed.

* DRAMBL UNLOADS THE NEW DRAM BASELINE WHEN RESULT 4 FROM RESCNT.(SEE FIRPAL1 6E ON SHT. 1)
RESCNT IS PLACED SO AS NOT TO ALLOW THE NEW BASELINE LOADING UNTIL THE USE OF THE OLD BASELINE IS DONE.(SEE SHT.8)

6E S IN STRAIGHT THRU

FILTER 32 RESULTS

70	T0	ACCr0	T0*R0+0
71	T28	ACCr1	T28*R0+ACCr1
72	T24	ACCr2	T24*R0+ACCr2
73	T20	ACCr3	T20*R0+ACCr3
74	T16	ACCr4	T16*R0+ACCr4
75	T12	ACCr5	T12*R0+ACCr5
76	T8	ACCr6	T8*R0+ACCr6
77	T4	ACCr7	T4*R0+ACCr7
78	T0	ACCi0	T0*R1+0
79	T28	ACCi1	T28*R1+ACCi1
7A	T24	ACCi2	T24*R1+ACCi2
7B	T20	ACCi3	T20*R1+ACCi3
7C	T16	ACCi4	T16*R1+ACCi4
7D	T12	ACCi5	T12*R1+ACCi5
7E	T8	ACCi6	T8*R1+ACCi6
7F	T4	ACCi7	T4*R1+ACCi7

6B R6=RE3*VAL3
6C R7=IM3*VAL3
OUTPUT =
6D R IN
6E S IN

70	T0*R0+0
71	T28*R0+ACCr1
72	T24*R0+ACCr2
73	T20*R0+ACCr3
74	T16*R0+ACCr4
75	T12*R0+ACCr5
76	T8*R0+ACCr6
77	T4*R0+ACCr7
78	T0*R1+0
79	T28*R1+ACCi1
7A	T24*R1+ACCi2
7B	T20*R1+ACCi3
7C	T16*R1+ACCi4
7D	T12*R1+ACCi5
7E	T8*R1+ACCi6
7F	T4*R1+ACCi7

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

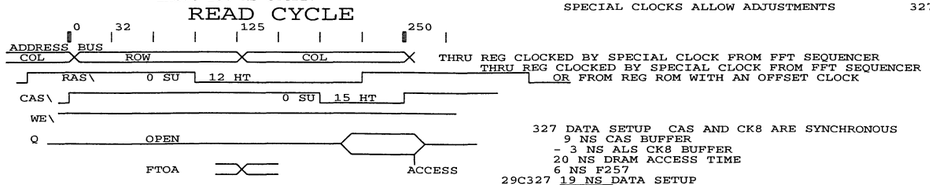
Title: MAIN LOOP MAC TIMING

Size	Document Number	REV
B	56000L031 (L031D32.SCH)	

Date: March 20, 1992 Sheet 12 of

BASIC 250 NS CYCLE.

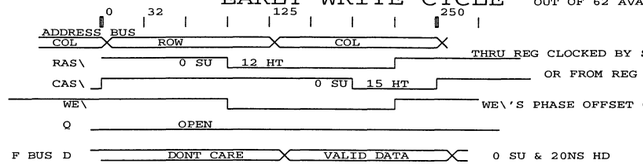
READ CYCLE



THRU REG CLOCKED BY SPECIAL CLOCK FROM FFT SEQUENCER
THRU REG CLOCKED BY SPECIAL CLOCK FROM FFT SEQUENCER
OR FROM REG ROM WITH AN OFFSET CLOCK

327 DATA SETUP CAS AND CK8 ARE SYNCHRONOUS
9 NS CAS BUFFER
- 3 NS ALS CK8 BUFFER
20 NS DRAM ACCESS TIME
6 NS F257
29C327 19 NS DATA SETUP
51 NS
OUT OF 62 AVAILABLE

EARLY WRITE CYCLE

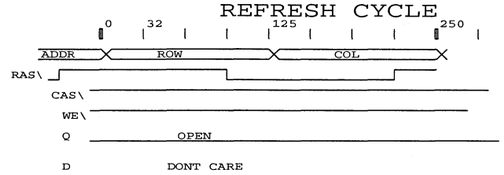


THRU REG CLOCKED BY SPECIAL CLOCK FROM FFT SEQUENCER
OR FROM REG ROM WITH AN OFFSET CLOCK

WE\'S PHASE OFFSET CAN BE TIED TO RAS\'S.

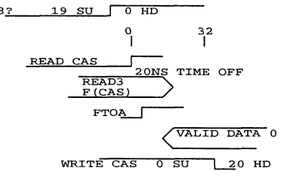
0 SU & 20NS HD

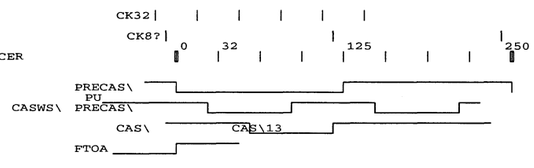
REFRESH CYCLE

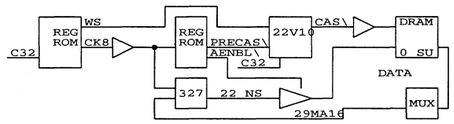


ADDRESS TIMING
245 12 NS
232 31 NS

SPECIAL CLOCKS ALLOW ADJUSTMENTS







CAS\ & CK8 ARE SYNCHRONOUS
(1 DELAY FROM CK32)

PRECAS\ TIMING
CK8 12NS
CK8 BUFFER 10 NS
PRECAS\ 12 NS
22V10 SU 12 NS
37 NS
62 AVAIL DUE TO WS

DATA TIMING
327 OUT 22NS
29MA16 25 NS
DRAM 0 SU
47 NS
62 AVAIL

AENBL\ & BENBL\ TO DATA PATH TIMING
-2 NS CAS BUFFER
10 NS ALS CK8 BUFFER
AENBL\ 12 NS
29MA16 25 NS
DRAM 0 SU
45 NS
62 AVAIL

FOR READING BUS, THERE IS 125 NS AVAILABLE AFTER FTOA.

MEETS SPECS EVEN THOUGH WE\ OFFSET

SEE L031D14

THE READ AND WRITES 0 THRU 7 CAN BE SEEN TO PROGRESS THROUGH THE 4 RAM BANKS.
A AND B REPRESENT THE 2 PHYSICAL SETS OF RAM, EACH WITH 2 RAM BANKS.
FTOA SWITCHES BETWEEN THE RAM BANKS.
SINCE FTOA ALWAYS ENABLES ONE BUS, A OR B, ITS INITIAL STATE DOES NOT MATTER, FOR AS FAR AS PREVENTING BUS CONTENTION.
IF THERE IS NO CLOCK, IT IS ASSUMED THAT THE DRAM OUTPUTS WILL BE HIZ.
REFRESH DRAMS DURING THE SETUP 2 USEC CYCLE IN THE 10 USEC LOOP.
THE 250 NS CYCLE ALLOWS FULL RANDOM ACCESS.

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: DRAM CYCLES

Size	Document Number	REV
C	56000L031 (L031D33.SCH)	
Date: November 19, 1991	Sheet 8 of	

lower case means actual value in prom before reg
nc = not clocked in 327

PAGE 2 ->| PAGE 1 ->|

do not multiply by validity here!

	AF	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75
instruction	r*r0+s	dummy	f=r												f=r			r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r0+s	
R INPUT	TW7															RE0	HiZ	HiZ	TW0	TW1	TW2	TW3	TW4
Rx REG																ACTUALLY IS 1		EARLY	R0=RE0				
rfsel(24-26)(number) & enrf\(27)(waveform)																	0						
oemuxg(103)\-ba(102,1)		1-3	1-0	1-0	1-0	1-0	1-0	1-0	1-0	1-0	1-0	1-0	1-0	1-0	0-0fifo	1-0	1-2	0-2 ram	0-2 ram	0-2 ram	0-2 ram	0-2 ram	0-2
efifoso\(68) #, FIFOSO(waveform)		1	1	1	1	1										1	1	0	1 *	1	1	1	1
vadroe(65)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
evalunck\(62)		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1						
													clacenbl\(3)										
tw(0-2)																		tw0	tw1	tw2	tw3	tw4	tw5
											SEE L031D10	div	sd(18)		SD0						gce(17)		
SUBARRAY FROM DELAY FIFO																							

ok to go ram to fifo

throw away imaginary value

60	DUMMY INSTRUCTION	FOLLOWING LAST MAC
61	VAL0	STRAIGHT THRU
62	VAL1	STRAIGHT THRU
63	VAL2	STRAIGHT THRU
64	VAL3	STRAIGHT THRU
65	RE0	STRAIGHT THRU
66	IM0	STRAIGHT THRU
67	RE1	STRAIGHT THRU
68	IM1	STRAIGHT THRU
69	RE2	STRAIGHT THRU
6A	IM2	STRAIGHT THRU
6B	RE3	STRAIGHT THRU
6C	IM3	STRAIGHT THRU
6D	R IN	STRAIGHT THRU
6E	S IN	STRAIGHT THRU

	FILTER 32 RESULTS		
70	T0	ACCr0	T0*R0+0
71	T28	ACCr1	T28*R0+ACCr1
72	T24	ACCr2	T24*R0+ACCr2
73	T20	ACCr3	T20*R0+ACCr3
74	T16	ACCr4	T16*R0+ACCr4
75	T12	ACCr5	T12*R0+ACCr5
76	T8	ACCr6	T8*R0+ACCr6
77	T4	ACCr7	T4*R0+ACCr7
78	T0	ACCi0	T0*R1+0
79	T28	ACCi1	T28*R1+ACCi1
7A	T24	ACCi2	T24*R1+ACCi2
7B	T20	ACCi3	T20*R1+ACCi3
7C	T16	ACCi4	T16*R1+ACCi4
7D	T12	ACCi5	T12*R1+ACCi5
7E	T8	ACCi6	T8*R1+ACCi6
7F	T4	ACCi7	T4*R1+ACCi7

BC	T15*R7+ACCi28	
BD	T11*R7+ACCi29	
BE	T7*R7+ACCi30	
BF	T3*R7+ACCi31	
61	R4=VAL0	
62		
63		
64		
65		
66		
67		
68		
69		
6A		
6B		
6C	OUTPUT =	
6D	RE0	
6E	S IN	
70	T0*R0+0	
71	T28*R0+ACCr1	
72	T24*R0+ACCr2	
73	T20*R0+ACCr3	
74	T16*R0+ACCr4	
75	T12*R0+ACCr5	
76	T8*R0+ACCr6	
77	T4*R0+ACCr7	
78	T0*R1+0	
79	T28*R1+ACCi1	
8A	T24*R1+ACCi2	
8B	T20*R1+ACCi3	
8C		
8D		
8E		
8F		

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title
VALIDITY LOOP INITIALIZATION TIMING

Size	Document Number	REV
B	56000L031 (L031D34.SCH)	

Date: February 3, 1992 | Sheet 12 of

lower case means actual value in prom before reg
nc = not clocked in 327

PUT VALIDITIES IN RAM BANKS 0,1,2,3 PUT 1/V IN RAM BANKS 4,5,6,7

	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F	80	81	82	83	84	85
instruction		r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r0+s	r*r0+s	1*r0+0	1*r+0	1*r0+0	1*r0+0	1*r+0	1*r0+0	1*r0+0	1*r0+0	r*r1+s	r*r1+s	r*r1+s	r*r1+s		
R INPUT	HiZ	HiZ	TW0	TW1	TW2	TW3	TW4	TW5	TW6	TW7	HiZ	1/1st val	HiZ	HiZ	2nd r val	HiZ	HiZ	HiZ	TW0	TW1			
S-INPUT	XX	XX	XX	ACCr0	ACCr1	ACCr2	ACCr3	ACCr4	ACCr5	ACCr6	ACCr7	ACCi0	ACCi1	ACCi2	ACCi3	ACCi4	ACCi5	ACCi6	ACCi7	ACCr0	ACCr1		

1 LESS PIPELINE STAGE IN 327

fstb\(16) — X

oemuxg\-ba: 1-2 | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 0-2 ram | 1-1 | 0-1div | 1-1 | 1-0 | 0-0fifo | 1-0 | 1-2 | 1-2 | 0-2 ram | 0-2 ram | 0-2 ram

1ST VAL 0 — R0=1st VALIDITY — rfsel(24-26) number & enrf(27) waveform — 1/1ST VAL 4 — 2ND VAL 1 — R1=2ND VALIDITY

efifoso\(68) #, FIFOSO(waveform): 1 | 0 | 1 | * | 1 | 1 | 1 | 0 | 1 | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | * | 1

1st imaginary validity — 2nd real validity — 2nd imaginary validity

8TO1 MUX OUT (SEE 08): RESULT 0 REAL | RESULT 0 IMAGINARY | RESULT 1 REAL

rqststb\(66)

rescnt(57): res4 — MUST BE AFTER rqststb\ AND ldlyldck(75) — res5 — PLACEMENT BASED ON DRMBL (SEE SHT. 8)

ldlyldck(75): *

tw(0-2): tw0 | tw1 | tw2 | tw3 | tw4 | tw5 | tw6 | tw7 | tw0 | tw0 | tw0 | tw0 | tw0 | tw0 | tw0 | tw7 | tw0 | tw1 | tw2

TW0 ALWAYS GIVES SNAPCE — tw7 for we\8 to output buffer

subaunck(4): *

gwe\(64)

---NEXT SUBARRAY

ldlyunck(76): * — 1ST ONE FOR DELAYED RESULT TO DRAMS SEE 08

SEE L031D10 — gce(17) — NOTE AT 2 NEXT ITERATION DUE TO LONGER PIPELINE FOR MAC — div sd(18) — SD0 — gce(17)

DIVIDE BUFFER REG CONTENTS — 1/1ST VALIDITY — 1/2ND

	0	0	0	0	0	vadroe(65) 0	0	0	1	1	1	0	0	0	0	0	0	0	0
	1	1	1	1	1	evalunck\(62) 1	1	1	1	1	1	1	1	0	1 *	1	1	1	1	1

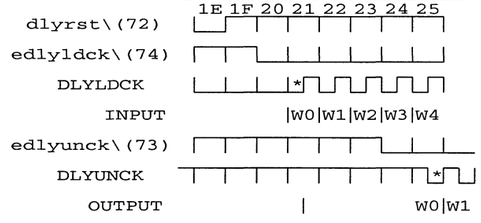
INITIALLY:
LOAD A BASELINE, DRAM BASELINE, MODULUS AND SUBARRAY
LOAD VALIDITY RAMS

efifoso\(68)=1
vadroe(65)=0
edlyunck\(73)=0
edlyldck\(74)=0
dlyrst\(72)=1

START BY CALLING NEWPAGE FOR PAGE 1
STARTS AT 0. HAVE LOOPS ALWAYS IN 2uSEC INCREMENTS.
IDLE LOOP WHEN DONE, AT END OF TIC'S WORK.

W = A FIFO WRITE
R = A FIFO READ

TO SET UP 4 CYCLE DELAY



6E	S IN	STRAIGHT THRU
	FILTER 32 RESULTS	
70	T0	ACCr0 T0*R0+0
71	T28	ACCr1 T28*R0+ACCr1
72	T24	ACCr2 T24*R0+ACCr2
73	T20	ACCr3 T20*R0+ACCr3
74	T16	ACCr4 T16*R0+ACCr4
75	T12	ACCr5 T12*R0+ACCr5
76	T8	ACCr6 T8*R0+ACCr6
77	T4	ACCr7 T4*R0+ACCr7

6B	R6=RE3*VAL3
6C	R7=IM3*VAL3
	OUTPUT =
6D	R IN
6E	S IN
70	T0*R0+0
71	T28*R0+ACCr1
72	T24*R0+ACCr2
73	T20*R0+ACCr3
74	
75	
76	
77	

2 uSEC CYCLES — NO DRAM WRITES

ENTER HERE	20 1E	30 PRE0	40 PRE1	50 PRE2	60 PRE3	70 INIT	80 0	90 1	A0 2	B0 3
evalunck\(62)							R	R	R	R
rqststb\(66)	RQ	RQ	RQ	RQ		(at 6) RQ	RQ	RQ	RQ	
ldlyldck(75)	W	W	W	W efifoso\(68)		W (at 0) R R	W R R	W R R	W R R	
subaunck(4)	GETS A DELAY OF 4						R	R	R	R
ldlyunck(76)	GETS A DELAY OF 4		res0				(at E) R	res1 R	res2 R	res3 R

4 BEHIND RESCNT

rescnt(57)	01	res0 C	res1 C	res2 C	res3 C	res4*	(at D) C	res5 C	res6 C	res7 C
RESET THE RESULT COUNTER						res8 ... res0		res9 res1	res10 res2	res11 res3
resclr\(56)	00									
adrfrst\(79)	01	RESET THE DELAY FIFO'S								
fiforst\(67)	01	RESET THE INPUT FIFO								

* DRAMBL UNLOADS THE NEW BASELINE WHEN RESULT 4 FROM RESCNT.(SEE FIRPAL1 6E ON SHT. 1)
RESCNT IS PLACED SO AS NOT TO ALLOW THE NEW BASELINE LOADING UNTIL THE USE OF THE OLD BASELINE IS DONE.(SEE SHT.8)

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: VALIDITY LOOP MAC TIMING

Size	Document Number	REV
B	56000L031 (L031D35.SCH)	

Date: February 6, 1992 | Sheet 12 of