Interoffice

VLBP Memo No. 14

National Radio Astronomy Observatory

Charlottesville, Virginia

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To: VLBP Project Group

From: R. P. Escoffier

Subject: Preliminary Design Thoughts on the VLBP Correlator

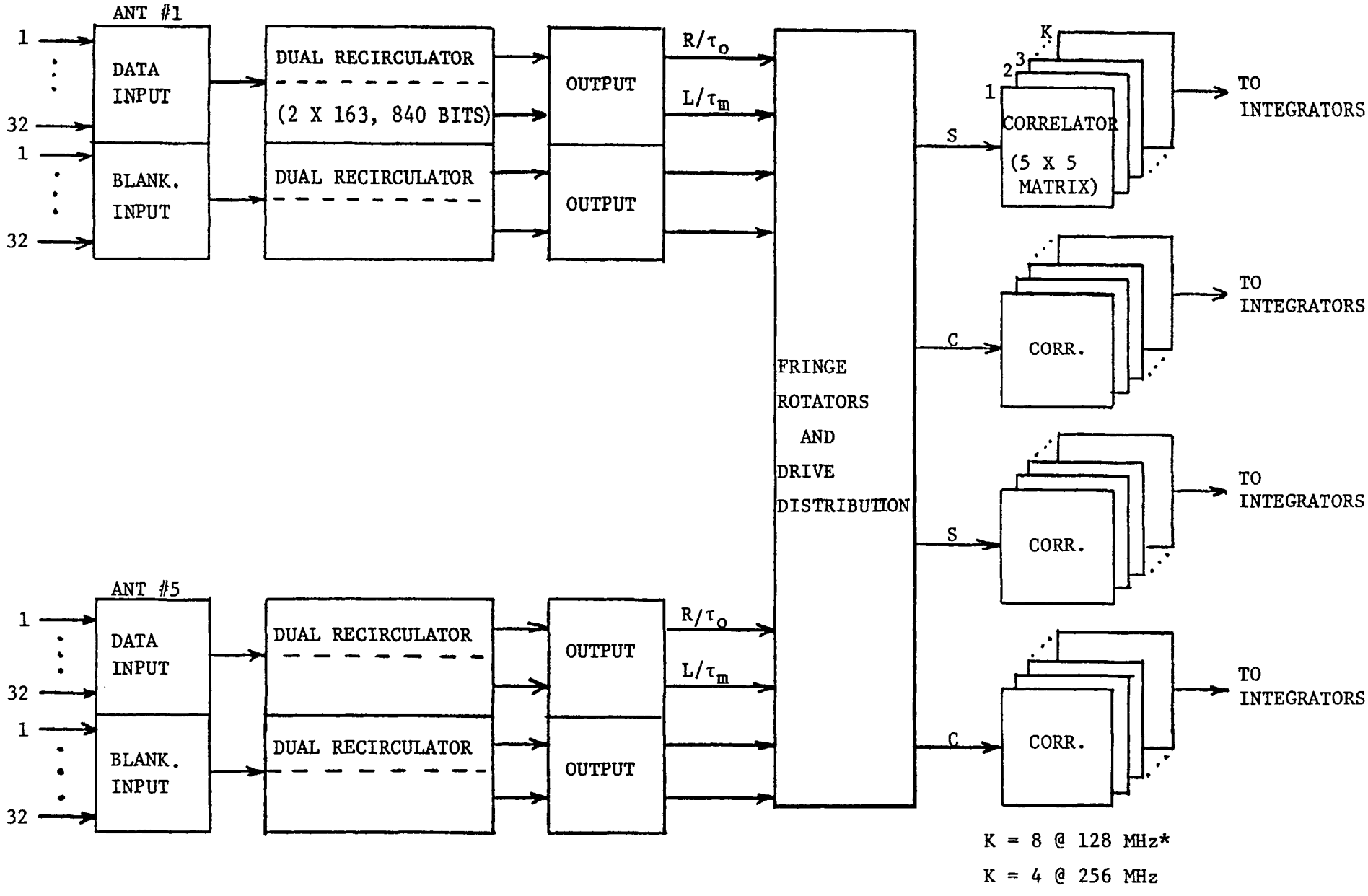
In order to better understand the various objectives of the VLBP project and to get a feeling for the relative difficulties of these objectives, I have devoted a couple of weeks to a conceptual design of a VLBI correlator. This design, presented in this memo will, I hope, serve as a starting point for the project and establish some minimum standards from which the project can proceed.

The design described is of a recirculating correlator in which digital astronomical data from relative low data rate parallel paths are stored in semiconductor RAM memory and extracted from this memory at higher data rates for correlation in high speed logic. The recirculation feature can save hardware by either allowing correlation of data multiple times thru the same hardware correlator circuits (MARK II) or by correlating data from many tape tracks consecutively thru a single correlator track (MARK III). This design does not consider such subjects as tape recorder control, delay lines, or post-correlation integration since these areas require more definition of the recording medium or correlator structure than is now convenient. A block diagram of the design is seen in Figure 1.

One objective of the proposed correlator is that it be able to process MARK III tapes. I have used this requirement to establish two features of the system seen in Figure 1. First, I took the 28 parallel MARK III data tracks, rounded this number up to a much nicer 32, and set this figure as the maximum number of parallel inputs per station. Second, I set 32 as a minimum recirculation factor (in continuum) meaning that the recirculation aspect of the design is used to eliminate the 28 wide parallel aspect of the MARK III recording medium.

A second objective of the proposed correlator is to make it as insensitive to the recording medium as possible. To meet this goal, a trade-off of parallel inputs for higher clock rate data is possible. A recirculating correlator lends itself well to such a trade-off since the data storage in the semiconductor memory and its extraction for correlation are inherently separate operations and can each be structured so as to meet the data formats desired. Thus, any combination of N data inputs at F MHz bit rates can be accommodated if

$$(N)(F) \leq 128, \quad N \leq 32.$$



5 ANT:	10 CARDS	10 CARDS	5 CARDS	7 CARDS	*32 CARDS → 64 CARDS
15 ANT:	30 CARDS	30 CARDS	15 CARDS	60 CARDS	*288 CARDS → 423 CARDS

FIGURE 1: CORRELATOR BLOCK DIAGRAM

In some cases, such as non-polarization observations in which R*L and L*R correlations do not have to be made, this equation can become

$$(N)(F) \leq 256, \quad N \leq 32.$$

Thus, 28 inputs each at a 4 MHz data rate (or 8 MHz for non-polarization) or, say, 4 inputs at 32 MHz, or one at 128 MHz can be processed.

The input block of Figure 1 consists of shift registers that convert the serial data inputs into parallel form for storage in the recirculator memory. Two designs for this card can be envisioned, one with 32 TTL inputs to handle data rates to about 32 MHz, and a second with 4 ECL inputs for data above 32 MHz. The operation and control of either would be relatively simple. Additional designs to, say, convert high speed multiplexed data inputs into multiple lower data rate paths prior to storage in the recirculator are also possible and would be very straightforward (assuming data formats not too complex).

Thus, the correlator input can be made to accommodate a wide variety of input data rates and formats and is hence relatively insensitive to recording medium. Of course, the recorder control circuitry, not even considered here, will have to be designed to satisfy the requirements of specific recording mediums.

One unfortunate feature shown in Figure 1 is that blanking signals, for headswitching, drop-out errors, header bits, sync patterns, etc., must be treated as data, doubling the required input, output, and recirculator stages. Some blanking terms such as headswitching or sync block are track independent but drop-out errors, etc. are not. Thus, I see no alternative to "marking" every data bit as "good" or "bad" by using parallel circuitry to process these blanking signals.

The recirculator will be a RAM memory with a total of 10,240 bits of storage for each of up to 32 tracks. This storage space will allow individual integrations of 8,000 to 9,000 bits at a time plus over 1,000 bits of lag generation. Modern RAM's allow this memory (327 K bits per station for data) to be fairly small. A split memory with simultaneous reading and recording of two tracks is needed to generate R*L and L*R polarization cross products without requiring multiple reads and hence ultra-fast RAM's and more complex circuitry. For spectral line observations a given data track will be written into both halves of the split memory and lags generated by simultaneously reading the split memory from displaced addresses. Thus, no lag generating shift register need be filled that would produce unacceptable inefficiency for short integrations.

The output stage will convert the parallel RAM output to high speed data to drive the correlator.

Up to the output stage all circuitry required has been station dependent. Thus, system expansion, another project objective, is very easy. Past this stage, however, requirements become baseline dependent and expandability becomes more difficult. I have chosen a square matrix system architecture which allows station expansion on an N^2 basis rather than a $\frac{N(N-1)}{2}$ basis. This matrix architecture is reflected in the fringe rotator and correlator portions of the system.

The correlator fits nicely into such a matrix. Consider a PC card with a 5 by 5 matrix of multiplier circuits. Drive one axis of the matrix with the 5 antenna signals and the other axis with the sine output, say, of the fringe generators delayed by M bits and the matrix then produces 1 lead product on one side of the diagonal and 1 lag product on the other side per baseline, and 1 auto product on the diagonal per antenna. A stack of 8 such matrix cards can then produce 8 lead, 8 lag and 8 auto products for all baselines/antennas. Four such stacks can simultaneously generate two sets of complex products (say, R*R and L*L or R*L and L*R).

The clock rate of the correlator cards can be determined later; however, the only two clock rates that seem reasonable at this time are 128 MHz and 256 MHz. The 128 MHz rate would probably be built with ECL 10 K series logic while 256 MHz would require 100 K logic. The main advantage to the 256 MHz clock is that it cuts the number of multipliers required in half.

The fringe rotators can also be put into a matrix configuration by having fringe rate counters for each station set for the natural phase and rate appropriate for the track being extracted from the recirculators and providing a matrix of circuits that use the difference in station fringe rates to obtain baseline fringe rates. Figure 2 illustrates this concept. Since the fringe generators are on the "one track at a time at high bit rate" side of the recirculator, only one counter per station and one matrix are required with the counter counting at the station fringe rate multiplied by the recirculation factor.

Control of this fringe rotation scheme is going to be fairly complicated. Something is going to have to keep up with up to 28 fringe rates per station plus keep up with the fringe phase appropriate to the particular starting bit upon extracting the 8,000-9,000 bit data streams from the recirculator for an integration. A 16-bit microprocessor will probably be required for control of the fringe rotators. Otherwise control of the recirculators, drivers, and multipliers will be simple and straightforward.

The requirement for individual baseline fringe rotation and individual track and baseline blanking will make the signal distribution logic

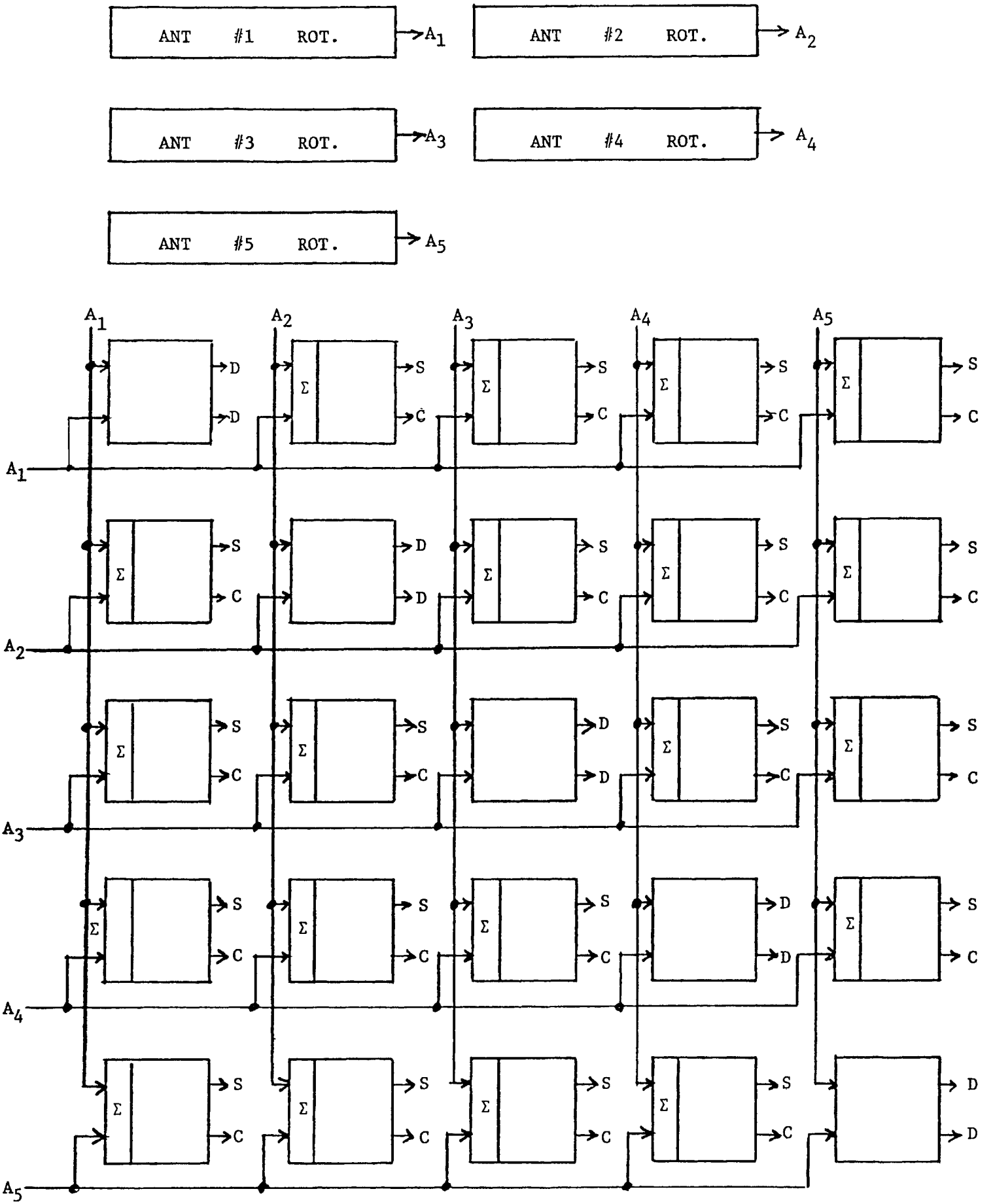


FIGURE 2: FRINGE ROTATORS

and signal cabling more difficult than the simple matrix correlator structure would seem to indicate. At this point it looks as if a 5 X 5 correlator card will need either a 25 X 25 cable input drive or a 25 X 5 drive with 25 blanking signals.

Spectral line observations may be done by restricting the number of inputs used or their data rates. If only 4 input tracks at 4 MHz each are processed, 128 complex lead and 128 complex lag channels may be generated per baseline by recirculating the input data multiple times thru the hardware correlators. Polarized spectral line observations with polarization cross product generation is possible but with one-half either the inputs or lag channels.

In continuum the 28 track MARK III tapes may be processed at a 8 MHz playback rate. Polarization observations will, however, restrict playback to 4 MHz since polarization cross products will be required. In continuum, 8 complex lag channels per baseline will be generated.

Figure 3 illustrates the expandability of this correlator design. Expansion from 5 to 15 stations will require a threefold increase in station related circuitry and a ninefold increase in circuitry in a matrix configuration.

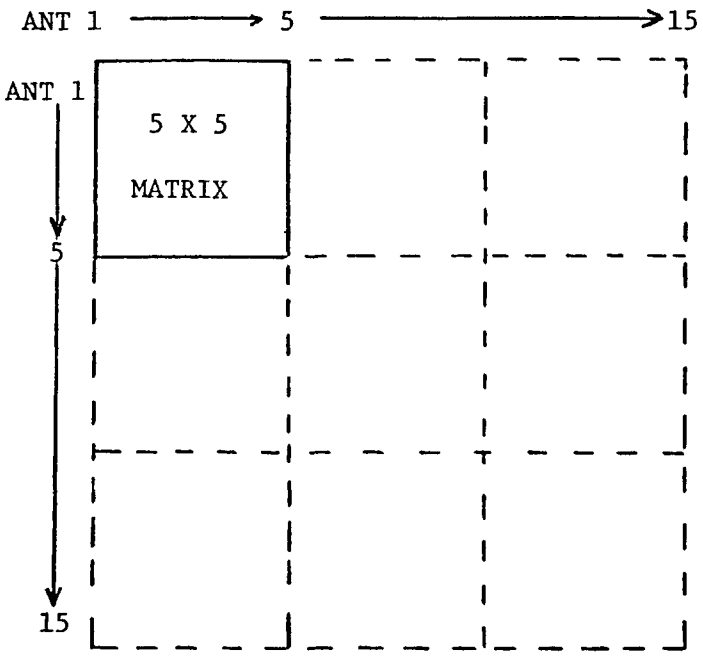
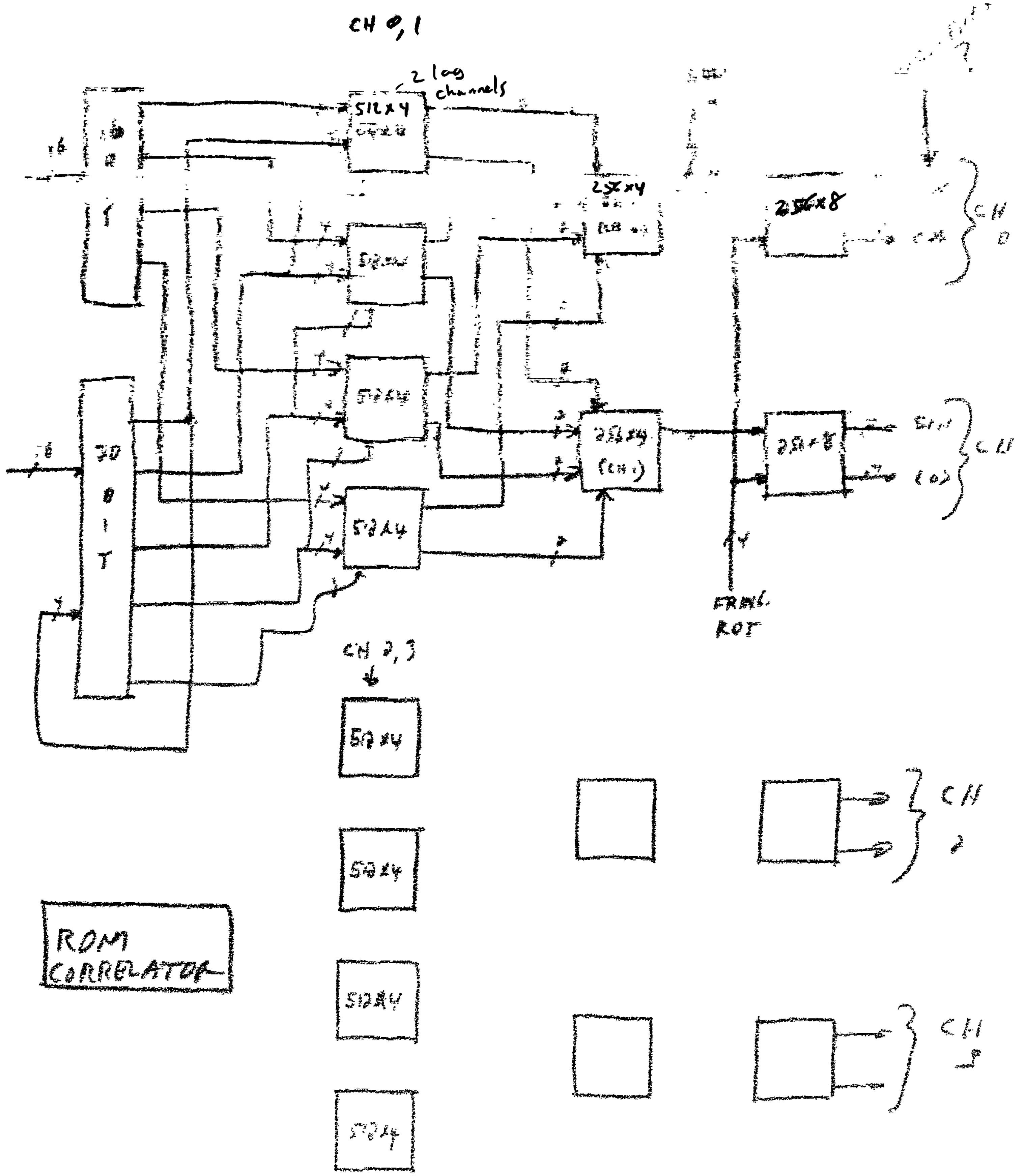
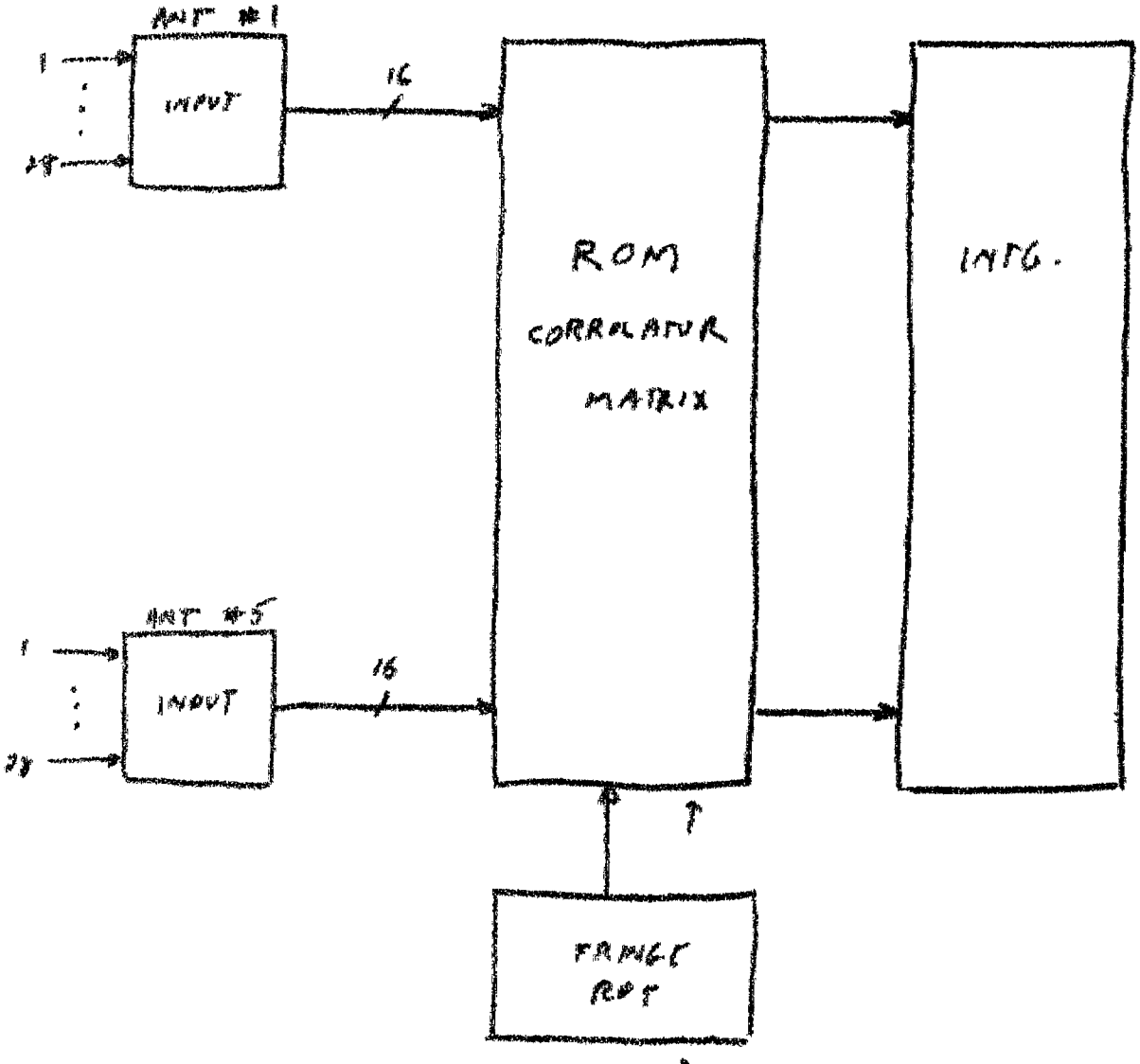


FIGURE 3: SYSTEM EXPANSION



8 BIT REG	4.5	
512x4	8	#24 K
256x4	18	#246
PL. REG	6	
	30.5	

X 50 5 ANT
X 450 15 ANT



5 ANT	5 CARDS	5 CARDS	25 CARDS	25 CARDS	~ 60
15 ANT	15 CARDS	15 CARDS	225 CARDS	225 CARDS	~ 480